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AIR FORCE TO 31W4-2G-12

DIRECT SUPPORT, GENERAL SUPPORT, AND DEPOT MAINTENANCE MANUAL

TELETYPEWRITER CONTROL UNIT C-7050/G

NSN 5815-00-999-3473

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DEPARTMENTS OF THE ARMY, THE NAVY, AND THE AIR FORCE
MAY 1967

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WARNING

DANGEROUS VOLTAGES EXIST WITHIN THIS EQUIPMENT

Be careful when working on the 115-volts or 230-volts ac line connections. Serious injury or death may result from contact with these terminals.

DON'T TAKE CHANCES!

TM 11-5815-335-35
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TECHNICAL MANUAL
No. 11-5815-335-35
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DEPARTMENTS OF THE ARMY,
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DS, GS, AND DEPOT MAINTENANCE MANUAL TELETYPEWRITER CONTROL UNIT C-7050/G

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CHAPTER 1

FUNCTIONING OF TELETYPEWRITER CONTROL UNIT C-7050/G

Section I. GENERAL

1-1. Scope

a. This manual covers direct and general support and depot maintenance of Teletypewriter Control Unit C-7050/G (TCU). It includes instructions for troubleshooting, testing, aligning, and repairing the equipment, replacing maintenance parts, and repairing specified maintenance parts. It also lists tools, materials, and test equipment. A block diagram analysis and detailed functional analysis is also provided.

b. The complete technical manual for this equipment includes TM 11-5815-335-12.

NOTE

For applicable forms and records, refer to TM 11-5815-325-12.

1-2. Indexes of Publications

a. DA Pam 310-4. Refer to the latest issue of DA Pam 310-4 to determine whether there are new editions, changes, or additional publications pertaining to the equipment.

b. DA Pam 310-7. Refer to DA Pam 310-7 to determine whether there are modification work orders (MWO) pertaining to the equipment.

1-2.1. Reporting of Errors

The reporting of errors, omissions, and recommendations for improving this publication by the individual user is encouraged. Reports should be submitted on DA Form 2028 (Recommended Changes to Publications and Blank Forms), and forwarded direct to Commander, US Army Electronics Command, ATTN: DRSEL-MA-Q, Fort Monmouth, NJ 07703 (Army); USAFLC Form 252 (Request for TO Revision or Change) and forward direct to prime ALC/MST (Air Force); or forward to: Commander, Naval Electronics Systems Command, Code 4903, Washington, D.C. 20360 (Navy).

1-2.2 Reporting Equipment Improvement Recommendations (EIR)

a. Army: Reporting Equipment Improvement Recommendations (EIR). EIR will be prepared using DA Form 2407, Maintenance Request. Instructions for preparing EIR are provided in TM 38-750, the Army Maintenance Management System. EIR should be mailed directly to Command, US Army Electronics Command, ATTN: DRSEL-MA-Q, Fort Monmouth, New Jersey 07703. A reply will be furnished directly to you.

b. Navy: Reporting Equipment Improvement Recommendations (EIR). Navy personnel are encouraged to submit EIR through their local Beneficial Suggestion Program.

c. Air Force: Reporting Equipment Improvement Recommendations (EIR). Air Force personnel are encouraged to submit EIR in accordance with AFM 900-4.

1-2.3 Administrative Storage

For procedures, forms, and records, and inspections required during administrative storage of this equipment, refer to TM 740-90-1.

1-2.4 Destruction of Electronic Materiel

Demolition and destruction of electronic equipment will be under the direction of the commander and in accordance with TM 750-244-2.

1-3. Internal Differences in Equipments

All TCU are wired for (but not equipped with) additional components required for operating with voice-frequency control networks (AUTOVON). Refer to TM 11-5815-335-12 for information concerning the additional items required. This manual describes the TCU equipped for AUTOVON operation. If a TCU is not equipped for AUTOVON operation, disregard the text that pertains to operation with the added components.

Section II. BLOCK DIAGRAM ANALYSIS

1-4. General

This section presents a block diagram analysis of the TCU as it operates with an automatic digital message switch (ADMS). Included are two basic subsections: message transmission (to the ADMS), and message reception (from the ADMS). Each subsection presents a description of the processing of a message from beginning to end, including the role of control characters and manual operations. Also included is a description of operation under conditions of abnormality or malfunction. It should be kept in mind that, because the TCU can simultaneously transmit and receive messages, it is advantageous to analyze the TCU as two separate machines. Because the TCU must send control characters associated with received messages and control characters associated with transmitted messages, situations often arrive where these are needed at virtually the same time. The TCU, however, cannot send more than one character (control or data) at the same time; consequently, a priority scheme is attached to control characters. Furthermore, if a situation arises where, at the time the TCU is transmitting data, it is required to send a control character relating to a message being received, the transmission of data is interrupted, the control character(s) is sent, then data transmission is resumed. The analysis of message transmission is presented first, followed by that for message reception.

1-4.1 Mnemonic Designations

The chart below furnishes a reference guide for identifying the mnemonic designations used throughout this manual with their related functions. The *Origin* column defines the assembly from which the signal is generated; the *Destination* column shows the logic board or other assembly, to which the signal is distributed. Each mnemonic has only one point of origin; however, mnemonic designated signals may be distributed to more than one location within the TCU. Certain common control signals with wide distribution are designated Logic Board DISTRIB.

NOTE

Only the primary signaling leads and their associated mnemonics are listed. Such other common leads as dc power potentials, grounds, shields (SH), and twisted returns (TR) are not included in the charts.

AE1160016A

Mnemonic	Related function
ABII	Abnormal Input Device-Indicator
ABNI	Abnormal Input Device.
ABNI-1	Abnormal Input Device-1.
ABNI-3	Abnormal Input Device-3.
ABNO	Abnormal Output Device
ABNO-1	Abnormal Output Device-1
ABNO-3	Abnormal Output Device-3
ABOI	Abnormal Output Device-Indicator
ABON	Abnormal Output-NOT.
ACKV	Acknowledgement Verified
AIOA	Abnormal Input/Output Alarm
AKFP	ACK Flag Pulse
AKOE	ACK-1 Enabled
AKOR	ACK-1 Received.
AKRP	ACK Received Pulse
AKTE	ACK-2 Enabled
AKTR	ACK-2 Received.
ALAI	Alarm Indicator
ALAR	Alarm Reset
ALAS	Alarm Set
ALMN	Allow Message Numbering
AORI	ACK-1 Received-Indicator
AORP	ACK-1 Received Pulse
ATRI	ACK-2 Received-Indicator
ATRP	ACK-2 Received Pulse
AUDA	Audible Alarm
A1TI	ACK-1 Transmitted-Indicator
A2TI	ACK-2 Transmitted-Indicator
BCRN	Baud Counter Receive-Negative
BCRP	Baud Counter Receive-Positive
BCTN	Baud Counter Transmit-Negative
BCTP	Baud Counter Transmit-Positive
BFRL	Buffer Loaded.
BIT1-5	Bits 1 through 5 (each character)
BLDR	Blind Receiver
BLFF	Blind Flip-Flop Flag
BLFN	Blind Flag-NOT
CAMA	Cancel Message Actuator (SW)
CANN	Cancel-NOT
CANR	Cancel Received
CANS	Cancel Sent
CARP	Cancel Received Pulse.
CARP-2	Cancel Received Pulse-2

Origin	Destination
A11	1A1
1A5	1A1 and A11
A11	A14 and A19
Input device	1A5
1A5	1A1 through A4
A4	A5 and A14
Output device	1A5
A4	1A1
A4	A5
A11	A3, A9, and A10
A14	A19
A11	A4 and A10
A4	A11
A2	A3
A11	A14
A4	A11
A2	A3
A19	1A1
1A1	A10 and A19
A19	A14
A15	A17
A3	1A4
A3	1A4, A5, A10, and A11
A3	1A4
A3	1A4, A5, A9, and A11
A14	1A1
A11	1A4
A11	1A4
A7	A6
A7	A6
A7	A8
A7	A8
A18	A8
A18	A19
A5	A2 and A4
A9	A14 and A18
A9	A8
1A1	A9
A9	A10
A2	A3
A9	A14
A3	1A4 and A4
A4	A5

Mnemonic	Related function
CCCP	Control Character Clear Pulse
CCLP	Control Character Load Pulse
CCRT	Control Character Received/Terminat
CCRT-1	Control Character Received/Terminat
CC1P	Control Character 1 Pulse
CC2P	Control Character 2 Pulse
CHAD	Character Detected
CLEP	Clutch Enable Pulse
CLRE	Clutch Reset-Enabled
CLUG	Clutch Gated (current driver)
CLUP	Clutch Picked
CLUP-1	Clutch Picked-1
CLUP-2	Clutch Picked-2
CLUP-3	Clutch Picked-3
CNFG	Cancel Flag
CNFP	Cancel Flag Pulse
CNLI	Cancel-Indicator
COCR	Control Character Received
CONN	Control Sequence-NOT
CPDR	Clutch-Precedence Detected-Reset
CRSE	Crypto Step Enable
CRST	Crypto Step
CRST-1	Crypto Step-1
CRST-2	Crypto Step-2
CRST-3	Crypto Step-3
CSSP	Control Sequence Sync Pulse
CSTP	Control Sequence Timing Pulse
DATI	Date Input
DATI-1	Date Input-1
DATI-2	Date Input-2
DATI-3	Date Input-3
DECAN	Decode *N*
DEMN-9	Decode Message Number (Hundredths)
DEMN-10	Decode Message Number (Tenths)
DEMN-11	Decode Message Number (Units)
DENR	Decoded *N* Received
DISC	Disconnect
DISC-1	Disconnect-1
EDSA	Enable date sample
EMBS	End-of-Message Blind Signal
EMCR	End-of-Message Clock Received

Origin	Destination
A14	A10 and A11
A8	A9, A10, and A11
A6	A2 and A3
A4	A3 and A6
A8	A2 and A9
A8	A9, A10, A11, and A14
A6	A3
A8	A14
A19	A14
A7	A1
A14	1A1
1A1	A7
A1	1A1 through 1A5
1A5	I/O device
A9	A10 and A11
A9	A10
A9	1A1
A6	A3 and A5
A8	A14, A17, A18, and A20
A14	A19
1A1	A9
1A5	1A1
1A1	A9
A9	A8
Crypto	1A5
A14	A9 and A10
A7	A14
1A5	1A1
1A1	A18
A18	A8
Input device	1A5
A18	A14
A15	A16
A15	A16
A15	A16
A2	A4
A13	1A6
1A6	Line ckt interface
A6	A4
A14	A9
A6	A4

Mnemonic	Related function
EMRD	End-of-Message Receive Delay
EMRD-1	End-of-Message Received Delay-1
EMRP	End-of-Message Receive Pulse
EMVP	End-of-Message Verification Pulse
EMVP-1	EOM Verification Pulse-1
ENQF	Enquiry Flag
ENQR	Enquiry Received
ENQS	Enquiry Sent
ENRP	Enquiry Received Pulse
EOMH	EOM Halt
EOMR	EOM Received
EOMS	EOM Sent
ERAD	Enquiry Routine Advance
ERAS	EOM Received-ACK Sent
FLGS	Flag Set
GBRL	Gate-Buffer Loaded
GEMD	Gate-EOM Delay
GIAB	Gate-Input Abnormal
GMDF	Gate-Mark Decode Five
GPPD	Gate-Printed and Punch Device
HALT	Halt TD
HBRE	High Baud Receiver Enabled
HBTE	High Baud Transmitter Enabled
HSCL	High-Speed Clock
LAKR	Incorrect ACK Received
LAK-1	Load ACK-1
LAK-2	Load ACK-2
LBRE	Low Baud Receiver Enabled
LBTE	Low Baud Transmitter Enabled
LCNL	Load Cancel
LDB1-5	Load Data Bits (1 through 5)
LDRT	Load Retransmit
LMPF	Lamp Flash Signal
LOED 0-14	Load Enquiry Device (0 through 14
LOEN	Load Enquiry
LOND-0	Load Numbering Device-0
LOND 1-15	Load Numbering Device-1 through
LPTE	Lamp Test (1A1)
LPTE-1	Lamp Test-1 (1A4)
LRPT	Load Repeat
LSTP	Load Stop
LSTT	Load Start
MAOE	Maintenance ACK-1 Enabled

Origin	Destination
1A1	A4 and A5
1A1	A5
A5	A4
A3	A5
A5	A11, A13, and A16
A20	A18
A2	A3
A20	A4 and A9
A3	A5, A11, and A20
1A1	A14
A4	A5
A14	A3, A9, A10, and A18
A21	A20
A4	A5
A11	A8 and A14
A8	A19
A5	A4
A11	A14
A6	A4
A10	A2
A14	A8 and A19
1A4	A7
1A4	A7
A7	A4, A6, A8, and A20
A11	A9
A11	A19
A11	A19
1A4	A7
1A4	A7
A9	A10, A11, and A19
A19	A18
A10	A19
A14	A10
A20	A21
A20	A21
A15	A16 and A17
A15	A17
1A1	Logic board DISTRIB
1A4	Logic board DISTRIB
A10	A19
A9	A5 and A19
A11	A19
1A4	A4 and A11

Mnemonic	Related function
MATE	Maintenance ACK-2 Enabled
MBLR	Maintain Blind Receiver
MBRE*	Medium Baud Receiver Enabl
MBTE*	Medium Baud Transmitter Er
MCOT	Mark Count of Three
MCSI	Maintenance Control Sequenc Indicator.
MDEA	Message Number Decode Ena
MDEB	Message Number Decode Ena
MDEC	Message Number Decode Ena
MDED	Message Number Decode Ena
MDPT	Message Number Disabled/Pr dence Transfer.
MDRE	Mark Detector Reset
MDRN	Mark Detector Reset-NOT
MDZN	Mark Decode Zero-NOT
MECR	Message Number Counter Res
MEND	Message Number Disabled
MENE	Message Number Enabled
MENR	Message Number Reset
MENS	Message Number Switch (Pres
MEPT	Message Number Enabled/Pr dence Transfer.
MINA-D(1-3)	Message Number Indicator (N puts).
MNFG	Message Number Flag
MNFN	Message Number Flag-NOT
MNFP	Message Number Flag Pulse (
MNRP	Message Number Reset Pulse
MREE	Message Receive Enable
MREI	Message Reception-Indicator
MSTI	Message Transmission-Indicat
MSWE	Maintenance Switch Enabled
MSWR	Maintenance Switch Receive
NEOM	No End-of-Message
PAPD	Printer and Punch Device Dis
PAPG	Printer and Punch Gated
PAPI	Printer and Punch Input
PAPI-1	Printer and Punch Input-1
PAPI-2	Printer and Punch Input-2
PAPI-3	Printer and Punch Input-3
PCCP	Precedence Character Clear Pu
PCDD	Precedence Character Detector

SP
SPI

	Origin	Destination
	1A4	A4 and A11
	A5	A2
l	1A4	A7
bled	1A4	A7
	A6	A3 and A5
	A2	1A4
e (A)	A16	A17
e (B)	A16	A17
e (C)	A16	A17
e (D)	A16	A17
e-	A17	A11
	A4	A6
	A6	A4
	A6	A4
	A16	A15
	1A4	A14, A16, and A17
	A17	A15
	A15	A4 and A14
)	1A1	A16
e-	A5	A11
ie In-	A16	1A1
	A15	A6, A14, A16, and A17
	A16	A15
F Set)	A16	A4, A6, and A15
	A15	A16
	A5	A4
	A5	1A1
	A11	1A1
	1A1	1A4
	1A4	A2
	A14	A11
led	A6	A5 and A10
	A7	A1
	A2	A7
	A1	1A1
	1A1	1A5
	1A5	Output device
e	A14	A19
isable	A9	A18

Mnemonic	Related function
PCDN	Precedence Character Detected-NOT
PCDP	Precedence Character Detected Pulse
PCDS	Precedence Character Detected/ Stored.
PCFT	Precedence Character FF Toggle
PREA-D(1-3)	Preset A through D (1-3) Flip Flop
PREE	Preset Enabled
PREE-1	Preset Enabled-1
PREE-2	Preset Enabled-2
PWRC	Power Clear (+5V momentary clear)
RCOS	Receiver Control Signal
RECD	Receiver Control Disabled
RECN	Receiver Control-NOT
REMA	Receive End-of-Message Alarm
REPA	Repeat Alarm
REPR	Repeat Received
RERP	Repeat Receive Pulse
RETR	Retransmit Received
RPFG	Repeat Flag
RPTI	Repeat 3—Indicator (Alarm)
RRPN	Repeat Receive Pulse-NOT
RTDS	Retransmit Disabled Switch
RTFG	Retransmit Flag
RTRP	Retransmit Received Pulse
RTSA	Retransmit Sent Automatically
RTSI	Retransmit Sent-Indicator (Alarm)
SADA	Sample Data
SARP	Start Receive Pulse
SDAK	Send ACK
SDDP	Send Delay Pulse
SDDT	Send Data Transmit
SDRR	Space Detector Received Reset
SDRS	Space Detector Received Set
SFTP	Shift Pulse (Transmitter)
SGDN	Send Generator Data-NOT
SGDS	Send Generator Data Set
SHTE	Shift Transmit Enable
SMFG	Set Message Number Flag
SMRT	Send Manual Retransmit
SNDA-D(1-3)	Select Numbering Digit A-D (1-3)
SPCN	Start Pulse Control-NOT
SPDR	Start Pulse Detected Receive
SPDT	Start Pulse Detected Transmit

Origin	Destination
A18	A14
A18	A9, A11, A16, and A19
A18	A4, A5, A9, and A14
A9	A18
A15	A16
A16	A5 and A15
A5	A15
A5	A15
1A4	Logic board DISTRIB
A6	A5
A6	A2 and A10
A10	A3 and A6
A5	A19
A10	A9 and A19
A2	A3
A3	1A4, A4, and A5
A2	A3
A10	A11
A10	1A1
A4	A5
1A4	A5
A10	A9 and A11
A3	1A4, A5, A9, A10, A14, and A19
A10	A19
A10	1A1
A6	A3
A3	1A4 and A5
A4	A9, A10, and A11
A8	A9
A8	A19
A6	A4
A6	A4 and A10
A8	A18
A8	A18
A8	A9
A19	A8
A11	A15 and A20
1A1	A3, A5, and A10
1A1	A15
A6	A5
A6	A5 and A7
A8	A7, A13, and A14

Mnemonic	Related function
SPRE	Start Pulse Receive Enable
SPRN	Start Pulse Receive-NOT
SRBC	Shift Receive Baud Clock
SRRC	Stop Received/Repeat Alarm Combined.
SRTP	Set Retransmit Pulse
SSPS	Stop-Stop Send (Auto Retransmit)
SSPW	Start Send Power
SSSW	Start Send Switch
SSTO	Send Stop Once
SSTO-1	Send Stop Once-1
STAR	Start Receive
STCN	Stop Command-NOT
STEN	Start Enable
STOP	Stop-Set
STOP-1	Stop-Set-1
STOP-2	Stop-Set-2
STPF	Stop Flag
STPN	Stop Character-NOT
STPR	Stop Received
STPS	Stop Character Sent
SRTI	Stop Received-Indicator
STRN	Stop Received-NOT
STRP	Stop Receive Pulse
SYSC	System Clear
TCAN	Test Cancel Sequence
TCUD	TCUD Disabled (crypto step control on).
TEMA	Transmitted EOM Alarm
TIFR	Transmission Identifier Flag Reset
TIRE	Transmission Identifier Reset
TITE	Transmission Identifier Transfer Enable.
TREP	Transmit Repeat Sequence (TEST)
TRHI	Transmission Halted-Indicator
TRTS	Transmit Retransmit Sequence (TES
TSEI 1-5	Transmit Shift Enquiry (1-5)
TSIL	Time Six Late (Transmitter)
TSIX	Time Six (Transmitter)
TSLN	Time Six Late-NOT
TSNI 1-5	Transmit Shift Number Input (1-5)
TSTP	Transmit Stop Sequence (TEST)
TSTT	Transmit Start Sequence (TEST)

Origin	Destination
A4	A6
A6	A5
A6	A2
A10	A14
A4	A10
1A4	A3
A18	A9, A10, A13, and A14
1A1	A9 and A18
A4	A9
A5	A4
A2	A3
A9	A4 and A5
A9	A11
A3	A9
A5	A3
A5	A3
A9	A10 and A11
A9	A4
A2	A3
A9	A4 and A5
A10	1A1
A10	A11
A3	1A4, A5, and A10
1A4	1A1
1A4	A9
1A1	A8 and A19
A14	A19
A4	A11
A6	A14
A14	A5
1A4	A10
A14	1A1
1A4	A10
A21	A19
A8	A14, A18, and A20
A8	A5 and A17
A8	A15, A18, and A20
A17	A19
1A4	A9
1A4	A11

Mnemonic	Related function
TSXN	Time Six-NOT (Transmitter)
TTLG	Teletype Line Gated
TTLR	Teletype Line Receive
TTLR-1	Teletype Line Receive-1
TTLR-2	Teletype Line Receive-2
TTLR-3	Teletype Line Receive-3
TTLT	Teletype Line Transmit
TTLT-1	Teletype Line Transmit
TTLT-2	Teletype Line Transmit
TTLT-3	Teletype Line Transmit
UNIN	Unintelligible
ZERB	Zero Buffer

The following TCU signal functions are indicated on logic boards; however, they do not go to a

TATE	Time Eight (Transmitter)
TTTN	Teletype Line Transmit-NOT
TSEV	Time Seven (Transmitter)

*For expansion for other than present system baud rates.

	Origin	Destination
.....	A17	A4 and A15
.....	A7	A1
.....	1A5	1A4 and 1A1
.....	1A1	A2
.....	A2	A3, A4, and A6
.....	Crypto	1A5
.....	A18	A7
.....	A1	1A1 and 1A4
.....	1A1	1A5
.....	1A5	Crypto
.....	A3	A5
.....	A4	A18
ther functional areas:		
.....	A8	Not used
.....	A18	Not used
.....	A8	Not used

1-5. TCU Mode Selection

a. The TCU operates in three modes: NORMAL, TEST, and EMERGENCY as selected on the Control Indicator Panel.

(1) In the NORMAL mode of operation, data transfers between the TCU and the ADMS is performed under control of the TCU.

(2) In the TEST mode of operation, the output of the TCU transmit section is connected to the input of the TCU receive section for test purposes. In this mode, control character transfers occur normally.

(3) In the EMERGENCY mode, the input lines from the ADMS are connected directly to the TTY device (printer or punch), and the TCU is bypassed as a control device. The TCU still has ability to enable clutch or allow CRYPTO STEP to do it. No control characters are generated by the TCU.

b. Throughout the functioning section, operation will be assumed to be on NORMAL mode, unless otherwise specified.

1-6. Block Diagram, Message Transmission

a. Message transmission (fig. 1-1) is initiated when primary power is applied to the TCU. This sends a momentary Power on Clear signal throughout the TCU, and sets the initial conditions into the TCU.

(1) At the Control Character Generator, a cancel flag is generated and applied to the Transmit Baud Counter control character section to produce the timing pulses used during generation of the cancel control sequence.

(2) The Timing Generator supplies a basic clock frequency of twice the transmission baud rate which begins to operate as soon as primary power is applied to the TCU. (The Transmit Baud Counter divides this input by two (to the baud rate) and produces the time pulses on this basis.)

b. The Transmit Baud Counter provides a 600 millisecond (ms) to 1 second time delay which is generated preceding the control characters, then it uses the cancel flag to initiate transmission of a Cancel Control character. All control characters are transmitted as two contiguous identical letters. The Transmit Baud Counter generates a Control Character Load Pulse, which is applied to the CNCL Control Character Generator. The CNCL Control Character Generator generates Load Cancel signal at the appropriate time following the delay. Load Cancel is applied to the Transmit Character Encoder and the transmit Buffer where it loads the buffer with the first of the two contiguous characters. As soon as the buffer is filled (this condition is sensed by the buffer when a one enters one of its five register stages), a buffer filled signal is routed back to the Transmit Baud Counter Shift Control FF. This causes the Transmit Baud Counter to produce shift pulses which serially shift the character out of the Transmit Buffer and Decoder to the ADMS.

c. The Transmit Baud Counter consists of three stages which produce 8 counts, or time pulses. The loading of the Transmit Buffer and Decoder always occurs at Time 6 Late of the Baud Counter (halfway between counts 6 and 7). Shifting begins at count 8. Thus, there is always a minimum time of 1 1/2 baud counts between loading and start of shifting. This permits a minimum rest interval of approximately 1 1/2 baud times between any two characters.

d. After the first of the two characters (which comprise cancel) is sent to the ADMS, the Transmit Baud Counter produces a control character 2 pulse which again causes the load cancel to load the Transmit Buffer and Decoder. The second character is then shifted out serially to the ADMS.

e. The ADMS replies with an ACK-2 (Acknowledge-2) control sequence, which consists

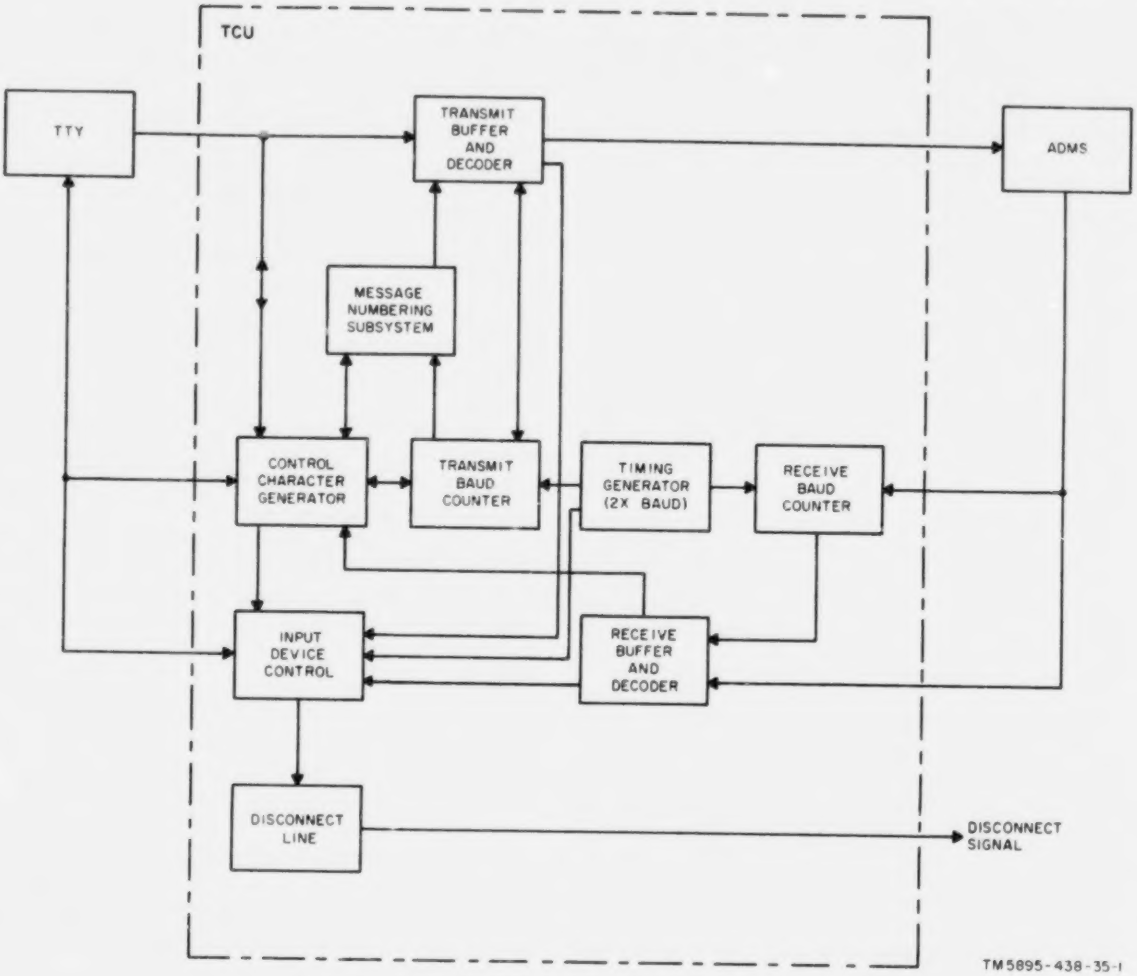
TCU
TTY
TRANSMIT BUFFER AND DECODER
ADMS
MESSAGE NUMBERING SUBSYSTEM
CONTROL CHARACTER GENERATOR
TRANSMIT BAUD COUNTER
TIMING GENERATOR (2X BAUD)
RECEIVE BAUD COUNTER
INPUT DEVICE CONTROL
RECEIVE BUFFER AND DECODER
DISCONNECT LINE
DISCONNECT SIGNAL
TM5895-438-35-1

Figure 1-1. Message transmission, block diagram.

of two contiguous letters. Assuming this is done, ACK-2 is applied from the ADMS to the Receive Buffer and Decoder. The Receive Buffer register portion of the Receive Buffer and Decoder consists of seven stages, a start stage, five intelligence stages, and a line interface stage. During idle conditions this register is loaded with all ones. A start bit, which precedes each character received, enters the Receive Buffer and Decoder, which detects this start condition. The Receive Baud Counter, which is supplied by the Timing Generator and begins to operate as soon as primary power is applied, counts at twice the input baud rate. This counter is synchronized to the input data by the Detected Start Signal. Start detection is made by means of a 7500-cps highspeed clock, which is generated in the Timing Generator and continually samples the line between characters. The counter also generates shift pulses which shift the input character serially into the Receive Buffer and Decoder. The Receive Buffer and Decoder then decodes the two input characters which are decoded as the ACK-2 response, and an ACK-2 pulse received signal is applied to the Control Character Generator to turn off the cancel flag.

f. The Operator then presses Start Send Switch; which resets the Cancel Sent logic. The resetting of this flag is detected in the Input Device Control logic. If all other necessary factors are normal at this time, the Input Device Control generates a clutch pulled signal to the TTY input paper tape reader. This tells the TTY input device to start sending information to the TCU. The TTY device responds by sending characters to the TCU. The TCU in this intermessage mode steps along a character at a time, looking for a precedence character, keeping the line to the ADMS blind (a constant mark). The precedence character initiates the actual start-of-message transmission.

g. When any character is applied to the TCU from the TTY device, the Transmit Baud Counter detects the start bit of this character. This synchronizes the Transmit Baud Counter with the incoming character. Shifting of the character into the Transmit Buffer and Decoder is then accomplished by the Transmit Baud Counter. When the Transmit Buffer and Decoder is loaded with a precedence character in the intermessage mode, this condition is decoded in the Transmit Buffer and Decoder. The results of this decoding also causes the precedence character to be stored in an auxiliary buffer within the Transmit Buffer and Decoder. The precedence character is then shifted out of the transmit buffer under control of the Transmit Baud Counter. However, at this time, the ADMS is blinded; thus shifting serves only to clear the Transmit Buffer and the ADMS does not receive the precedence character.

h. The receipt of the precedence character in the TCU also sets the Start Flag. This initiates transmission of a control sequence which may be START, or any other control sequence being transmitted. The control sequence consists of two contiguous letters which are loaded into the Transmit Buffer and Decoder and transmitted to the ADMS under control of the Transmit Baud Counter. The detection of the precedence character is used to set logic, the output of which is applied to the Input Device Control to inhibit the TTY input device from sending data to the TCU during the transmission identifier.

i. After the control sequence is transmitted, a signal is applied to the Message Numbering Subsystem, which initiates transmission of SOM (Start-of-Message). SOM follows control character and precedes the actual message data. The transmission identifier (TI) consists of VZCZC [ABC] FIGS [000] Ltrs, CR, CR, LF.

j. The Message Numbering Subsystem contains a four-state binary counter which provides up to 16 counts, and whose rate of counting is controlled by the Transmit Baud Counter. The Message Numbering Subsystem counter advances at each time 6 of the Transmit Baud Counter, thus, a complete character can be sent to the ADMS during each Message Numbering Count. The TI consists of up to 16 characters and contains information of a general nature as well as information peculiar to a particular TCU site. The Message Numbering Subsystem contains an encoder which generates the particular SOM character at each stage advance of the Message Numbering Subsystem counter. The Transmit Baud Counter controls loading of the TI characters into the Transmit Character Encoder and the shifting of each character to the ADMS. In this case, the Transmit Buffer and Decoder is loaded from the encoded outputs of the Message Numbering Subsystem.

k. After the final SOM character is sent to the ADMS, the Message Numbering Subsystem is reset, and this status is detected in the Control Character Generator. This results in a Precedence Character Transmit Pulse being applied to the Transmit Buffer and Decoder at the following Time 6 of the Transmit Baud Counter. This loads the precedence character from the auxiliary buffer into the Transmit Buffer, and under control of the Transmit Baud Counter, the precedence character is sent to the ADMS.

l. The Input Device Control, which had also sensed the resetting of the Precedence flip-flop by the transferring into the XMIT buffer of the precedence character, generates a clutch pull signal that energizes the clutch of the input TTY device. This enables the TTY device to begin sending data characters, one after another, to the Transmit Buffer and Decoder where, under control of the Transmit Baud Counter, data characters are sent to the ADMS.

m. An end-of-message sequence denoting the end of the transmitted message, is detected in the Input Device Control. This causes an EOMS (End-of-Message Sent) signal to be sent to the Control Character Generator. The Control Character Generator, under control of the Transmit Baud Counter, sends a Repeat Control sequence (a pause and two contiguous R's), to the ADMS via the Transmit Buffer and Decoder. This informs the ADMS that the TCU has sent its message and expects an acknowledgement. If operation is normal, an acknowledgement is the correct ACK response, and the ADMS sends the correct ACK response to the TCU. The TCU receives the ACK response in two contiguous letters, at the Receive Buffer and Decoder, under control of the Receive Baud Counter. The ACK response is then decoded in the Receive Buffer and Decoder as the appropriate ACK received pulse. This pulse is applied to the Input Device Control, which generates an End-of-Message-Verified pulse indicating a message has been successfully transmitted, has been correctly acknowledged, and that the TCU is conditioned to send subsequent messages.

n. The End-of-Message-Verified pulse is applied to the Message Numbering Subsystem and advances a message numbering decimal counter one step, which in turn, sends this status to the Control Indicator panel for visual display. This denotes successful acknowledgement of a message. This condition is detected by the Input Device Control which energizes the clutch of the TTY, initiating the search for the next precedence character. See *h* above. Also, between the time that the End-of-Message-Verified pulse is generated and the precedence character for the next message is sent to the TCU, i.e., the intermessage state, and End-of-Message-Blind Set signal is generated by the Input Device Control. This prevents the receiver (ADMS) from receiving characters which may be present on the paper tape of the TTY input device, during the intermessage state.

1-7. Block Diagram, Abnormal Message Transmission

a. When malfunctions are encountered during transmission, the message transmission operation alters somewhat. *For example*, if during transmission of the message, there is trouble at the ADMS, the ADMS will send a Stop Control character to the TCU. The Receive Buffer and Decoder converts this to a Stop Receive Pulse which is applied to the Control Character Generator. This condition sets the TCU repeat control character flag in the Control Character Generator. Since control characters have priority over data characters, this flag is sensed in the Input Device Control and disables the TTY Input Device clutch, stopping the TTY device from sending any more data while the abnormal condition persists. The Transmit Baud Counter loads the repeat into the Transmit Buffer and Decoder (in two contiguous) letters, and sends them to the ADMS. The ADMS then responds with a retransmit (RT) control sequence which is sent to the Receive Buffer and Decoder and is converted by the Receive Baud Counter to the retransmit receive pulse. This pulse is sent to the Control Character Generator, which under control of the Transmit Baud Counter, results in a cancel control character being sent to the ADMS via the Transmit Buffer and Decoder. This tells the ADMS that the TCU will scrap the message and retransmit it. The ADMS must then respond with ACK-2 which results in retransmission of the message by the TCU to the ADMS.

b. Once the TCU has sent its message, it sends a repeat to which the ADMS would normally respond with the correct ACK response. Abnormal conditions at the ADMS may preclude this; however, and in this case the ADMS sends a stop to which the TCU responds with another REPEAT. This is continued until the ADMS eventually clears its trouble and sends the correct response.

c. Other abnormal conditions may result in the transmitted message being manually cancelled at the TCU by operator action at the Control Indicator panel. In this case, message transmission is abruptly stopped, a cancel is sent to the ADMS, the ADMS responds with ACK-2, and the TCU retransmits the message.

d. Each time a cancel or repeat is sent to the ADMS during normal or abnormal operation, the ADMS must respond with an appropriate control character by the time that three repeats or cancels are sent to the ADMS. If a response is not received in time, an alarm condition, detectable at the Control Indicator Panel, is produced, which requires subsequent REPEATS or CANCELS to be sent. This is initiated at the Control Indicator Panel by pressing the start send switch. If a response is still not received in time, other means must be initiated to correct the trouble. The time between successive repeats or cancels is from two to four seconds. The time-out is produced in the Input Device Control and is supplied from the Timing Generator. The counting of the three repeats or cancels is accomplished in the Control Character Generator which, under the adverse conditions just described, initiates the alarm conditions.

e. A final type of adverse condition which may be encountered during message transmission, is abnormal operation of the TTY. In this case, the abnormal condition is sent from the input TTY device to the Input Device Control which in turn, disables the clutch of the input device, bringing a halt to transmission from the TTY input device to the TCU and producing an audible and visual alarm at the Control Indicator Panel when the TCU is in the intramessage state. The abnormal condition is also sent to the control character generator so that once the alarm condition is cleared, a START character(s) is sent to the ADMS as a dummy character(s) until data transmission is resumed. Once the START has been sent to the ADMS, this condition is cleared by the Input Device Control, which produces clutch pull, pulling the clutch of the TTY input device, resuming transmission of characters. The above does not occur until the abnormal condition goes away and, if it persists, other means must be undertaken to resume message transmission.

f. On TCU's which are equipped with AUTOVON logic, an End-of-Message-Verified pulse is sent by the Input Device Control to the Disconnect Line where it starts a 15-second timeout. If a subsequent message to be transmitted occurs within this 15-second period, as denoted by a Start Pulse Detected Transmit pulse from the Transmit Baud Counter, the timeout sequence is restarted with the next EOM verified pulse. If a Start Pulse Detected Transmit pulse is not received by the Disconnect Line within 15 seconds, the timer sends a disconnect signal to the enquiry response and disconnect line feature logic, which halts digital message transmission. Subsequent message transmissions can be resumed by AUTOVON communication between the TCU and the ADMS.

g. The TCU can also stop the sending of messages by manual operation of a control indicator panel stop at EOM switch. If this is done, the current message is allowed to finish and then the Input Device Control sends an End-of-Message alarm and stops the TTY input device from sending any more data. When message transmission is ready to be resumed, the TCU operator actuates the Control Indicator Panel START SEND switch. This resets the signal which had disabled the TTY input device.

1-8. Block Diagram, Message Reception

(fig. 1-2)

a. At some point after power has been applied to the TCU, the ADMS sends a cancel to the TCU to initiate message reception. The cancel control character is applied to the Receive Buffer and Decoder as two contiguous letters. The first of these is applied to the input of the Receive Buffer and Decoder. During the idle condition following power turn-on, the lines from the ADMS to the TCU are in a mark condition, which is the idle condition. The Receive Baud Counter is driven by the Timing Generator and is counting at the selected receive baud rate. The input from the Timing Generator is twice the baud rate, but a frequency divider (by two) is included in the Receive Baud Counter to provide the proper baud rate.

b. In order that the TCU not confuse reception of a control sequence with data, a minimum time of between 170 and 480 milliseconds must have elapsed from the last character received. The TCU receive baud counter includes logic which detects this condition.

c. The start bit of the first cancel character is detected by the Receive Baud Counter by way of the Receive Buffer and Decoder. This synchronizes the Baud Counter with the input data. Sampling for the presence of data is made by a high-speed clock in the Timing Generator which is applied to the Receive Baud Counter. The detection of input data results in the generation of a shift Receive Bit Clock pulse in the Receive Baud Counter which is applied to the Receive Buffer and Decoder, shifting in the characters. Once the character is completely shifted in, a decoding network located in the Receive Buffer and Decoder, decodes the 5-bit baud character into the first of the cancel characters. A Mark counter, located in the Receive Baud Counter, advances each time the baud counter advances through a complete cycle. The Mark counter ascertains that at least three marks (three cycles of the Baud Counter) have elapsed before a control character can be received. Once this is checked and found to be true, the first character is decoded and held in the Receive Buffer portion of the Receive Buffer and Decoder. At the same time, the Output TTY device is disabled so that it cannot print out the control character. As soon as the second character of the cancel control character is detected in the Receive Control logic, a

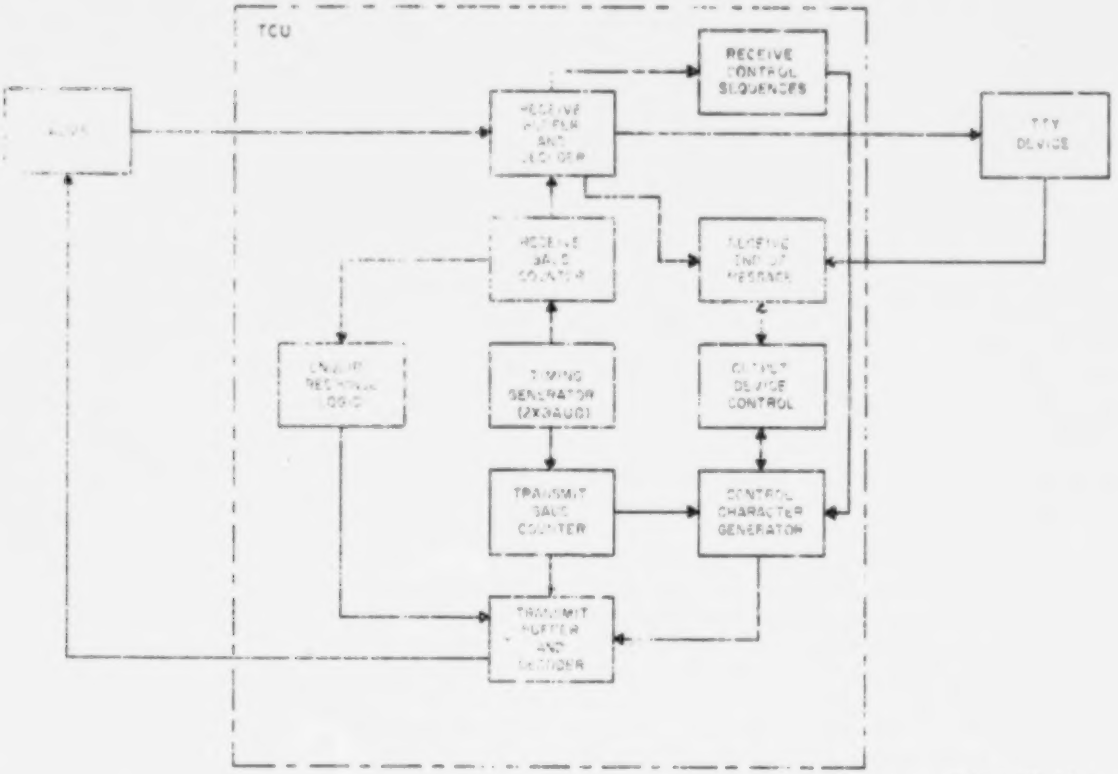
TCU
ADMS
RECEIVE CONTROL SEQUENCES
RECEIVE BUFFER AND DECODER
TTY DEVICE
RECEIVE BAUD COUNTER
RECEIVE END OF MESSAGE
CANCEL RECEIVE LOGIC
TIMING GENERATOR (2X3AUG)
OUTPUT DEVICE CONTROL
TRANSMIT BAUD COUNTER
CONTROL CHARACTER GENERATOR
TRANSMIT BUFFER AND DECODER
TM5895-435-35-12

Figure 1-2. Receive section, block diagram.

Cancel Receive pulse is generated by this logic and applied to the Control Character Generator. This results in an Acknowledge flag being set. This signal causes two ACK-2 contiguous characters to be loaded into the Transmit Buffer Decoder. Shift pulses from the Transmit Baud Counter then shift the first ACK-2 character to the ADMS. Next, the Transmit Baud Counter produces a control character-2 pulse which is sent to the Control Character Generator to load the second half of ACK-2 into the Transmit Buffer and Decoder. The Transmit Baud Counter then shifts the second ACK-2 character to the ADMS. This acknowledges the fact that the TCU has received the CANCEL.

d. Once the ADMS receives ACK-2, it sends a control sequence to the TCU. This control sequence is received as two contiguous letters and is converted into a pulse in the Receive Control logic. This pulse is applied to the Output Device Control and allows the forthcoming data message to be shifted through the Receive Buffer into the TTY output device (printer or punch). At this point, the ADMS sends its TI (which is similar to that generated by the TCU for transmitted messages), then sends the message data. The TI is printed out on the TTY output device along with the data characters.

e. Assuming that the data message is received without any malfunctions or abnormalities, the last part of the message, the EOM sequence is received in the Receive Buffer and Decoder where it is detected and sent to the End-of-Message Received logic. The End-of-Message Received logic converts this to the End-of-Message Received signal. This is applied to the Output Device Control.

f. After sending the EOM, the ADMS sends a repeat control character which is received by the TCU as two contiguous letters. These are converted to a Repeat Receive Pulse. This is applied to the Output Device Control and combines with EOM signal, producing the End-of-Message Received pulse.

g. The End-of-Message Received pulse represents the successful receipt of the message and is used to set the proper Acknowledge flag. At this point the TTY output device is blinded. Under control of the Transmit Baud Counter, the appropriate acknowledge is sent to the Transmit Buffer and Decoder where it is encoded into the two letters, and shifted to the ADMS. The TCU is now in condition to receive a subsequent message. During the time between which the acknowledge is sent to the ADMS and the first printable character of a subsequent message is received, the Output TTY device blind is retained.

1-9. Abnormal Message Reception, Block Diagram Analysis

a. During the rest interval of every received character, the TCU samples the data line for the presence of this rest interval. If the rest interval is not present, this condition is detected in the Receive Control Sequence and results in the generation of a STOP signal, which is applied to the Control Character Generator.

b. STOP results in the setting of the STOP flag and under control of the Transmit Baud Counter, the STOP control character is loaded into the Transmit Buffer and Decoder and shifted out to the ADMS. The ADMS in turn immediately stops transmitting the message to the TCU. The ADMS then responds with a repeat Control Character which is converted in the TCU Receive Control Sequence as the repeat receive pulse. This pulse is applied to the Receive End-of-Message and is used to generate a Send Retransmit pulse.

c. The Send Retransmit pulse is applied to the Control Character Generator via the Output Device Control. This pulse initiates transmission of the Retransmit Control character. Under control of the Transmit Baud Counter, the Retransmit Control character is loaded into the Transmit Buffer and Decoder and sent to the ADMS. This requests that the ADMS retransmit the message. The ADMS replies with a cancel which states in effect that the ADMS agrees with the TCU, will scrap the message, and will retransmit. The cancel is decoded in the Receive Control Sequence as a Cancel Receive pulse. This pulse is applied to the Control Character Generator and sets an ACK-2 flag. Under control of the Transmit Baud Counter, ACK-2 is loaded into the Transmit Buffer and shifted out to the ADMS. The ADMS can now retransmit the message.

d. If there is trouble in receiving the original message due to abnormal operation of the TTY Output Device, the message is allowed to be received by the TCU, before the TCU takes action. Once End-of-Message-Receive is generated in the End-of-Message logic, it is applied to the output device control. The abnormal TTY Output Device status signal (ABNO) is applied through the Receive-End-of-Message logic to the Output device control. Upon receipt of an ensuing repeat control character from the ADMS which results in an indication to this effect in the Output Device Control, a SSTO-1 (Send Stop Once) pulse is generated. This is applied to the Control Character Generator, setting the STOP flag. Then under control of the Transmit Baud Counter, STOP is sent to the Transmit Buffer and shifted out to the ADMS. The ADMS then responds with repeat to which the TCU sends its response. If the abnormal output device condition persists, the TCU will keep sending STOPS followed by receipt of repeats until the abnormal condition is corrected, in which case the TCU will send an acknowledge (and be in condition to receive a subsequent message).

e. An option available to the TCU is to manually request retransmission of an incoming message. The TCU operator may initiate a retransmission of the message being received by manually operating the REQUEST MES switch. The TCU initiates the sequence by sending a STOP to the ADMS. The ADMS replies by sending a REPEAT to the TCU. The TCU then replies by sending a RETRANSMIT to the ADMS. The ADMS replies by sending a CANCEL to the TCU. The TCU returns ACK-2 to the ADMS. The ADMS may then retransmit the message.

f. A message can also be stopped manually from the TCU by operation of the Control Indicator RECEIVE at EOM switch. In this case, the message is allowed to be received by the TCU and STOP is actually sent after the TCU has received the ensuing repeat from the ADMS. The ADMS then replies to STOP with repeat. The stop-repeat transfers are continued until the TCU operator restarts message reception by actuating the CONTINUE switch. Following this, the TCU receives another repeat, then acknowledges the message. This method of stopping a message results in a REMA (receive End-of-Message Alarm) which in turn results in an audible and visual alarm indication at the Control-Indicator Panel.

g. If a problem arises during reception of a message which the ADMS recognizes, but the TCU does not, the ADMS can cancel the message manually. In this case, the TCU receives a cancel control character which enters the Receive Buffer, is decoded and, under control of the Receive Baud and Mark Counter, is converted to the cancel pulse. This is applied to the ACK control character generator, it sets the ACK-2 flag, and, under control of the Transmit Baud counter, loads the ACK-2 into the Transmit Buffer and shifts ACK-2 to the ADMS. The ADMS may then start the message over.

h. Some TCU's are equipped with Enquiry Response/Disconnect Line interface logic. These are at times requested by the ADMS to send their special response routing indicator. This consists of a variable number of characters (form 12 to 15) depending upon the particular TCU site. The ADMS request this response by sending an enquiry control character to the TCU. The TCU receives this in the Receive Buffer and control. The Receive Control section decodes it into an enquiry Receive pulse. This pulse is sent to the Control character generator, setting the START flag. Under control of the Transmit Baud counter, the START control character (or any control sequence) is loaded into the Transmit Buffer and shifted out to the ADMS. Following transmission of the control sequence, a flag is set in the Enquiry Response Generator and Encoder, which enables an Enquiry Counter. This counter is slaved to the Transmit Baud Counter so that each time the Baud counter counts through a complete cycle, the enquiry counter, which consists of four stages, enabling a count of 0 to 15, is advanced. Each advance of the Enquiry counter is applied to an encoder which selects a certain character. By advancing the enquiry through its entire cycle, the complete enquiry response routing indicator is transmitted to the ADMS. Each character is loaded into the Transmit Buffer through the Transmit Buffer Encoder and, under control of the Transmit Baud counter, is shifted out to the ADMS. Certain Enquiry response characters are standard; others vary per TCU. The choice of which variable characters comprise the routing indicator is made by patchable connections on the Enquiry response logic cards. The Routing Indicator is a variable 4 to 7 characters depending upon the particular TCU.

i. In the Receive Control, as previously mentioned, two contiguous control characters are converted to a control character received pulse. If a control character is forthcoming but is not completed, a UNIN (unintelligible) signal is generated, indicating that the character is not recognizable. This signal is sent to the Output Device Control. If the TCU is not in the End-of-Message receive mode, has not sent a stop, has not disabled the retransmit capability, and is not receiving a message, MBLR is produced (Maintain Blind on Receiver). MBLR is then sent to the Receive Buffer.

j. MBLR is also produced if the condition of UNIN is replaced by RERP (REP receive pulse). The significance of these conditions is that more than one repeat is being received.

Section III. INITIAL POWER-ON CONDITION

NOTE

The OR circuits described and represented in paragraphs 1-10 through 1-69 should be verified with the schematic diagrams to determine that the circuits perform a logic (OR) or a logic (NOR) function.

1-10. General

When power is turned on initially, the TCU circuits are set to a prescribed state. This is accomplished by +5 volts being supplied from the power supply through contacts 8-9 of relay A1K1 (fig. 1-3), through terminal A1J1-1 over the system clear (SysC) lead to A4J1 pin 9 contacts 1-2 of the SysC switch, through resistor A4R4, 10 of pin A4J1, to various points in the TCU logic as the PWRC (Power Clear) lead. The following paragraphs describe the functions of the PWRC lead. Observe that relay A1K1 operates when the ±12 volts and the +5 volt supplies are operating. The time it takes the relay to energize determines the width of the PWRC pulse. Thus, the PWRC lead contains a pulse. If, during operation of the TCU, it is desired to set the TCU to the cleared position, the SysC switch on the control and indicator panel is depressed momentarily. This action provides +5 volts on the PWRC lead while the switch is depressed.

1-11. A2A2, Receive Buffer and Decoder PL-1139/G, Power On Functional Analysis

(fig. 1-4)

a. The Power on clear (PWRC) high signal is applied to A2A2P1-22. From here it is applied to input 8 of OR 15B, which operates with OR 15A as a flip-flop. Output 10 of OR 15 goes low and is applied to input 3 of OR 15A. Input 4 OR 15A is low since it is grounded. Input 5 of OR 15A is normally low, from the CONT SEQ. SIMULATOR switch. Output 2 of OR 15A goes high and is applied to input 9 of OR 15B. This locks the flip-flop in this position despite the fact that PWRC becomes disabled. The low output 10 of OR 15B is applied through resistor R2 to the base of Transistor Q1 and extinguishes the lamp. Resistor R1 provides a high resistance path to the Maintenance Control switch Indicator, to keep the filament hot (not incandescent) to extend lamp life.

b. PWRC is also applied to input 8 of OR 10B. Output 10 of OR 10B goes high and is applied to the direct set (P) 3 input of Receive Buffer FF 3, 8, 13, 18, 23, and 24, setting them (loading them with a MARK).

c. PWRC is also applied to input 5 of OR 5A. Output 2 of OR 5A goes high and is applied to input 9 of OR 5B. Output 10 of OR 5B goes high and is applied to the direct set input 3 (P) of FF 25, the Receive Buffer Line Interface flip-flop; setting it and thus loading it with a mark.

1-12. A2A3, Receive Control Sequences PL-1141/G, Power On Functional Analysis

(fig. 1-5)

a. PWRC is applied to input terminal A2A3A1-45. From here it is applied to input 5 of OR 3A. Output 2 of OR 3A goes high and is applied to input 9 of OR 15B. Output 10 of OR 15B is applied to input 8 of OR 20B, which operates with OR 20A as a flip-flop. Output 10 of OR 20B goes low and is applied to input 4 of OR 20A. Input 5 of OR 20A is low since it is grounded. Input 3 of OR 20A is low because the Receive Mark Counter is not in a count of three (because of PWRC). Output 2 of OR 20A goes high and is applied to input 7 of OR 20B. This locks the flip-flop in this state even after PWRC is disabled. The low output 10 of OR 20B is applied to input 7 of AND 25B, diabling the unintelligible signal decode.

b. PWRC is also applied to input 3 of OR 2A. Output 2 of OR 2A goes high and is applied to the direct reset 8(c) input flip-flops 6, 11, 12, 17, 19, 13, 24 and 22, the control character receive flip-flops. This high level transition clears these flip-flops.

1-13. A2A4, Receive End of Message PL-1142/G, Power On Functional Analysis

(fig. 1-6)

a. PWRC is applied to input terminal A2A4P1-36. From here it is applied to input 9 of OR 9B, which operates with OR 9A as a flip-flop. Output 10 of OR 9B goes low and is applied to input 3 of OR 9A. Input 5 of OR 9A is low because it is grounded. Input 4 of OR 9A is low because the Space Detect Receive set signal is disabled. The high output 2 of OR 9A is applied to input 7 of OR 9B. This locks the flip-flop in this condition even after PWRC is disabled. The low 10 output of OR 9B disables the Start Pulse Receive Enable Signal.

b. PWRC is also applied to input 7 of OR 11B, which operates with OR 11A as a flip-flop. Input 5 of OR 11A is low since it is grounded. Input 3 of OR 11A is low since GMDF is made low by PWRC. The high output 2 of OR 11A is applied to input 9 of OR 16B. This disables the Control Character Receive Terminate signal by causing output 10 of OR 16B to be low. Pin 2 of OR 11A connected to 8 of OR 11B locks the flip-flop in this condition even after PWRC is disabled.

c. PWRC is also applied to input 4 of OR 6A. Output 2 of OR 6A is high and is applied to the direct reset 8(C) input of flip-flops 19, 20, and 18 (N's counter for received Messages); clearing them.

d. PWRC is also applied to input 3 of OR 12A. Output 2 of OR 12A is high and is applied to the direct set 3(P) input of flip-flop 17; setting this flip-flop. This assures that the first ACK transmitted will be an Acknowledge 2.

1-14. A2A5, Output Device Control PL-1157/G, Power On Functional Analysis

(fig. 1-7)

a. PWRC is applied to input terminal A2A5 P1-7. From here, it is applied to input 9 of OR 6B. Output 10 of OR 6B goes high and is applied to input 3 of OR 22A. Output 2 of OR 22A, which operates with OR 22B as a flip-flop, goes low and is applied to input 9 of OR 22B. Input 8 of OR 22B is low because it is grounded. Input 7 of OR 22B is low because AND 14B is disabled, by PWRC (Pin 9). Output 10 of OR 22B goes high and is applied to input 5 of OR 22A, locking the flip-flop in this condition, even after PWRC is disabled. The low output 2 of OR 22A is applied through Resistor R2 to the base of Transistor Q1, cutting it off and extinguishing the lamp. Resistor R1 provides a high resistance path to the Receive Indicator on the Maintenance Panel, extending lamp life.

b. PWRC is also applied to input 4 of OR 23A, which operates with OR 23B as a flip-flop. Output 2 of OR 23A goes low and is applied to input 7 of OR 23B. Input 8 of OR 23B is low because it is grounded. Input 9 of OR 23B is low because AND 18A is disabled when OR 16A is set by PWRC. Output 10 of OR 23B goes high and is applied to input 5 of OR 23A, locking the flip-flop in this condition even after the PWRC signal is disabled. The low output 2 of OR 23A disables the Receive EOM Alarm

c. PWRC is also applied to input 8 of NOR 16B. The low output 10 of OR 16B which operates with OR 16A as a flip-flop, is applied to input 3 of OR 16A. Input 4 of OR 16A is low since the cancel receive pulse is disabled. Output 2 of OR 16A goes high and is applied to input 9 of OR 16B, locking the flip-flop in this condition, even after PWRC is disabled. This action disables EOM receive, sending of stop, and the gated End-of-Message Delay.

d. PWRC is also applied to input 4 of OR 6A. Output 2 of OR 6A goes high and is applied to input 5 of OR 11A, which operates with OR 11B as a flip-flop. Output 2 of OR 11A goes low and is applied to input 7 of OR 11B. Input 8 of OR 11B is low since it it grounded. Input 9 of OR 11B is low because AND 20A is disabled by PWRC (OR 5A pin 5). Output 10 of OR 11B goes high and locks the FF to desired state. The low output 2 of OR 11A disables the MBLR (Maintaining of Blind on TTY receiver).

e. PWRC is also applied to input 9 of OR 19B, which operates with OR 19A as a flip-flop. Output 10 of OR 19B goes low and is applied to input 5 of OR 19A. Input 3 of OR 19A is low because it is grounded. Input 4 of OR 19A is low because output 2 of AND 14A is disabled, since PWRC also makes the output 10 of OR 9B low. Output 2 of OR 19A goes high and is applied to input 8 of OR 19B locking the flip-flop in this condition, even after PWRC is disabled. The low 10 output of OR 19B is applied to input 4 of AND 2A. Output 2 of AND 2A is low and is applied to input 7 of OR 16B. This enables the Power On flip-flop (ORs 16A and 16B) to be reset later when the TCU transmits a stop.

f. PWRC is also applied to input 7 of OR 7B. Output 10 of OR 7B is high and is applied to input 7 of OR 12B, which operates with OR 12A as the Intramessage flip-flop. Output 10 of OR 12B goes low and is applied to input 5 of OR 12A. Input 3 of OR 12A is low because it is grounded. Input 4 of OR 12A is low since PWRC reset the Control Character Receive flip-flops. Output 2 of OR 12A is high and is applied to input 8 of OR 12B, locking the flip-flop in this condition even after PWRC is disabled. The high output 2 of OR 12A produces the BLDR signal. This blinds the Output TTY device after an acknowledge has been sent during the Intermessage state, or on PWR On or System Clear.

g. PWRC is also applied to input 4 of OR 7A. Output 2 of OR 7A goes high and is applied to input 9 of OR 9B, which operates with OR 9A as a flip-flop. Output 10 of OR 9B goes low and is applied to input 5 of OR 9A. Input 3 of OR 9A is low because it is grounded. Input 4 of OR 9A is low because AND 4A is disabled since PWRC reset the Control Character Receive flip-flops. Output 2 of OR 9A goes high and is applied to input 8 of OR 9B, locking it in this condition even when PWRC is disabled. The low output 10 of OR 9B is applied to input 5 of AND 14A. This disables the output of AND 14A.

1-15. A2A6, Receiver Baud Counter PL-1140/G, Power On Functional Analysis

(fig. 1-8)

a. PWRC is applied to input terminal A2A6 P1-16. From here, PWRC is applied to input 7 of OR 4B. Output 10 of OR 4B goes high and is applied to the direct reset 8 (c) input of FF 14 (START PULSE DETECT), resetting it.

b. PWRC is also applied to input 3 of OR 4A. Output 2 of OR 4A is high and is applied to the direct reset input 8 (c) of flip-flops 25, 24, and 23 (which comprise the Mark Interval (Counter). The high level input clears the counter.

c. PWRC is also applied to input 4 of OR 22A, which operates with OR 22B as a flip-flop. Output 2 of OR 22A is low and is applied to input 7 or OR 22B. Input 8 of OR 22B is low because it is grounded. Input 9 of OR 22B is low because PWRC inhibits OR 3B. Output 10 of OR 22B goes high and is applied to input 5 of OR 22A, locking the flip-flop in this condition, even after PWRC is disabled. The high 10 output of OR 22B holds the various associated decoders disabled until a Start Pulse signal is detected.

d. PWRC is also applied to input 9 of OR 3B, which operates with OR 3A as a flip-flop. Output 10 of OR 3B goes low and is applied to input 5 of OR 3A. Input 4 of OR 3A is low because it is grounded. Input 3 of OR 3A is low since a START PULSE has not yet been detected. Output 2 of OR 3A is high and is applied to input 7 of OR 3B, locking the flip-flop in this condition. The high output 2 of OR 3A then enables the set and reset level inputs of the Baud Counter flip-flops; flip-flops 20, 19, 18 and 17.

1-16. A2A7, Timing Generator, PL-1143/G, Power-On Functional Analysis

(fig. 1-9)

a. When power is first applied, the high speed clock and timeout generator, transmit baud generator, and receive baud generator begin to run. The High Speed clock and timeout generator is used throughout the TCU to provide high speed pulses to sample incoming and outgoing data. It produces negative pulses at a frequency of approximately 8.0 kc. These pulses are in the order of 5 microseconds. This represents a time between pulse of approximately 135 microseconds. When potentiometer R25 is adjusted to approximately 9.85K, this adds to R26 to produce a total series resistance of approximately 13.5K. The time constant of R25, R26, and C21 is $RC=(13.5)(10^3)(.01)(10^{-6})=135$ microseconds. At this time (one time constant) the voltage across C21 is approximately 63% of the 9.3 volt supply or 4.7 volts which is sufficient to trigger unijunction Q10, which for a short time, produces a positive pulse. This is applied through Resistor R35 to the base of Transistor Q14, causing Q14 to conduct. The collector of Q14 which has been at +5 volts through resistor R36, is grounded through Q14 for a short time producing a negative going nominal 5-microsecond pulse. Once Q10 starts to conduct C21 discharges through Q10 and Resistor R28 to ground, turning off Q10 and starting the charging process over again. Thus, approximately every 135 microseconds the HSCL (High Speed Clock/Pulse) is produced for a short duration at a frequency of 8.0 kc.

b. The time Out generator provides a ¼ to ½ second time delay used by the Control Sequence Synchronizer. Each 135 microseconds Q10 conducts thus each 135 microseconds, a positive pulse is applied to the base of transistor Q11, through R29, causing it to conduct. During the nonconduction period of Q11, the +12 volts charge capacitors C22 and C23 through Diode CR8. The time constant for R30 and the capacitive combination of C22 and C23 is $(270)\frac{(.001)(5.6)}{(.001+5.6)}(10^{-6})=.001$ microfarads times 270 times $10^{-6}=.27$ microseconds. In approximately 5 time constants (1.35 microseconds) C22 and C23 build up to full charge. This is small compared to the allowable charging time (135 microseconds), thus C22 and C23 build up to full charge. The voltage built across series capacitors is in inverse proportions to the value of the capacitance thus C23 builds up to .0017 volt during this time. Each time that Q11 conducts the charge built across C22 is discharged through Diode CR7 and Q11 to ground, but because of the blocking action of Diode CR8, the charge on C23 is retained. The triggering voltage of unijunction Q12 occurs at approximately half of the source voltage, 12 volts, or about 6.0 volts. Each time that C22 and C23 charge (when Q11 is off), .0017 volt is added to C23. At this rate it takes approximately 3530 steps to build C23 to triggering voltage, thus the time delay circuit (R30, C22, and C23) divides by about 3530 to one. Since it requires 3530 steps to trigger Q12 and each step is approximately 135 microseconds, the total time required to trigger Q12 is 4765 (about 0.4) of a second; which is the basic time interval. Once Q12 fires it applies a short-duration positive pulse, through resistor R33 to the base of transistor Q13. When Q13 conducts, its collector is grounded (effectively) and provides the negative CSTP (Control Sequence Time Pulse). This lasts for a short duration and occurs about every 4/10 of a second. By adjustment of potentiometer R25, this time can be varied from approximately ¼ to ½ second. When Q12 is on, C23 discharges very quickly through resistor R32 to ground, and the charging process resumes.

c. The Receive baud generator provides positive and negative pulses to the receive baud counter at the rate of twice the baud data rate. Once power is applied to the TCU the receive baud generator starts to operate. The TCU can operate at one of three baud rates; 45.45, 74.2 or 75. If 45.45 baud is used potentiometer R37 and resistor R44 are used and are connected through input terminal A2A7P1-4 to +9.3 volts. If 74.2 or 75 baud are used, potentiometer R38 and resistor R43 are used and are connected through input terminal A2A7P1-5 to +9.3 volts and selection is made by adjustment of potentiometer R38. Potentiometer R39 and resistor R40 are not used but, in the future may provide an additional baud rate. Assume that 75 baud is being used and potentiometer R38 and resistor R43 are in the circuit. Since the baud rate is 75, the baud generator must operate at about 150 cycles per second. Thus pulses should be generated every 6.7 milliseconds. Potentiometer R38 is adjusted so that the firing voltage of the UNJ is reached every 6.7 milliseconds. Initially, when power is applied (before data is received) a mark (+5 volts) is present in the data lines which makes input terminal A2A7A1-11 SPDR (Start Pulse Detect Receive) low. This ground is applied through diode CR9 and resistor R41 to the base of transistor Q15, keeping it off. Thus capacitor C25 may charge. Once it reaches triggering voltage, unijunction Q16 conducts, applying a short duration positive pulse through resistor R47 to the base of Transistor Q17. As soon as Q16 conducts, C25 discharges through Q16 and Resistor R46 to ground. The positive output of Q16 is applied to the base of Q17. Q17 conducts, placing its collector effectively at ground. This is sent to output terminal A2A7 P1—37 as the negative BCRN (Bit Clock Receive Negative) pulse. Also, BCRN is applied to input 4 of OR 7A, whose output 2 goes high, providing the positive BCRP (Bit Clock Receive Positive) pulse. Also, BCRP is applied back through Diode CR10, and Resistor R41 to the base of Transistor Q15. Transistor Q15 conducts allowing C25 to discharge fully. Q16 now shuts off, turning off Q17, which inhibits OR gate 7A. The ground output of OR 7A shuts off Q15 allowing C25 to charge again. This oscillation continues. When the teletype line contains a start pulse, the SPDR (Start Pulse Receive) signal goes positive. This positive level is sent through Diode CR9 to the junction of R41 and C24. This causes a positive potential at the base of Q15, which causes Q15 to conduct. When Q15 conducts the charging operation of capacitor C25 is stopped and C25 is discharged. When SPDR is removed, the Receive Baud Generator continues its normal operation. This action synchronizes the baud counter with the teletype signals.

d. The TCU uses the Transmit Baud Generator to operate the Transmit Baud Counter at twice the baud rate. The Transmit Baud Generator operates identically to the Receive Baud Generator including selection of baud rates. Also all respective components have the identical value as those of the Receive Baud Generator, but with different reference designations.

1–17. A2A8, Transmit Baud Counter PL–1144/G, Power-On Functional Analysis

a. PWRC (fig. 1–18) is applied through A2A18–57 to CR3, generating SSPW. SSPW is applied through A2A8P1 (fig. 1–10) to input 3 of OR 15A, which operates with OR 15B as a flip-flop. Output 2 of OR 15A goes low and is applied to input 7 of OR 15B. Input 9 of OR 15B is low because it is grounded. Input 8 of OR 15B is low because Q6 conducts. When the Send Generate timer is not operating, output 10 of OR 15B goes high and is applied to input 4 of OR 15A; locking the flip-flop in this state even after PWRC becomes disabled. The high output from pin 10 of

OR 15B disables the set and reset level inputs of FF 23 via OR gate 24A.

b. SSPW (fig. 1-18) is also generated by the Start Stop Switch (SSSW) which is discussed later.

c. SSPW is also applied to the direct clear 8(C) inputs of flip-flops FF 5, 23, and 22, clearing these flip-flops. SSPW is also applied to input 3 of OR 3A. Output 2 of OR 3A goes low and is applied to pin 7 of OR 3B. DATI-2, a high pulse, is applied to input 9 of OR 1B. The low 10 output of OR 1B is applied to input 9 of OR 3B. OR 3B now has complete low coincidence and output 10 goes high and is applied to input 4 of OR 3A, locking the flip-flop in this state, even after SSPW disappears. SSPW is also applied to the reset 7(R) input of FF 2. With the first HSCL pulse (applied to the toggle 5(T) input of FF 2), FF 2 becomes reset.

1-18. A2A9, Transmit Cancel-Stop Sequence PL-1145/G, Power-On Functional Analysis

(fig. 1-11)

a. PWRC is applied to A2A9P1-16, and is then applied to the direct clear 8(C) input of flip-flop 12, which is the CNCL FLAG flip-flop; to clear it.

b. PWRC is also applied to input 3 of OR 11A, which operates with OR 11B as a flip-flop. Output 2 of OR 11A goes low and is applied to input 9 of OR 11B. Input 7 of OR 11B is low because it is grounded. Input 8 of OR 11B is low since Start Transmit is disabled. Output 10 of OR 11B is high and is applied through Resistor R3 to the base of Transistor Q1. Q1 conducts and provides a path to ground for the Control panel CANCEL SENT lamp; causing the lamp to light. The high output from pin 10 of OR 11B is also applied to input 4 of OR 11A, locking the flip-flop in this condition, even after PWRC is disabled. The low output from pin 2 of OR 11A disables CANN (Cancel Not Sent). The high output from pin 10 of OR 11B produces CANS (Cancel Sent), which makes the TCU appear as though it had just transmitted a cancel to the ADMS.

c. PWRC is also applied to input 5 of OR 3, which operates with OR 8B as a flip-flop. The output from pin 2 of OR 3 goes low and is applied to input 9 of OR 8B. Input 8 of OR 8B is low because it is grounded. Input 7 of OR 8B is low since the ACK received pulse is disabled. Output 10 of OR 8B goes high and is applied to input 4 of OR 3, locking the flip-flop in this condition even after PWRC becomes disabled. The low output from pin 2 of OR 3 is applied to input 3 of OR 8A. Inputs 4 and 5 of OR 8A are low since neither Repeat Alarm (REPA) nor End-of-Message Sent (EOMS) are enabled. The output from pin 2 of OR 8A goes high and is applied to the set level 4(s) input of flip-flop 12.

d. PWRC is also applied to the direct reset 8(c) input of flip-flop 14 (STOP COMMAND), resetting it.

e. PWRC is also applied to input 3 of OR 9A, which operates with OR 9B as a flip-flop. The output from pin 2 of OR 9A goes low and is applied to input 9 of OR 9B. Input 8 of OR 9B is low because SSTO is grounded. Input 7 of OR 9B is low because the TSTP signal is inhibited. The output from pin 10 of OR 9B goes high and is applied to input 4 of OR 9A, locking the flip-flop in this condition even after PWRC becomes disabled.

f. PWRC is also applied to the direct clear 8(c) input of flip-flop 13, clearing it and disabling the Stop flag signal (STPF).

1-19. A2A10, Transmit Repeat-Retransmit Sequence PL-1147/G, Power-On Functional Analysis

(fig. 1-12)

a. PWRC is applied to input terminal A2A10P1-23. From here, it is applied to the direct reset 8(c) inputs of flip-flops 18 and 13, resetting them. It is also applied to input 5 of OR 15A. Output 2 of OR 15A goes high and this high level applied to the direct reset 8(c) input of flip-flop 20, clearing it. Flip-flops 18, 13, and 20 are associated with the transmission of RT (retransmit).

b. PWRC is also applied to input 3 of OR 1A. Output 2 of OR 1A goes high and this high level is applied to input 5 of OR 6A. OR gate 6A operates with OR 6B as the Retransmit flip-flop. Output 2 of OR 6A goes low and this low level is applied to input 9 of OR 6B. Input 8 of OR 6B is low because it is grounded. Input 7 of OR 6B is low since Send RT pulse and Test RT sequence are disabled. Output 10 of OR 6B goes high and this high level is applied to input 4 of OR 6A, locking the RT flip-flop in this condition even after PWRC becomes disabled. The low output from pin 2 of OR 6A disables the set level input 4(s) of the RT FLAG flip-flop 18.

c. PWRC is also applied to the direct reset (c) input (pin 8) of flip-flop 24. The PWRC pulse clears flip-flop 24.

d. PWRC is also applied to input 5 of OR 2A. Output 2 of OR 2A is high and this high level is applied to the direct reset input 8(c) of flip-flops 23 and 22 (the Repeat Counter), clearing the Counter.

e. PWRC is also applied to input 8 of OR 9B. The output, 10 of OR 9B, goes high and is applied to input 3 of OR 16A, which operates with OR 16B as the Repeat (RP) flip-flop. Output 2 of OR 16A goes low and is applied to input 9 of OR 16B. Input 7 of OR 16B is low because the output 2 of AND 8A is disabled. AND gate 8A is disabled since PWRC disabled CANN. Input 8 of OR 16B is low because output 2 of 25A is low since EOMS and TREP are disabled. The high output of pin 10 is applied to input 4 of OR 16A, locking the flip-flop in this condition, even though PWRC becomes disabled. The low output from pin 2 of OR 16A is applied to input 5 of AND 21A, disabling the gate. Disabling AND 21A prevents the REP FLAG FF24, from being directly set except by CSSP (Control Seq. SYNC Pulse).

f. PWRC is also applied to input 4 of OR 9A. Output 2 of OR 9A goes high and this high level is applied to input 9 of OR 10B, which operates with OR 10A as the STOP Received flip-flop. The low output from pin 10 of OR 10B is applied to input 4 of OR 10A. Input 3 of OR 10A is low because it is grounded. Input 5 of OR 10A is low because the STOP receive pulse (STRP) is disabled. Output 2 of OR 10A goes high and this high level is applied to input 7 of OR 10B, locking the flip-flop in this condition, even after PWRC becomes disabled. The low output from pin 10 of OR 10B disables the STOP Received signal.

1-20. A2A11, Transmit Start-Acknowledge Sequence PL-1146/G, Power-On Functional Analysis

(fig. 1-13)

a. PWRC is applied through A2A11P1-25 to the direct reset 8 (c) inputs of flip-flops 25 and 17, START FLAG and ACK Flag Flip-Flops. This PWRC pulse clears this FF.

b. PWRC is also applied to input 4 of OR 6A. The high output, pin 2 of OR 6A, is applied to the direct reset 8 (c) input of flip-flop FF22 (Acknowledge). This PWRC pulse clears this flip-flop.

1-21. A2A13, Disconnect Line PL-1154/G, Power-On, Functional Analysis

(fig. 1-14)

PWRC is applied through A2A13P1-35 to input 9 of OR 21B, which operates with OR 21A as a flip-flop. Output 10 of OR 21B goes low and is applied to input 4 of OR 21A. Pin 5 of OR 21A is low because it is grounded. Input 3 of OR21A is low because the End-of-Message verified pulse is disabled. Output 2 of OR 21A goes high and is applied to input 7 of OR 21B, locking the flip-flop in this condition, even after PWRC becomes disabled. The high output, pin 2 of OR 21A, is applied through resistor R14 to the base of Transistor Q7. This makes the base positive with respect to the emitter and causes transistor Q7 to conduct. When transistor Q7 conducts its collector is placed at ground potential which disables DISC.

1-22. A2A14, Input Device Control PL-1152/G, Power-On Functional Analysis

(fig. 1-15)

a. PWRC is applied to input Terminal A2A14 P1-39. From here, it is applied to the reset level input 8 (c) of flip-flops 20, 21, 24 and 23. This PWRC pulse clears these flip-flops. The PWRC pulse is also applied to the direct set 3 (P) input of flip-flop 22. These flip-flops comprise the Control Sequence Synchronizer and these states represent the initial conditions at start of operation.

b. The Control Sequence Time Pulse (CSTP) is applied to input A2A14P1-58 from the high speed clock (para 1-16). The high-speed clock furnishes a pulse every ¼ to ½ second (assume that it is ¼ second). Every ¼ second, a pulse is applied to the pulse T (5) input of flip-flop 20. Its set 4 (s) and reset 7 (R) inputs are connected to +5 volts; thus, it becomes set. One-fourth second later CSTP arrives again, resetting flip-flop 20 and setting flip-flop 21 whose set 4 (s) and reset 7 (R) level inputs are connected to +5 volts, and whose pulse input is connected to the one (2) output of flip-flop 20. One-fourth second later flip-flop 20 is set and flip-flop 21 remains set (Count 11). One-fourth second later both flip-flops 20 and 21 are reset and the low one (2) output of flip-flop 21 which is applied to the pulse T (5) input of flip-flop and clears flip-flop. These three flip-flops continue to be toggled by the CSTP Pulse except when a flag is present. Any flag causes a "1" to be maintained at the set input(s) of FF20 preventing FF20 from changing states.

c. PWRC is also applied to the direct clear 8 (c) input of flip-flop 13 (CLUTCH CONTROL) and resets it.

d. PWRC is also applied to input 8 of OR 11B. The output, pin 10 of OR 11B, goes high and is applied to pin 4 of OR 11A. The output, pin 2 of OR 11A, goes high and this high level is applied to the direct clear 8 (c) input of flip-flops 9, 14, and 15 (N counter for transmitted messages) and clears this counter.

1-23. A2A15, Message Identifier Sequence Generator PL-1151/G Power-On Functional Analysis

(fig. 1-16)

a. PWRC is applied to input terminal A2A15 P1-50. From here it is applied to the direct reset 8 (c) input of flip-flop 12 (Message Numbering Flag) and resets it.

b. PWRC is also applied to input 9 of OR 11B. Output 10 of OR 11B goes high and this high level is the Message Numbering reset pulse, which initiates clearing of the message numbering operation.

1-24. A2A16, Message Identifier Decimal Counter PL-1150/G, Power-On Functional Analysis

(fig. 1-17)

PWRC is applied to input terminal A2A16P1-36. From here it is applied to input 4 of OR 23A, which operates with OR 23B as a flip-flop. Output 2 of OR 23A goes low and this low output is applied to input 9 of OR 23B. Input 7 of OR 23B is low because it is grounded. Input 8 of OR 23B is low provided the Control Panel Message Number Preset switch is disabled. The output, pin 10 of OR 23B, goes high and this high level is applied to pin 3 of OR 23A; locking the flip-flop in this condition, even after PWRC becomes disabled. The low output from pin 2 of OR 23A disables preselection of the transmit message number. The low output from pin 2 of OR 23A also prevents the message numbering counter from being cleared.

1-25. A2A18, Transmit Buffer Decoder PL-1148/G, Power-On Functional Analysis

(fig. 1-18)

a. PWRC is applied to input terminal A2A 18P1-57. From here, it is applied to the direct reset 8 (c) input of Transmit Buffer flip-flops 6, 11, 12, 7, 9, and 14 and clears them. PWRC is also applied to input 3 of OR 10A. Output 2 of OR 10A goes high and this high level is applied to the direct set 3 (P) input of flip-flop 15 (LINE DRIVER). This flip-flop contains the level ("1" or "0") that appears on the transmit line. PWRC is also applied to the direct reset 8 (c) input of FF3, resetting this flip-flop.

b. PWRC is also applied to diode CR3, producing SSPW, which is used to condition the logic as previously explained during time PWRC.

1-26. A2A19, Transmit Character Encoder PL-1156/G, Power-On Functional Analysis

(fig. 1-19)

PWRC is applied to input terminal A2A19P1-12. From here it is applied to input 7 of OR gates 2B, 7B, 12B, 17B, and 22B, each of which operate with their corresponding A half as flip-flops. The output, pin 10 of each of the above OR gates, goes low and is applied to input 4 of the corresponding A half of the OR gates. Input 3 of each A half is low because it is grounded. Input 5 of each A half is low because there is at this time no precedence character. Output 2 of each A half becomes high and is applied to input 9 of the corresponding B half, locking each flip-flop in this condition even when PWRC becomes disabled. The low output, pin 10, from each B half thus disables, for the time being, the precedence character logic.

1-27 A2A20, Enquiry Response Sequence Generator PL-1153/G, Power-On Functional Analysis

(fig. 1-20)

a. PWRC is applied to input terminal A2A20P1-21. From here it is applied to input 4 of OR 15A. Output 2 of OR 15A goes high and this high level is applied to the direct reset 8 (c) input of flip-flop 25 and clears it, to prevent advancing the Enquiry Counter at this time.

b. The output from pin 2 of OR 15A is also applied to input 5 of OR 20A, which operates with OR 20B as a flip-flop. Output 2 of OR 20A goes low and is applied to input 9 of OR 20B. Input 8 of OR 20B is low because it is grounded. Input 7 of OR 20B is low since ENQUIRY receive pulse is disabled. The high output 10 of OR 20B is applied to input 4 of OR 20A, locking the flip-flop in this condition, even after PWRC becomes disabled. The output from pin 2 of OR 20A, which is low, disables the set level input to flip-flop 25.

c. The low output from pin 2 of OR 20 is also applied to OR 19B pin 7. Pin 9 of OR 19B is low because it is ground. OR 19B's output (pin 10) goes high and is applied to the direct clear 8(C) input of flip-flops FF 21 and FF 22, resetting them. Pin 10 of OR 19B is also applied to pin 8 of OR 17B. The output (pin 10) of OR 17B goes high and is applied to the direct clear 8(C) input of flip-flops FF 24 and FF 23, resetting them, thus preventing at first special advancing of the ENQUIRY counter.

d. PWRC is also applied to input 9 of OR 14B, which operates with OR 14A as a flip-flop. Output 10 of OR 14B goes low and is applied to input 4 of OR 14A. Input 3 of OR 14A is low because it is grounded. Input 5 of OR 14A is low because OR gate 18A is inhibited by ERAD, normally a "1". Output 2 of OR 14A goes high and this high level is applied to input 8 of OR 14B; locking the flip-flop in this condition, even when PWRC becomes disabled. The high output, pin 2 of OR 14A, disables OR 19A, thus preventing OR 19A from producing a high input to the direct set 3(P) input of flip-flop FF 22.

Section IV. MESSAGE TRANSMISSION

Note: Refer to note preceding paragraph 1-10.

1-28. Transmission Start Detection, Idle State Functional Analysis

a. When power is applied to the TCU, the Transmit Baud Generator which is part of A2A7, Timing Generator, is running (fig. 1-9). The speed at which the Transmit Baud Generator is to operate is selected using the SPEED SEL switch. This selection is provided electrically by the application of +9.3 volts to input A2A7 P1-7 LBTE (Low Baud (45.45) Transmit Enable) or A2A7 P1-8 HBTE (High Baud (74.2 or 75) Transmit Enable). Application of primary power then starts the Transmit Baud Generator running at the selected speed. The Transmit Baud Counter operates at twice the selected baud frequency (i.e.) 90.9, 148.4, and 150 cps. It transmits both positive pulses (sent out of the Timing Generator at A2A7 P1-33) and negative pulses (sent out of the Timing Generator at A2A7 P1-34).

b. The Baud Counter (fig. 1-10), consisting of flip-flops FF17, FF18, and FF13, is counting from 1 through 8 as a result of pulses on the BCTP (Baud Clock Transmit Positive) lead. The BCTN (Baud Clock Transmit Negative) lead contains the same wave shape, but of the opposite polarity. The BCTP lead drives flip-flop FF8 which divides the repetition rate by two before the counter is driven. This causes the counter to shift at the same rate as the output teletypewriter baud rate.

c. The output of the counter is decoded by gates OR12B, OR12A, OR6, and OR7A. Refer to figure 1-26, which is a timing chart that shows the various outputs of the baud counter. Only counts 6, 7, and 8 are decoded. Also OR6 decodes count 6, but is inhibited until the output of FF8 and lead BCTN are coincident. This condition exists halfway between count 6 and count 7 and produces TSIL (Time Six Late). When OR 6 is enabled, its high output is applied to pin 7 of the START DETECTOR ENABLE flip-flop comprised of OR 4 (A and B).

d. The output, pin 10, of OR 4B (fig. 1-10) is sent to pin 7 of OR 1 partially enabling this gate which is monitoring the data-in line (DAT I-2). Also controlling this gate is the high speed clock (HSCL) pulse. The data line, during idle conditions, contains a mark which maintains an inhibit condition on OR 1B.

1-29. Generation of Cancel Following Power-On Functional Analysis

a. When the Transmit Baud Counter (fig. 1-10) enters the sixth count, which is actually binary 5 in the counter "101," a logical 0 at pin 9 of flip-flop 8; a low signal is applied to input 3 of OR 10A (from FF8), a low signal is applied to input 5 of OR 10A (from FF17), and a low pulse is applied to input 4 of OR 10A from the Timing Generator (BCTN) OR 10A now has complete input negative coincidence and its low output 2 is applied to input 8 of OR 12B. The input of OR 12B is low from FF18; input 9 of OR 12B is low from FF13. OR 12B now has complete low input coincidence and its output 10 is the TSIX (Time 6) pulse.

b. This TSIX pulse is applied as a high pulse to input 3 of AND gate 14A. When SSPW is applied to terminal A2A8 P1-17, it pulses input 3 of the SEND GENERATOR FF, which is comprised of OR 15 (A and B). This causes output 2 of OR 15A to go low. This low level is applied to input 7 of OR 15B. Input 8 (due to the recent PWRC signal) and input 9 (due to a ground) of OR 15B are low. This causes output 10 of OR 15B to be high, locking the flip-flop in this state. The high level from pin 10 of OR 15B is also applied to input 5 of AND 14A.

c. At the Transmit Cancel-Stop Sequence circuit A2A9 (fig. 1-11) PWRC is applied to terminal A2A9P1-16. From here, it resets the CNCL FLOP flip-flop consisting of OR gates 3 and 8B enabling OR 8A and presenting a high level to FF12's set (4) lead. Nothing happens at this time until the CSSP (Control Seq. Set Pulse) occurs. PWRC also resets the flip-flops comprised of OR 11 (A and B). Output 2 of OR 11A goes low, disabling CANN' (cancel not sent) and enabling CANS. Enabled CANS causes CNCL sent indicator to light. In this way it appears to the TCU that a Cancel has been sent. Output 10 of OR 11B generates a high level on the CANS lead. CANS is also applied through biasing Resistor R3 to the base of Transistor Q1. Transistor Q1 conducts, providing a ground path for the Control and Indicator Panel CANCEL XMITED Lamp, the other end of which is connected to +12 volts.

d. PWRC is also applied to input 5 of OR 3 which operates with OR 8B as the CANCEL flip-flop. Output 2 of OR 3 goes low and this low output is applied to input 9 of OR 8B. Input 8 of OR 8B is grounded. Input 7 of OR 8B is low because PWRC disabled the receive control sequence counter. Output 10 of OR 8B goes high and this high level is applied to input 4 of OR 3, locking the flip-flop in this condition. Also output 10 of OR 8B is applied to terminal 19 as CNFP (Cancel Flop). It is extended to (fig. 1-12) A2A10P1 terminal 14 and applied to input 8 of OR 15B. Output 10 of OR 15B is applied to terminal 47 as SRRC (Stop Received or 3-Repeat). SRRC is extended to (fig. 1-15) terminal 13 of A2A14P1 and prevents the TTY input device clutch from being generated during cancel. Inputs 5 and 4 respectively, of OR 8A are grounded. Output 2 of OR 8A goes high, however, no action occurs at this time.

e. The Control Sequence Synchronizer (fig. 1-15) consists of flip-flops 20, 21, 22, 24, 23, OR 18B and OR 4B. The purpose of the control sequence synchronizer is to synchronously set control sequence flags, of which FF 12 CANCEL (fig. 1-11) is one. The control sequence synchronizer (fig. 1-15) performs this task by producing a pulse, CSSP (Control Sequence Synchronizer Pulse), approximately every 2 to 4 seconds, depending on the particular TCU but always at T6L time. Note: this pulse is 100 msec long at 75 baud and 160 msec long at 45.45 baud. The CSSP pulses the trigger input of the Flag FF's and if the appropriate level conditions are present, the flip-flop is set; initiating transmission of that control sequence. Figure 1-27 is a timing chart showing the control sequence synchronization pulse (CSSP).

f. In the case of cancel (fig. 1-11) the level conditions are such that output 2 of OR 8A is high. When power is initially applied to the TCU, FF 22 (fig. 1-15) is set, and FF's 20, 21, 24 and 23 are reset conditioning the synchronizer to generate a CSSP at the first TSIL. Subsequent CSSP pulses are generated as described below. Timing Generator, A2A7 (fig. 1-9) Time Out Generator, has been adjusted to generate CSTP (Control Sequence Time Pulse) every ½ second. CSTP is applied to terminal A2A7P1-42 and sent through terminal A2A14P1-58 (fig. 1-15) to the pulse input of flip-flop FF20. FF20 divides this time by two; provided no FLAG signal exists; thus, every second the pulse input of FF21 is triggered. Since

FF21 divides by two, every 2 seconds the pulse input of FF22 is triggered. As long as message numbering is not in the process of being performed, MENR (Message Numbering Reset) signal is enabled (high). This enables the set and reset level inputs of FF22. Under these conditions, FF22 also divides by two, thus, its outputs switch every 2 seconds. Since FF22 goes to the set state every 4 seconds, it becomes reset and its one output goes low and is applied to the set level input of FF24. When the first TSIL arrives at A2A14P1-16 from the Transmit Baud Counter, FF24 becomes set. At this time FF23 is not affected and remains reset. The low zero output of FF24 is applied to input 8 of OR 18B. The low one output of FF23 is applied to input 7 of OR 18B. Output 10 of OR 18B goes high and starts a CSSP pulse. The next T6L pulse complements FF24 and FF23 terminating the CSSP pulse. Four seconds later FF24 becomes set, OR 18B is enabled and CSSP is generated again. Thus every 4 seconds a CSSP pulse is generated. Once conditions are met on one of the control flags (such as cancel), the FLGS signal is applied to terminal A2A14P1-10 and directly sets FF20. This locks the FF20 in this state as long as FLGS is present, inhibiting further generation of CSSP until FLGS becomes disabled. This is done to prevent new FLAG being set while any flag is set; thus precluding the possibility of garbling a control sequence. In this case (cancel), CSSP is applied to terminal A2A14P1-47 and extended through terminal A2A9P1-41 (fig. 1-11) to input 4 of OR 17A. Output 2 of OR 17A is applied to the pulse input of CANCEL FLAG FF12, setting this flip-flop.

g. The high one output (2) of FF12 is applied through A2A9P1-22 and A2A11P1-16 (fig. 1-13) as CNFG (Cancel Flag) and is applied to input 7 of OR 4B, which operates with OR 4A and OR 24B as one OR gate. Output 10 at OR 24B goes high and this high level is routed to A2A11P1-48 as the FLGS (Control Sequence Flag Set) level. CNFG is also applied through terminal 16 (fig. 1-13) to input 4 of FF10. This action extinguishes the MSTI (Message Transmitted Indicator).

h. FLGS is applied to the Transmit Baud Counter (fig. 1-10) at A2A8P1-21. This high level is applied to input 4 of AND gate 14A. AND gate 14A (at time) has complete input high coincidence and therefore generates a high output on pin 2. This high level is applied to the direct set P(3) input of flip-flop 23 and sets this flip-flop. This places FF 23 and 22 to a state of 10; flip-flop 23 set and 22 reset. (These FF's were cleared by PWRC.)

i. Since FF 23 is now set, output 2 of OR 25A is high. This high level is applied to input 9 of OR 24B. Output 10 of OR 24B is low and this low level is applied through biasing Resistor R8 to the base of Transistor Q4, which is part of a one second timer. When Q4 shuts off, the path to ground is removed for Resistors R9, R10, and R11 (pot) from the +12 volt source. The current through these resistors charges Capacitor C6. For a one second delay, pot R11 is adjusted so that the total series resistance of R9, R10, and R11 is about 15K ohms. This combined with the 70 μf capacitor C6 provides a time constant of 1 second. In one time constant, 1 second, approximately 63% of the 12-volt supply, about 7 volts, is placed across capacitor C6. This is sufficient to trigger the unijunction transistor Q5. When this occurs, the unijunction starts to conduct. This allows a negative signal to be applied through C7 to the base of Transistor Q6, turning it off. Thus the input 8 of OR 15B goes high. This timer (Send Generate) is used to generate the control leader, a 0.8-second mark level on the transmit line prior to the transmission of the two control characters. This sets FF OR 15, the SEND GENERATOR flip-flop. Output 10 of OR 15B goes low and this level is applied to input 3 of OR 24A. The low output 10 of OR 24B is applied to input 5 of OR 24A. OR 24A now has complete input low coincidence and becomes high at its 2 output, and this high level is applied to the set and reset level inputs of FF23.

j. At any count eight of the Baud Counter (111), flip-flops 8 and 17 cause OR 10A to be negatively enabled. This causes outputs 2 of OR 10A to go low. This low level and flip-flops 13 and 18 enable OR 12A. Output 2 of OR 12A thus produces TATE (Time 8 pulse). TATE is a high pulse and is applied to input 8 of OR 25B. Output 10 of OR 25B applies a high pulse to the pulse input (T) of FF23 (this always occurs at TATE). Since the level inputs of FF23 are enabled, TATE toggles FF23 to the reset state. The negative-going one output of FF23 toggles FF22 to the set state, since its level inputs are connected to +5 volts dc.

k. The low level from the one(2) output of FF23 is applied to input 8 of OR 21B. The low level from the zero (9) of FF22 is applied to input 9 of NOR 21B. While the baud counter is in the count TSIX following the switching of FF's 23 and 22, it is pulsed by BCTP at the next half baud count and goes into state 0011 which is count 6 Late (TSIL). OR 6 has complete negative input coincidence at this time and generates positive pulse at pin 2 TSIL (Time 6 Late).

l. The high TSIL pulse is applied to input 9 of OR 16B. Output 10 of OR 16B generates a low pulse which is sent to input 7 of OR 21B. OR 21B now has complete input negative coincidence, thus it generates a high pulse output at 10. This high pulse is sent to A2A8P1-34 as the high CC1P (Control Character 1 Pulse). Output 10 of OR 21B is also applied to input 4 of OR 16A. The output 2 of OR 16A is a low pulse which is CCLP (Control Character Load Pulse). CCLP is sent to A2A8P1-35.

m. The CCLP is applied to the A2A9 Card Transmit Cancel-Stop Sequence (fig. 1-11) at input terminal A2A9P1-8. From here the CCLP is applied to input 3 of OR 6A. Input 5 of OR 6A is low since it is applied from the zero (9) output of the CNCL FLAG 12 FF, which is set. Input 4 of OR 6A is low because it is grounded externally. OR 6A now has complete input low coincidence and thus produces a high output at terminal 2. This high output is routed to output terminal A2A9P1-39 as the LCNL (Load Cancel) pulse. It is routed from here to input terminal A2A19P1-17 of the character store Encoder (fig. 1-19) where it is applied to input 7 of OR 9B. The high output pin 10 of OR 9B, is applied to input 9 of OR 8B. The high output from pin 10 of OR 8B is applied through output terminal A2A19P1-14 as the LDB4 (Load Data Buffer 4) level.

n. The high level on input terminal A2A19P1-17 is also applied to input 5 of OR 15A. The output 2 of OR 15A is high and is applied to input 9 of OR 15B. Output 10 of OR 15B is applied to input 9 of OR 19B. The high output of OR 19B is sent to output terminal A2A19P1-22 as the LDB1 (Load Data Buffer 1) level.

o. Both LDB1 and LDB4 are high and are routed to the TRANSMIT BUFFER DECODER (fig. 1-18). There levels are applied respectively to input terminals A2A18P1-22 and 13. They in turn are placed respectively, into stages Bit 4 and Bit 1 of the Transmit Buffer, which is comprised of flip-flops 6 (Character Bit 5), 11 (Character Bit 4), 12 (Character Bit 3), 7 (Character Bit 2), 9 (Character Bit 1), 14 (Start Bit), and 15 (Line Driver, Rest period).

1-30. Shifting Cancel Out, Functional Analysis

a. During the previous PWRC transition, all FF's of the Transmit Buffer Decoder were cleared by way of their direct reset inputs C(8), and FF15, the Line Driver (which contains the rest interval MARK) was set via its direct set input P(3) from output 2 of OR 10A.

b. The fact that flip-flops FF11 and 9 are set applies high levels to input 9 of OR 2B and thus to input 3 of OR 2A and to input 5 of OR 2A. Output 2 of OR 2A is high and is the BFRL (Buffer Loaded) level. Note that when one or more of flip-flops (6, 11, 12, 7, or 9) contains a one, the buffer is filled with a specific character.

c. The BFRL Level is applied out of the Transmit Buffer-Decoder on output terminal A2A18P1-7, to input terminal A2A8P1-20 of the Transmit Baud Counter (fig. 1-10) partially enabling AND 9A.

d. On the A2A9 circuit (fig. 1-11) the CNCL SENT FF (OR 11) is set, causing output 10 of OR 11 to be high. This is applied to terminal 9 as CANS (cancel sent) and extended to input A2A14P1-11 (fig. 1-15). This is applied to input 9 of OR 3B. Output 10 of OR 3B is high and is applied to input 3 of OR 2A. Output 2 of OR 2A is low and is applied to input 3 of OR 8A. Output 2 of OR 8A is high, is applied to terminal 23 as HALT and is extended to circuit A2A8P1-19 (fig. 1-10). This is applied to input 8 of AND 14B. FF5 is set by SHTE on its direct clear INPUT 3(P) during time seven of the baud count and its high one (2) output is applied to input 7 of AND 14B.

c. At Count 8 (TATE) of the Baud Counter, a high pulse is applied to input 9 of AND 14B. AND 14B now has complete high input coincidence, its output 10 goes high and sets the SHIFT ENABLE flip-flop, FF2, by way of its direct set P(3) input. The low level from the zero (9) output of the SHIFT ENABLE flip-flop, FF2, is applied to input 9 of OR 7B. At the next transition to zero of FF8, a negative input is applied to input 7 of OR 7B. Each BCTN applies a negative pulse to input 8 of OR 7B. Complete low input coincidence is now present on OR 7B; the resulting output 10 is a high pulse produced at the baud rate, because FF8 will be set only once during the baud count. Therefore, each time FF8 is reset and a BCTN pulse occurs output 10 of OR 7B produces a high pulse which is SFTP (shift pulse). SFTP is routed out of the Transmit Baud Counter on terminal A2A8P1-11.

f. The SFTP enters the Transmit Buffer-Decoder (fig. 1-18) on input terminal A2A18 P1-35. It is applied to the pulse input (T) of flip-flops 6 and 11, and by way of OR 8A to flip-flops 12, 7, 9, 14, and 15. Beginning with FF6 (which contains bit 5 of the character, in this case a zero), the "one" output of each FF is connected to the reset level input of the succeeding flip-flop, and the "zero" output of each FF is connected to the reset level input of the succeeding flip-flop. As each shift pulse (SFTP) is applied, therefore, each flip-flop is loaded with the condition of the previous stage. As this occurs, the character is shifted serially from the the "one" output of flip-flop 15 (LINE DRIVER) by way of OR 10B, to the line at TTLT (Transmit Teletype) on output A2A18P1-24.

g. With each SFTP a zero is loaded into FF 6 (Bit 5 of the character) due to the fact that CONN on input 4 of AND 4A is low. During shifting of the first control character zeroes are propagated through the buffer, clearing it so that the second character may be loaded into the cleared register.

h. For zeroes to be propagated as described above, the reset level input 7(R) of FF6 must be high, and the set level input of FF6 must be low. On Circuit A2A8 (fig. 1-10), once generation of a control sequence (such as cancel) is started, flip-flops 23 and 22 leave state 00. This causes output 2 of OR 25A to be high and output 10 of OR 24 to be low, disabling CONN (Control Character Not Sent). CCNN is applied to terminal 56 and sent to A2A18 (fig. 1-18) terminal 20. This is applied to input 4 of AND 4A. Output 2 of AND 4A goes low and this low output is applied to input 7 of OR 8B. Inputs 8 and 9 of OR 8B are grounded. Output 10 of OR 8B is low and this low level is applied to the set level input (4) of FF6, and to input 8 of OR 1B. Input 7 and 9 of OR 1B are grounded. Output 10 of OR 1B is high and this high level is applied to the reset level input 7(R) of FF6. This satisfies the input requirements of FF6.

i. The cancel control-character consists of two contiguous D's. The loading and shifting out of character 01001 (D) represents one half of the control character thus, one more is required. T six late (TSIL) provides the pulse (CCLP) which loads the character into the Transmit Buffer (fig. 1-11). At time eight (TATE), shifting begins. This represents one and one half baud times between loading and shifting. This results in a minimum rest interval of 1½ baud times between characters.

j. At the next time 6 (TSIX) of the Band Counter (fig. 1-10), following the time 8 during which shifting began, OR 12B is enabled and its 10 output is TSIX (high). TSIX is applied to SHIFT ENABLE flip-flop FF2 on the direct reset 8(C) input and clears it; disabling shifting. At the TATE, which started shifting, the pulse input of FF23 is triggered. The level inputs of FF23 are still enabled. FF23 becomes complemented to the set state and FF22 retains its set state. The low level from the zero output of FF23 is applied to input 5 of OR 21A. The low level from the zero output of FF22 is applied to input 4 of OR 21A. When time 6 late (TSIL) is generated by the baud counter, a low pulse is applied to input 3 of OR 21A. Output 2 of OR 21A generates a high pulse which is applied to output terminal A2A8P1-33 as CC2P (Control Character 2 pulse). From here CC2P is applied to the Transmit Cancel-Stop Sequence circuits (fig. 1-11) on input terminal A2A9P1-56. Since the CNCL FLAG FF12 has been set, the high LCNL pulse produced by the second CCLP pulse is routed back to input 3 of AND 18A. At the same time CC2P is applied to input 4 of AND 18A. Output 2 of AND 18A is a high pulse which is applied to input 3 of OR 17A. Output 2 of OR 17A is a high pulse, which is applied to the trigger T(5) input of the CNCL FLAG flip-flops FF12. The Reset level input 7 (R) of FF12 is permanently connected to +5 V. Thus FF12 becomes reset, disabling the cancel flag. This signifies the completion of transmission of the initial cancel control sequence to the distant station.

k. At TATE, during which the shifting of the second cancel character is started, FF23 (fig. 1-10) is pulsed. This clears FF's 23 and 22. This causes output 2 of OR 25A to be low and output 10 of OR 24B to be high. This resets the SEND GENERATE TIMER by turning on Q4. Also the high output 10 of OR 24B is applied to input 9 of AND 9B. At the following TSIL a high pulse applied to input 8 of AND 9B, enables this gate. Output 10 of AND 9B resets the SEND GENERATE FF (OR 15), disabling OR 24A and preventing subsequent advancement of FF 23 and 22 until the next control character is ready to be transmitted.

1-31. Reply to Cancel After Power-On Functional Analysis

a. When the TCU sends a cancel after power turn-on, the distant station replies with ACK2. The receive portion of the TCU generates an ATRP (Acknowledge To Receive Pulse) at the Receiver Control Sequences A2A3. ATRP is applied to input terminal A2A9P1-13 of the TRANSMIT CANCEL-STOP SEQUENCE (fig. 1-11). It is applied to input 7 of OR 8B which operates with OR 3 as the CNCL (Cancel) FF. Output 10 of OR 8B becomes low, and this low level is applied to input 4 of OR 3. Input 7 of OR 3 is low because TCAN (Test Cancel Sequence) is not being used. Input 8 of OR 3 is low because IAKR (Incorrect Ack Received) is presumably disabled (correct Ack response is assumed). Input 9 of OR 3 is low because CAMA (Cancel Message Switch, Manual Operation) is currently not being used. Input 5 of OR 3 is low because PWRC is disabled. Input 3 of OR 3 is low because RTRP (Request Retransmission Pulse) in normal operation, will be disabled. OR 3 now has complete low coincidence; thus its 2 output is high. This is applied to input 3 of OR 8B whose output 2 is low. (The high output 2 of OR 3 is applied back to input 9 of NOR 8B, locking the FF in this state even after the ATRP pulse becomes disabled.)

b. The low output 2 of OR 8A is applied to the set 4 (s) level input of the CNCL FLAG 12 flip-flop. This prevents CNCL FLAG from becoming set again by the next CSSP, thus concluding the cancel transmission operation.

1-32. Verification of Initial and Subsequent ACK Responses, Functional Analysis

a. Once power is applied to the TCU, a CANCEL is sent to the distant station which responds, in normal operation, with an ACK2 signal. From this point, ACK alternates while the TCU is ON LINE for any one period. That is, when the first message (following power turn on) is sent by the TCU, the distant station must respond with an ACK-1, the second message with an ACK-2, the third message with an ACK-1 and so on, alternately. This is checked by the TCU as described in the following subparagraphs.

b. When ATRP is generated following the initial ACK2 received, ATRP is applied to input terminal A2A11P1-10 of The Transmit Start-Acknowledge Sequence (fig. 1-13) as a high pulse. It is applied to input 7 of OR 11B. The output 10 of OR 11B is high and applied to input 3 of AND 12A. Recall that during the transmission by the TCU of the CANCEL control sequence, a signal LCNL was generated (para. 1-291) which loaded the cancel character into the Transmit Buffer Register. This was applied also through input terminal A2A11P1-18 and directly reset FF23, the ACK TOGGLE flip-flop, which is the state of FF23 at this point in time. The high zero (9) output of FF23 is applied to input 5 of AND 12A. AND 12A now has complete high input coincidence, thus its output 2 is high. This is applied to input 3 of OR 13A. The 2 output of OR 13A is high and is applied out of the circuit as the ACKV (Ack verified) pulse. The high output 2 of OR 13A is also applied to input 4 of OR 15A, forcing the output (pin 2) to a low level.

c. At this time the TCU transmission path remains idle until the START XMIT Switch on the Control and Indicator Panel is operated. It is possible that an alarm may sound at this time (Transmit End of Message) however, this can be ignored.

d. After the first message is transmitted, an EOM (End-of-Message) sent signal is transmitted. The eventual response by the ADMS to this (following a transmitted Repeat by the TCU) is ACK1. When EOM is generated (it is a high signal), NEOM (End of Message not sent) becomes low. This is applied to input terminal A2A11P1-12 and is applied to the pulse T (5) input of FF23 (ACK TOGGLE flip-flop). The set level input, pin 4, and the reset level input, pin 7, of FF23 are enabled since LNCL is now disabled, thus the NEOM level sets FF23. The high output from pin 2 of FF23 is applied to input 9 of AND 12B. The ACK-1 receive control sequence is culminated in application of AORP (Ack 1 receive pulse), a high pulse, from the Receive Control Sequence circuit to input terminal A2A11 P1-11. AORP is applied to input 5 of OR 11A. Output 2 of OR 11A goes high and this high level is applied to input 7 of AND 12B; enabling the gate. Output 10 of AND 12B goes high and this high level is applied to input 5 of OR 13A. The high output from OR 13A is the ACKV (Ack verified) pulse.

e. Observe that when receiving an ACK response, AORP should be received when FF23 is set and ATRP should be received when FF23 is reset. If either of the other two combinations are present ($\text{AORP}\cdot\overline{\text{FF23}}+\text{ATRP}\cdot\text{FF23}$), the correct ACK response has not been received. This is checked as follows:

f. The high ATRP signal is applied from OR 11B to input 7 of OR 13B. The high AORP signal is applied from OR 11A to input 8 of OR 13B. Either of these places a high pulse on input 9 of AND 19B. If an incorrect ACK is received, neither AND 12A or AND 12B will have high complete input coincidence. This results in low outputs from pin 2 of AND 12A and from pin 10 of AND 12B which are applied, respectively, to inputs 3 and 5 of OR 13A. This produces a low output from 2 of OR 13A which will disable ACKV (ACK verified). The low 2 output, of OR 13A is applied to input 4 of OR 15A.

g. The high output from pin 2 of OR 15A is applied to input 8 of AND 14B. AND 14B now has complete input high coincidence; thus its output 10 is high. This is routed out of output terminal A2A11P1-53 as the high IAKR (Incorrect ACK received) signal.

h. IAKR (which is also the condition ACK not verified) is applied as a high pulse through A2A9 P1-44+0 input 8 of OR 3 (fig. 1-11). This sets the CNCL FLOP flip-flop, comprised of OR 3 and B, and enables the CNCL FLAG flip-flop FF12's set level input 4. At the next CSSP, FF12 is set, and a second cancel is generated.

i. When the first cancel was generated, LNCL (load cancel) was produced. This was applied to input terminal A2A10P1-52 (fig. 1-12), and from there to input 8 of OR 25B. Output 10 of OR 25B went high and was applied to the set 4 (s) and reset 7 (R) level input of FF23, which with FF22, comprises the Repeat timer. (The Repeat Timer was cleared by PWRC.) At CC2P (of the first cancel) a one was loaded, into FF23. During a second cancel a two is loaded into FF's 23 and 22. If, after the second cancel is sent, ACK-2 is still not received, a third attempt is made. If the third attempt is not successful, flip-flop's 23 and 22 are placed in count 3 (11). At this point the high one (2) output of flip-flops 23 and 22 are applied, respectively, to inputs 7 and 8 of AND 21B. Output 10 of AND 21B goes high and this high level is sent out as REPA (repeat alarm). This prevents the automatic generation of subsequent cancels. REPA is applied through a resistor R4 to the base of transistor Q3. This causes transistor Q3 to conduct, shunting the high resistance of R5 and allowing a ground path by which the Control and Indicator panel ALARM lamp is illuminated. At this point for continued operation, manual intervention is required.

j. When the Control Panel START XMIT switch operated after a 3RPT alarm, input terminal A2A10P1-13 goes high and is applied to input 3 of OR 3A (SSPW=SSSW+PWRC). Output 2 of OR 3A goes high and this high level is applied to input 3 of OR 2A. Output 2 of OR 2A goes high and clears the repeat counter (REP COUNT) through the direct reset input 8 (C) of flip-flop FF23 and 22. This disables REPA. The disabling of REPA causes input 4 of OR 8A (fig. 1-11) to return to a low level. Assume EOMS is still low on input 5 of OR 8A. IARK applied to pin 8 of OR 3 left output 2 of OR 3 low, which is applied to input 3 of OR 8A. Output 2 of OR 8A enables the set level input 4 (S) of FF12. When CSSP is generated, FF12 is set, initiating the ultimate transmission of three more cancels. If ACK-2 is still not received, other arrangements must be made between the TCU and ADMS to correct the problem.

1–33. Introduction to Message Numbering Functional Analysis

a. Once the TCU has transmitted the CANCEL control sequence, and has received the ACK–2 reply from the ADMS, data messages can be transmitted. If message numbering has not been disabled from the Control Indicator Panel, a Transmission identifier precedes the message body. This is as follows:

XX VZCZC CALL LTRS (FIGS) MESS# (LTRS) 2CR LF PRECED

(Control
Sequence)
The intelligence (body) and End of Message (NNNN) then follow.

Note. The above format is the JANAP 128 format; ACP 127 format is similar except there is no 2CR LF. A TCU uses either JANAP 128 or ACP 127. The logic at each site is wired to generate the required format of the particular site.

b. At every TATE generation of the Transmit Baud Counter (fig. 1–10), CLEP (Clutch Enable Pulse) is applied to output terminal 58. CLEP (fig. 1–15) is applied through input terminal A2A14P1–45 to input 8 of AND 12B, on the Input Device Control. Flip-flop FF 17 was reset by SSPW during PWRC time. The high output from pin 9 is sent to pin 7 of AND 12B. This partially enables AND 12B. The low 2 output of FF 17 is applied to pin 5 of OR 2A. Input 4 of OR 2A is low since EOMS (End of Message Sent) is currently disabled. Neither PCDS (Precedence Character Detected and Stored) MNEG (Message numbering flag), FLGS (Flags of a transmit control sequence), SRRC (Stop control sequence Received), nor ABNI–1 (Abnormal Input TTY Device) are present. However, CANS is high since the CANCEL has just been sent and acknowledged, at this point.

c. When the START XMIT switch is operated at the Control Indicator panel (fig. 1–3), a +5 volt potential (SSSW) is sent through A1–J1–29. The SSSW signal enters A2A9P1–11 (fig. 1–11) and is sent to pin 8 of OR 11B, which operates with OR 11A as a flip-flop. This flip-flop was set by the PWRC lead at Power turn on and is now reset. This removes the CANS condition at OR 3B (fig. 1–15) resulting in a complete enable condition at AND 12B, input 9.

d. With the arrival of CLEP, AND 12B has complete high input coincidence. Thus its output 10 is high and sets the FF13 (CONTROL CLUTCH) from its direct set (4) input. The high one (2) output of FF13 is applied to output terminal 36 as CLUP (clutched picked). The high output 10 of AND 12B is also applied to output terminal 9 as PCCP (Precedence Character Clear Pulse).

e. PCCP is applied to input pin 39 of the A2A19 circuit (fig. 1–19), Transmit Character Encoder. From here it is applied to input 8 of OR gates 2B, 7B, 12B, 17B, and 22B. This clears a buffer comprised of 5 OR gates, the function of which is to store a precedence character. Observe that during initialization, PWRC also clears this buffer.

f. CLUP is applied to Control Indicator Panel, A1J3 terminal 47 to terminal 44 on S6, MODE SWITCH, Section 3 (fig. 1–3). The TCU is in the NORMAL operating mode, so, through the switch CLUP, is routed to terminal 6 of the switch to output terminal 58 as CLUP. From here, CLUP is applied to circuit A2A7 (fig. 1–9) Timing Generator, terminal 17. This is the input of the Clutch Transmitter which converts CLUP from +5 or 0 volts used within the TCU logic to +6, −6 volts, used in the TTY input device. The output of the Clutch Transmitter (positive 6 volts) is CLUG which is applied from output terminal 20 to the TTY input device. If the clutch signal is disabled (zero), a ground is applied through Resistor R11 to the base of Transistor Q4. This shuts off Q4 placing a positive voltage from the +12 volt supply through R13 at the junction of CR5 and R15. The −12 volts through Resistor R14 CR5 places a negative voltage at the junction of CR5, R14, and R16. The effect is that the positive voltage at the collector of Q4 breaks down to zener diode. The base of Transistor Q6 (an NPN) becomes positive with respect to the emitter through R16. This causes Q6 to conduct, placing the −6.2 volts (through R17) across CLUG (a zero). Also the +12 volts is applied to Transistor Q5 through R13 and R15 making Q5 (a PNP) base positive with respect to the emitter. This shuts off Q5. If a one is to be transmitted, +5 volts is applied through R11 to the base of Q4, causing Q4 to conduct. The collector of Q4 is thus grounded and this ground is applied through R15 to the base of Q5, a PNP transistor. Transistor Q5 conducts and +6.2 volts is applied through R17 as CLUG. Also −12 volts is applied through R14 and R16 to the base of Q6, because CR5 does not conduct making the base negative with respect to the emitter, (which is connected to −6.2 volts). Q6 is thus shut off. These levels, which leave at CLUG terminal 20 and CLUG TR terminal 50 are applied to Logic Card A2A1, (fig. 1-21), Transmit Line Filter Driver. CLUG is applied to terminal 44 and CLUG TR is applied to terminal 43. CLUG is then applied to the input of an emitter follower, the purpose of which is to provide drive, and reduce noise. The emitter follower output is then applied to terminal 9 and extended through the Control Indicator Panel (A1J4 pins 16 and 17) to the T & R filter. From here the CLUP and CLUP TR (return) signals are applied to the TTY input device. Once CLUP-2 (one) is applied to the TTY device, the TTY starts to operate, and sends characters to the TCU Transmit Buffer (fig. 1-18). These characters enter the Transmit Buffer by way of the T-R filter and the Control and Indicator Panel MODE selector switch. They are converted by the Transmit Buffer from +6 and −6 to +5 and ground by the receiver consisting of Q1 and Q2, and associated components. When a "one" is being transmitted, +6 volts is applied to terminal 26 as DATI-1. This is applied through R1 to CR1 and to the base of Q1, causing Q1 to conduct. This applies ground to the base of Q2 through CR2, shutting off Q2. This applies +5 volts through R3 to input 3 of AND 4A. When the buffer is not being zeroed and a control sequence is not being sent, the set level input of FF6 is enabled through OR 8B. When shifting begins, a "one" is loaded into FF6. Application of −6 volts to terminal 26 loads a "zero" into FF6 by shutting off Q1 and turning on Q2. At this time, characters are sent by the TTY input device, but, until a precedence character is received by the TCU, the message transmission does not actually begin. During reception by the TCU of these characters, which may consist of extraneous information and also during reception of the TCU by the precedence character (when it first enters), the distant station is blinded from receiving data. This is done because the distant station has no use for extraneous information and because, as shown in the message format (para 1-33*a*), the precedence character is not the first character to be received by the distant station. The distant station is blinded at this time from receiving characters as described in the following paragraph.

g. On those TCU's equipped with enquiry logic for use with the AUTOVON capability, there is additional logic. This includes circuit A2A20 Enquiry Response Sequence Generator (fig. 1-20). During PWRC, FF25 is reset by way of OR 15A. Until the TCU is requested to send its AUTO VON routing indicator FF25 remains reset. The high zero output of FF25 is routed to terminal 5, ENQF and extended to terminal 53 of circuit A2A18 (fig. 1-18). From here it is applied to input 9 of AND 4B. (On TCU's not equipped with AUTOVON interface logic, input 9 of AND 4B is open which logically is equivalent to a one.) On circuit A2A8, Transmit Baud Counter (fig. 1-10), the SEND GENERATOR flip-flop (OR 15A and B) is presently reset (assuming there are no control sequences being transmitted at this time). This causes a high SGDN level to be routed to terminal 49 and extended to terminal 50 of A2A18 (fig. 1-18). From here SGDN is applied to input 7 of AND 4B. On circuit A2A9 (fig. 1-11), SSPW during PWRC has reset the flip-flop consisting of OR 10 (A and B) since a precedence character from the TTY input device has not yet been detected and stored. FF OR 10 is still reset. This causes output 10 of OR 10B to be high and it is sent to output terminal 24 as BLFF (Blind Flip-Flop). It is extended from here to input A2A18P1-48 (fig. 1-18) and applied to input 8 of AND 4B. This completely enables AND 4B, whose output 10 goes high. This high level is applied to input 7 of OR 10B. Thus, when characters are sent to the TCU from the TTY device before the message actually begins, output 10 of OR 10B (TTLT) is held at a +5 volts (steady mark), even though these characters are being shifted out of the Transmit Buffer.

1-34. Precedence Characters Functional Analysis

a. Certain characters are called precedence characters. These are V, Z, O, P, R, Y, and **W.** One of these is transmitted to the TCU Transmit Buffer (fig. 1-18) from the TTY input device to signify that transmission of a message from the TTY device, through the TCU, to the ADMS, is about to begin. Once the TCU decodes a precedence character, it knows that a message is about to be transmitted, and prepares the TCU accordingly. A Precedence Character is the first character of a message received by the TCU. The TCU then stores it, sends the Transmission identifier, and does not actually send this character to the distant station until the transmission identifier has been sent. Then the precedence character precedes the first character of the message intelligence.

b. The EOM character N, when sent by the TTY four times contiguously, signifies that the message is finished. The 4 N's follow the last character of the message intelligence and when the TCU receives and decodes 4 N's consecutively it reacts accordingly to prepare for termination of the message.

c. When the Transmit Buffer is filled with a character (the START bit is shifted into FF14 of the Transmit Buffer), detection for precedence characters is performed by seven OR gates (16, 17, 18, 19, 20, 24, 23) and a 5-input OR gate (22), each of which detect for a particular precedence character. As an example, detection of the letter Z is described. Letter Z in the five bit ITA-2 code is 10001. The low zero (9) output of Bit 5, FF6 (which contains a one), is applied to input 10 of OR 17. The low one (2) output of Bit 4 FF11 (which contains a zero) is applied to input 7 of OR 17. The low one (2) output of Bit 3 FF12 (which contains a zero) is applied to input 5 of OR 17. The low one (2) output of Bit 2 FF7 (which contains a zero) is applied to input 3 of OR 17. The low zero (9) output of Bit 1 FF9 (which contains a one) is applied to input 4 of OR 17. Input 8 and 9 of OR 17 is grounded. OR 17 now has complete input negative coincidence; thus it produces a high output at 2. This is applied to input 10 of OR 21. Output 2 of OR 21 is low and is applied to input 5 of OR 1A. This partially enables OR 1A.

d. On circuit A2A9 (fig. 1-11), FF OR 10, reset during PWRC applies a low level to input 8 of OR 17B. On circuit A2A8 (fig. 1-10), the low SGDS (send generate set) level is applied to terminal 23, and extended through A2A9 (fig. 1-11) terminal 55 to input 9 of OR 17B. On circuit A2A20 (fig. 1-20) ENQS, disabled when the AUTOVON identifier is not being transmitted by the TCU, is applied as a low level ENQS to terminal 25, and extended through terminal 6 (fig. 1-11), to input 7 of OR 17B. OR 17B is negatively enabled and its low 10 output is applied to terminal 23 as PCDD (Precedence Character Detector Disabled). From here it is extended through A2A18P1 terminal 46 of (fig. 1-18) to input 4 of OR 1A. During the generation of TSIL (time six late), a low pulse TSLN (fig. 1-10), is generated at output 10 of OR 16B and applied to terminal 39. From here it is extended through A2A18P1 terminal 5 (fig. 1-18) to input 3 of OR 1A. Output 2 of OR 1A is a high pulse which enables the set (4) input of FF3, and which is applied to terminal 6 as PCDP (Precedence Character Detected Pulse). PCDP is extended to A2A9P1 (fig. 1-11) terminal 40 to input 7 of OR 4B. Output 10 of OR 4B is a high pulse which is applied to terminal 49 as PCFT (Precedence Character Flop Toggle). From here PCFT is extended to A2A18P1 terminal 43 (fig. 1-18) to the pulse input of FF3. Since the set input is enabled, the trailing edge of PCFT sets FF3, causing it to produce PCDS (Precedence Character Detected and Stored) at terminal 45.

e. As described above, when the precedence character arrives, it is shifted into the TCU Transmit Buffer and is detected by the decoder (fig. 1-18) and results in the generation of PCDP and PCDS. The precedence character is saved by extending the high (2) outputs of the Transmit Buffer flip-flops to output terminals A2A18P1-51, -17, -18, -14, and -11 for bits 1 through 5. These are applied, (fig. 1-19) to input terminals A2A19P1-33, -34, -5, -35 and -38 of the character store-encoder. From here each high level is applied, respectively to input 3 of AND's 21A, 16A, 11A, 6A, and 1A. PCDP (Precedence Character Detected Pulse) is applied on input terminal A2A19P1-36 and to input 4 of these AND gates. Where ones exist, the output of the AND (2) is high and applied to input 5 of an associated OR pair (2A, 2B), (7A, 7B), (12A, 12B), (17A, 17B), and (22A, 22B) which operate as five storage flip-flops that store the precedence character. Ones place the respective flip-flops in a condition where their output (pin 2 in each case) is low. All flip-flops were previously in the opposite state (output 10 low) due to the PCCP (Precedence Character Clear Pulse) and originally due to PWRC.

f. Once the precedence character is received by the TCU, the TTY input device must be inhibited from transmitting data while the TCU prepares the message header, which is not generated from the TTY device, but by the TCU logic. This has already been done. Before the precedence character is detected by the TCU, FF3 (fig. 1–18) is reset. The high reset output of FF3 is sent to terminal A2A18P1-15 as PCDN (Precedence Character Detected Not), and is extended through A2A14P1 terminal 8 (fig. 1–15) to input 3 of AND 12A. The high BLFF (Blind FF) level is extended from terminal 24 of A2A9P1 (fig. 1–11), through terminal 7 (fig. 1–15) to input 4 of AND 12A. Output 2 of AND 12A is high and this high level is sent to terminal 18 as CPDR (Clutch Precedence Drop). From here CPDR is extended through A2A19P1 terminal 52 (fig. 1–19) to input 3 of OR 19A. Output 2 of OR 19A goes high and is applied to terminal 37 as CLRE (Clutch Reset Enable). From here it is extended through A2A14P1 terminal 52 (fig. 1–15) to the reset level input of FF13 (CLUTCH CONTROL). As soon as any character, sent from the TTY device is detected by the TCU, SPDT (Start Pulse Detect Transmit) is generated (fig. 1–10); the generation of SPDT is described logically in paragraph 1–28. SPDT is applied to terminal 18 and extended through A2A14P1 terminal 17 (fig. 1–15) to the pulse input of FF13. Recall that at every time 8 of the Transmit Baud Counter, the CONTROL CLUTCH FF13 was set; pulling the clutch and starting the TTY device, provided certain conditions had been met. As soon as any character from the TTY device is detected by the TCU (SPDT), including the precedence character, the TTY clutch is disabled by the resetting of FF13. The nature of the TTY device is such that, although CLUP is disabled during SPDT, the device continues to operate until it has sent the entire character to the TCU, then it stops.

g. Once the precedence character is detected and stored the reset input of FF13 is disabled since CLRE (produced as a result of PCDN) is disabled. The clutch is prohibited however from being set again until the TCU has sent the start of message. PCDS is extended from A2A18P1 terminal 45 (fig. 1–18) through A2A14P1 terminal 49 (fig. 1–15) to input 7 of OR 3B. This results in the disabling of AND 12B. so that FF13 cannot be set, although CLUP is generated.

h. The first phase of the transmit message header is START (II), or any control sequence. When the precedence character was first detected by the TRANSMIT BUFFER, PCDP (Precedence Character Detected Pulse) high pulse was generated. This is applied to the Transmit Start-Acknowledge sequence circuit (fig. 1–13) through input terminal A2A11P1–24 and is applied to input 7 of OR 9B. Output 10 of OR 9B goes high and is applied to the direct set (P) input 3 of the START FLAG flip-flop FF25; setting it. As mentioned above, the first phase of the message header is any Control Sequence. If no other control sequence is being generated at this time, START will be generated, otherwise the control sequence being generated will take the place of START, and START will not be generated. Assume below that START is to be generated. Flip-flop FF25 had been previously cleared by application of primary power (PWRC). Since FF25 is now set, the low zero (9) output of FF25 is applied to input 3 of OR 8A. Input 9 of OR 8 is presumably low since an ACK control sequence is not being generated. Inputs 4, 5, 7, 8 of OR 8 are low presumably since none of the following control sequences are being generated: Cancel, Stop, Retransmit or Repeat. Input 10 of OR 8 is the CCLP (Control Character Load Pulse) which, when generated, will provide a low pulse to OR 8.

i. The low CCLP pulse (fig. 1–10) is the output of OR 16A of the Transmit Baud Counter. CC1P is produced at the time 6 Late (TSIL) of the Transmit Baud Counter provided that FLGS is enabled, which is true if the START Flag (fig. 1–13) has been set, the TTY input device is not abnormal, and a STOP has not been received. These conditions enable AND 19A causing its high output 2 to be applied to input 7 of OR 24B, the output of which is FLGS. The role of FLGS and other logic (fig. 1–10) contributing to the generation of CC1P and CC2P for Control Sequences is described logically in the section of Generation of Cancel. CCLP generated at TSIL (Time 6 Late) is sent out of circuit A2A8 on output terminal A2A8P1–35 (fig. 1–10). It is applied to the Transmit Start-Acknowledge Sequence Circuit (fig. 1–13) through input terminal A2A11P1–41 to input 10 of OR 8A. OR 8A now has complete low input coincidence and its output 2 is a high pulse which is routed out of this circuit on output terminal A2A11P1-17 as LSTT (Load Start). LSTT is applied through input terminal A2A19P1-48 to input 4 of OR 9A, on the character store Encoder (fig. 1-19). The high output 2 of OR 9A is applied to input 9 of OR 13B. The high output 10 of OR 13B is applied to output terminal A2A19P1-41 as LDB3 (Load Data Bit 3). LSTT is applied also to input 5 of OR 14A, the high 2 output of which is applied to input 3 of OR 13A. The high output (pin 2) of OR 13A is applied out of this logic card on output terminal A2A19P1-40 as LDB2 (Load Data Bit 2). LDB3 and LDB2 are applied to input terminals A2A18P-10 and -12, respectively, of the Transmit Buffer-Decoder (fig. 1-18). LDB3 and LDB2 load the Transmit Buffer. Once the buffer is loaded, the buffer filled condition is detected (fig. 1-10) and shifting begins. After the first I (half of start) is shifted out, CC2P (Control Character 2 Pulse) is produced.

j. At the next TSIL (T six late) of the Transmit Baud Counter, CCLP is again generated, this time by, and in coincidence with CC2P. CC2P again loads an I (second half of start) into the Transmit Buffer Register as described above, shifting starts, and the second I of the START sequence is shifted out.

k. CC2P is also applied to input terminal A2A11P1-51 of the Transmit Start-Acknowledge Sequence (fig. 1-13), and is applied to the toggle input (T) of START FLAG flip-flop FF25. The reset level input is connected permanently to +5 volts; thus, FF25 is reset terminating the START control sequence and CC2P also resets the START FF (OR 20A and B).

l. The CC2P (a high pulse) is also applied to input 4 of OR 18A. Output 2 of OR 18A goes high and this high level is applied through terminal A2A11P1-47 as SMFG (Set Message Numbering Flag). From this point, it is applied to the Message Identifier-Sequence Generator (fig. 1-16) on input terminal A2A15P1-14, and to the toggle (T) input 5 of FF12, preparing it for setting.

m. Observe that any control sequence could produce SMFG because SMFG occurs during CC2P which occurs during every control sequence transmission. Also CC2P resets the START flip-flop so that START will not be transmitted if any other control sequence is transmitted.

1-35. Generation of Message Header, VZCZC Functional Analysis

a. The next portion of the message header to be generated, following START (or any control sequence), is VZCZC. When PCDP (Precedence Character Detected Pulse) was generated during transmission of the precedence character by the input TTY device, PCDP was applied through input terminal A2A16P1-14 (fig. 1-17) to input 3 of OR 3A as a high pulse. OR 3A operates with OR 3B as a flip-flop. Output 2 of OR 3A goes low and is applied to input 7 of OR 3B. Input 8 of OR 3B is low due since presumably the Control and Indicator Panel MEND (Message numbering disable switch) is off. Input 9 of OR 3B is low since the MNRP (Message Numbering Routine Complete) is disabled. This causes output 10 of OR 3B to be high. This is applied to input 5 of OR 3A locking the flip-flop in this state even after PCDP expires. The high output 10 of OR 3B is sent on output terminal A2A16P1-15 as MNFP (Message Numbering FF set).

b. MNFP is applied to the Message Identifier Sequence Generator (fig. 1-16) on input terminal A2A15P1-21, and to the set level input 4 (5) of FF12, enabling it. Thus when SMFG arrives, as described previously, FF12 becomes set.

c. The high one (2) output of FF12 is sent to output terminal A2A15P1-53 as MNFG (Message Numbering Flag). MNFG is applied to input terminal A2A17P1-57 of the Message Identifier Binary-Baud of logic (fig. 1-22) and to input 3 of AND 5A. Input 4 of AND 5A is high when a control sequence is *not* in process. Input Time T6 (TSIX) from the Transmit Baud counter is applied through input terminal A2A17P1-17 and is applied to input 5 of AND 5A. Each time TSIX is generated, output 2 of AND 5A becomes high and is applied via output terminal A2A17P1-19 as the high MENE (Message Number Enable) Pulse.

d. MENE is applied to the Message Identifier-Sequence Generator (fig. 1-16) on input terminal A2A15P1-33 to input 3 of OR 11A. Output 2 of OR 11A goes high and this high level is applied to the pin 5 (T) input of FF16. FF16 is the first stage of a four stage binary counter (FF-16, -21, -22, and -23), which provides the count for each character of the message header. The counter is in a reset condition.

e. When MENE enters, it is also applied to input 3 of OR 17A. The output of OR 17A is low and is applied to input 5 of OR 25A. Input 4 of OR 25A is low from the low one (2) output of FF22. Input 3 of OR 25A is low from the low one (2) output of FF23. Since OR 25A has complete input low coincidence output 2 is low and this low level is applied to input 8 of OR 14B. Input 9 of OR 14B is low from the low one (2) output of FF21. Input 7 of OR 14B is low from the low one (2) output of FF16. OR 14B now has complete input coincidence and its 10 output is a high pulse LOND-O (Load Number Device O). This is applied through output terminal A2A15P1-25 and input terminal A2A17P1-52 (fig. 1-22) to four places:

(1) Input 4 of OR 15A. The high 2 output of OR 15A is applied to input 3 of OR 10A. The high 2 output of OR 10A is applied to output terminal A2A17P1-23 as TSNI-5 (Transmit Shift Number Input 5).

(2) Input 7 of OR 10B. The high output 10 of OR 10B is applied to output terminal A2A17P1-24 as the TSNI-4 signal.

(3) Input 5 of OR 9A. The high 2 output of OR 9A is applied to output terminal A2A17P1-14 as the TSNI-3 signal.

(4) Input 7 of OR 9B. The high 10 output of OR 9B is applied to output terminal A2A17P1-15 as the TSNI-2 signal.

f. TSNI-5, -4, -3, and -2 are sent, respectively, to input terminal A2A19P1-19, -15, -47, and -50 of the character store-encoder (fig. 1-19). They are decoded by OR 4B, 8A, 9B, 8B, 9A, 13B, 14B, 14A, 13A, 19B, 15A and 15B and results in LDB-5, -4, -3, and -2 are high while LDB 1 is low. LDB 5, 4, 3, and 2 are applied to the transmit Buffer-Decoder (fig. 1-18) and are loaded into the Transmit Buffer Bits 5, 4, 3, and 2 to represent V, the first character of the message header sequence.

g. The remaining characters of the message header (ZCZC) are generated as the counter is stepped. They are generated in the same manner except the decoding of the counter outputs are different. However, the following similar steps are performed.

(1) The message counter and the decoder (fig. 1-16) determine the decoded LOND pulse.

(2) The LOND pulse is applied to the encoder (fig. 1-21) which generates the TSNI(s) signal.

(3) The TSNI pulses are applied to the character Store-Encoder (fig. 1-19) which generates the LDB level(s).

(4) The LDB signals load the Transmit Buffer (fig. 1-18) with the appropriate character.

(5) The character is shifted out to the lines.

h. Each application of MENE (fig. 1-16) steps the message counter by one, during each generation of TSIX. Observe that the counter is advanced during the trailing edge of the pulse. After V has been decoded, the Message counter enters count 1000. This is decoded as LOND-1 which when decoded as described in subparagraph g (1) through (5) above, generates character Z, the second message header character. Observe that in decoding LOND-1 the state of FF21 is not essential since character Z must also be generated at count 3 which, except for FF21, is identical to count 1 (1100), (1000). Once the Message counter enters count 2 (0100), the decoding networks described above generate character C (LOND-2) which is the third message character generated. At count 3, another Z is generated by LOND-1 which is the fourth message header character. At count 4, another C is generated by LOND-4 which is the fifth message header character. The message counts generated at this time are as follows:

(1) Count 0 (0000): LOND-0=V
(2) Count 1 (1000): LOND-1=Z
(3) Count 2 (0100): LOND-2=C
(4) Count 3 (1100): LOND-1=Z
(5) Count 4 (0010): LOND-4=C

1-36. Generation of Message Header Channel Designator Functional Analysis

The next three message header characters generated are the particular call letters of a site. These are wired-in on assembly A2A17 and are the call letters for the TCU. The next three message counts (i.e., 5, 6, and 7) produce LOND 5, 6, and 7. LOND 5, 6 and 7 are extended on output terminals A2A15P1-52, -22, and -23 to the Message Identifier, Binary-Baudot circuit (fig. 1-22) on input terminals A2A17P1-21, -22 and -25. LOND-5 is applied to terminal 1; LOND-6 to terminal 2; and

LOND-7 to terminal 3 all located on A2A17. Terminal 3 is strapped as required to terminals numbered 31, 32, 33, 34, 35. Terminal 2 is strapped as required to terminals numbered 21, 22, 23, 24, 25. Terminal 1 is strapped as required to terminals numbered 11, 12, 13, 14 and 15. As LOND-5, 6, and 7 are generated they enable the three call letters, peculiar to a particular site. The message counter (fig. 1-16) has proceeded to count 7 as follows:

Count 5 (1010): LOND-5
Count 6 (0110): LOND-6
Count 7 (1110): LOND-7

1-37. Generation of Message Header Figures Functional Analysis

The next message header character to be transmitted is figures. This controls a change from the letters mode of the receiving TTY device (at the ADMS) to the figures mode in preparation for the message number which will follow. Count 8 of the message counter (0001) produces LOND-8. The various decoding described previously ultimately loads the Transmit Buffer with binary 11011 which is the switch to figure character. This is shifted out to the distant station.

1-38. Generation of Message Number Functional Analysis

The following three message header characters generated are the three digit message number. The operator has certain capabilities which he can employ regarding message numbering: He may allow the message number to increase by one from the previous message; he may preset the message number to 000 and start over; or he may assign whichever number he wishes to a particular message. A message numbering counter is located on the Message Identifier Decimal Counter logic circuit (fig. 1-17). This is comprised of flip-flops numbers FF-2, -6, -11, -21, -22, -4, -5, -9, -10, -15, and -20.

b. The message number counter is not a simple 12 stage counter. but rather three 4-stage decimal counters. The counter output is decoded decimally from 000 to 999 and back to 000, providing a decimal count of 1000 maximum. The least significant decimal digit (LSD) (0-9) is produced by FF-2, -6, -11, and -16. The second digit is produced by FF-21, -22, -4, and -5. The most significant digit (MSD) is produced by FF-9, -10, -15 and -20. The decimal count is normal; that is the LSD advances from 0 to 9. When it advances back to zero the middle digit advances to one. Each complete count of the LSD advances the middle digit one count. When it advances back to zero, the MSD advances to 1 and each complete count of the middle digit advances the MSD one count. When the MSD advances from 9 to 0 the entire 3 digits are cleared. The following shows the counting of FF-2, -6, -11, and -16 from 0000 to 1001. The other two groups of four operate similarly and are not described in detail.

c. Assume that FF-2, -6, -11, and -16 are all in the zero state. When a message is successfully sent by the TCU, an EMVP-1 (End-of-Message-Verified Pulse) is applied to input terminal A2A16P1-40. Assume that prior to EMVP-1 the count is 000. EMVP-1 is applied as decimal count 001 to the pulse input 5 (T) of FF2, the least significant bit of the least significant decimal digit. The set 4(S) and reset 7(R) level inputs of FF2 are connected to +5 volts; thus FF2 becomes set (1000). When EMVP-1 arrives again, after successful completion of the second message as decimal count 002, FF2 is reset. FF6 whose pulse input T (5) is connected to the one (2) output of FF2, becomes set since the high zero (9) output of FF16 is connected back to FF6's set 4(s) and reset 7(R) inputs (0100). At decimal count 003, FF2 becomes set and since its one (2) output goes high FF6 remains set (1100). At decimal count 004, FF2 becomes reset. FF6 now becomes reset since the one(2) output of FF2 goes low. FF11 is connected to +5 volts at its set 4(S) and reset 7(R) inputs and since the one (2) output of FF6 (to which the T (5) input of FF11 is connected) goes low, FF11 becomes set (0010). At decimal count 005, FF2 becomes set and since its one (2) output goes high, FF6 remains reset. Since FF6 remains reset, FF11 remains set (1010). At decimal count 006, FF2 becomes reset and since its one (2) output goes low, FF6 becomes set. Since FF6 one (2) output goes high, FF11 remains set (0110). At decimal count 007, FF2 becomes set. Since its one (2) output goes high, FF6 remains set. Since FF6 remains set, FF11 remains set (1110). At decimal count 8, FF2 becomes reset. Since flip-flop FF6's one (2) output goes low, FF11 becomes reset. The low zero (9) output of FF6 during count 1110 is applied to input 8 of

OR 13B. The low zero (9) output of FF11 during count 1110 is applied to input 9 of OR 13B. Input 7 of OR 13B is low since it is grounded. OR 13B is thus high at output 10 which is applied to the set 4 (s) level input of FF16. When FF2 becomes low at its one (2) output at decimal count 008, it sets FF16 by triggering the pulse 5 (T) input of FF16 (0001). At decimal count 009, FF2 becomes set. Since its one (2) output goes high FF6 remains reset. Since FF6 remains reset, FF11 remains reset. Since the one (2) output of FF2 goes high, FF16 remains set (1001). At decimal count 010, FF2 becomes reset. The low zero (9) output of FF16 is connected to the set 4 (s) and reset 7 (R) level inputs of FF6; thus FF6 remains reset. Since FF6 remains reset, FF11 remains reset. When FF2 becomes reset, its one (2) output goes low and is applied to the trigger T 5 (T) input of FF16. An advance has thus been propagated to stages FF-21, -22, FF16 becomes reset (0000). However, when the one (2) output of FF16 goes low FF21 becomes set since its set 4 (s) level input and reset 7(R) level inputs are connected to +5 volts and since the one (2) output of FF16 is connected to the pulse 5 (T) input of FF21. An advance has thus been propagated to stages FF-21, -22, -4 and -5. These, and FF-9, -10, -15 and -20 operate similarly to the stages described above. The middle four stages use OR 13A as their gating logic and the last four stages use OR 25A as their gating logic.

d. The number contained in the message numbering counter must be converted to the ITA-2 baud of code for transmission to the distant station. The message number is transmitted in three steps if each digit of the message number is one character.

e. When the message counter (fig. 1-16) was in condition 8 (0001), LOND-8 was produced for the previous character. At message count 9 (1001), the low zero (9) output of FF23 is applied to input 3 of OR 13A. The low level (2) output of FF22 is applied to input 4 of OR 13A. Input 5 of OR 13A is grounded. The 2 output of OR 13A becomes low and is applied to input 4 of OR 20A. The low zero (9) output of FF16 is applied to input 3 of OR 20A. The low (2) output of FF21 is applied to input 5 of OR 20A. Output 2 of OR 20A becomes high and is applied on output terminal A2A15P1-59 as DEMN-9 (Decode Message Number 9) signal.

f. DEMN-9 is applied through input terminal A2A16P1-19 (fig. 1-17) to inputs 4 of AND 14A, 7 of AND 14B, 3 of AND 24A, and 7 of AND 24B. Input 5 of AND 14A is from the one (2) output of Message numbering Counter FF9. Input 8 of AND 14B is from the one (2) output of FF10. Input 4 of AND 24A is from the one (2) output of FF15. Input 9 of AND 24B is from the one (2) output of FF20. This means that at this time (DEMN-9) ANDs 14 and 24 decode the most significant digit. Where a one exists in the four FF's the output of the corresponding AND is high. OR's 8 and 19 provide common decoding for the three digits (at three times 9, 10 and 11). Output 2 of AND 14A is applied to input 4 of OR 8A. Output 10 of AND 14B is applied to input 9 of OR 8B. Output 2 of AND 24A is applied to input 5 of OR 19A. Output 10 of AND 24B is applied to input 8 of OR 19B. Output 2 of OR 8A is extended to output terminal A2A16P1-42; 10 of OR 8B, to A2A16P1-48; 2 of OR 19A, A2A16P1-53; and 10 of OR 19B to A2A16P1-54.

g. These outputs are applied, respectively, to input terminals A2A17P1-11, -9, -7, and -6 (fig. 1-22) as MDEA (Message Number Decode A), MDEB, MDEC, and MDED. In this circuit, the numbers are converted from BCD to decimal then encoded to ITA-2. Assuming that the MSD is BCD 6 (binary 0110); MDEA is low, MDEB and MDEC are high and MDED is low. Decoding is accomplished as follows:

(1) The input 7 of OR 1B is high; thus its 10 output is low.

(2) Input 3 of OR 2A is low and since inputs 4 and 5 are grounded, output 2 is high.

(3) Input 9 of OR 2B is high; thus its 10 output is low.

(4) Since output 10 of OR 2B is low, output 10 of OR 8B is low (output 10 of OR 2B is applied to input 8 of OR 8B and input 7 of OR 8B is grounded).

(5) Input 7 of OR 4B is high; thus its output 10 is low.

(6) Input 9 of OR 3B is high; thus its output 10 is low.

(7) Input 3 or OR 3A is low; thus, since inputs 4 and 5 are grounded, its output 2 is high.

(8) Input 5 of OR 1A is low. Input 3 of OR 1A is grounded (low). Input 4 of OR 1A is low since it is connected to output 10 of OR 3B, which is low. Thus, output 2 of OR 1A is high.

(9) The result of (1) places low levels on inputs 7 of AND 11B, 3 of AND 11A, 7 of AND 6B, and 5 of AND 6A. Thus, outputs 2 of AND 6A, 10 of AND 6B, 2 of AND 11A and 10 of AND 11B are low.

(10) The result of (4) places low levels on inputs 9 of AND 7B, 4 of AND 17A, and 9 of AND 17B. Thus outputs 10 of AND 7B, 2 of AND 17A, and 10 of AND 17B are low.

(11) The result of (3) places a low level on input 4 of AND 7A. Thus, output 2 of AND 7A is low.

(12) Since input 3 of OR 2A is low, input 9 of AND 12B is low. Thus, output 10 of AND 12B is low.

(13) The result of (8) places a high level on input 3 of AND 12A. The results of (2) above places a high level on input 4 of AND 12A. Input 9 of OR 2B is high; thus input 5 of AND 12A is high. The result of this is that output 2 of AND 12A is high. (Observe that this AND is the only one in this situation with a high output.)

(14) Since output 2 of AND 12A is high, output 2 of OR 21 is low.

(15) Since output 2 of AND 12A is high, output 10 of OR 18B is high. Thus output 2 of OR 23A is low.

(16) As a result of the low outputs from the AND gates, inputs 4, 5, 8, 7, and 9 of OR 16 are low. Input 10 of OR 16 is low due to the presence of a ground.

(17) As a result of the low outputs from the AND's, inputs 5, 4, 9, 8, and 7 of OR 22 are low. Input 10 of OR 22 is low due to the presence of a ground.

(18) As a result of the low outputs from the AND's, inputs 7, 8, and 9 of OR 13B are low. Output 10 of OR 13B is thus low, and is applied to input 9 of OR 23B. Input 7 of OR 23B is low since output 10 of AND 11B is low.

h. ORS 16, 22 and 23B now have complete input low coincidence except for their respective 3, 3, and 8 inputs. DEMN-11 is produced (fig. 1-17) and a high level is applied to input 8 of OR 20B. Its output 10 goes low and this low level is applied to input 8 of OR 25B. Input 9 of OR 25B is grounded. At Transmit Baud Counter Time 6, an inverted (low) TSXN (Time Six Negative) pulse is applied to input 7 of OR 25B. Output 10 of OR 25B goes low and is extended as ALMN (Allow Message Numbering) on output terminal A2A15 P1-57. (Observe that at TSIX the presence of either DEMN-9, -10, or -11 produces ALMN Allow Message Numbering). ALMN is applied through input terminal A2A17P1-5 (fig. 1-22) to inputs 3 of OR 16, 3 of OR 22, and 8 of OR 23B. These three ORs have input low coincidence causing their respective 2, 2 and 10 outputs to go high.

(1) The high output 2 of OR 16 is applied to input 5 of OR 24A. Output 2 of OR 24A is applied to input 3 of OR 8A. The high output 2 of OR 8A is the TSNI-1 (Transmit Shift input 1) signal.

(2) The high output 2 of OR 22 is applied to input 5 of OR 25A. Output 2 of OR 25A is high and is applied to input 3 of OR 9A. Output 2 of OR 9A is high and is the TSNI-3 signal.

(3) The high 10 output of OR 23B is applied to input 5 of OR 15A. The high 2 output of OR 15A is applied to input 3 of OR 10A. The high output from pin 2 of OR 10A is the TSNI-5 signal.

(4) TSNI-2 and -4 are disabled and are thus low. This produces a 5 bit code of 10101 which in the figures made of the ITA-2 baud of code is number 6, as had been assumed.

i. Number 6 is loaded into the Transmit Buffer and shifted out to the distant station. At DEMN-10 the second digit of the decimal message number is transferred out to the ADMS, and at DEMN-11 the third (LSD) digit is transmitted to the ADMS.

1-39. Generation of Message Header Letters Functional Analysis

When the four-stage message counter (fig. 1-16) advances to count 12, a shift to letters is generated. The next portion of the message header to be transmitted is either: the precedence letter or character (for ACP-127) or 2 carriage returns and a Line feed (for JAN 128). When the message counter advances to count 12, OR 4A decodes this condition and output 2 of OR 4A generates the high LOND-12 pulse (Load Number Device (12)). LOND-12 is in turn decoded (fig. 1-22) as all TSNI's are one. The TSNI's are in turn eventually loaded into the Transmit Buffer and the Letters character is shifted out to the ADMS.

1-40. Generation of CR, CR, LF Functional Analysis

a. The message counter (fig. 1-16) advances to state 13. When the TCU is wired to operate in the JAN-128 mode, 2 Carriage Returns and a Line Feed (in that order) follow the shift to letters. In this case the zero (9) output of FF16 is strapped to input 8 of OR 18B and the zero (9) output of FF21 is strapped to input 9 of OR 18B. When the Message counter is in state 13, the low one (2) output of FF21 is applied to input 8 of OR 4B. The low zero (9) output of FF16 is applied to input 7 of OR 4B. The low zero (9) output of FF23 is applied to input 5 of OR 24A. The low zero (9) output of FF22 is applied to input 4 of OR 24A. When the MENE pulse arrives (at Baud Count Time 6), a low pulse is applied to input 3 of OR 24A. Output 2 of OR 24A is low and is applied to input 9 of OR 4B. Output 10 of OR 4B goes high and is the LOND-13 pulse. This selects TSNI-4 which ultimately loads the Carriage Return character into the transmit Buffer and shifts it out to the ADMS.

b. At count 14 (0111) of the message counter, LOND-14 is generated. LOND-14 selects TSNI-4 and ultimately shifts out another carriage return character to the line.

c. At Count 15 (1111) of the message counter, LOND-15 is decoded and selects TSNI-2. This ultimately shifts out the line feed message header character to the receiving ADMS.

1-41. Function of JAN-128 or ACP-127, Functional Analysis

a. Each TCU is wired for either JAN-128 or ACP-127 by strapping on assembly A2A15. The message counter output is monitored by these straps to determine whether CR, CR, LF is generated or not. The message header can end at count 12 or count 15 depending on the straps used. Once the message counter reaches the selected count, the low output of FF16 is applied to input 8 of OR 18B, through the selected patch. The low output of FF21 is applied to input 9 of OR 18B, through the selected patch. Input 7 of OR 18B is grounded. Output 10 of OR 18B goes low and is applied to input 5 of OR 18A. The low zero (a) output of FF22 is applied to input 3 of OR 18A. The low zero (9) output of FF23 is applied to input 4 of OR 18A. The output 2 of OR 18A is low and is applied to input 7 of OR 17B. Input 9 of OR 17B is grounded (low). At Time T6 late of the Transmit Baud counter (following the time 6 which placed the counter to count 12 or 15), the TSLN (Time Six Late not) pulse is low and is applied through input terminal A2A15P1-51 to pin 8 of OR 17B. Output 10 of OR 17B goes high and this high level is applied to input 8 of OR 11B. Output 10 of OR 11B goes high and this high level is extended on output terminal A2A15P1-41 as the MNRP (Message Numbering routine complete) pulse.

b. MNRP is extended through terminal A2A16 P1-17 (fig. 1-17) to input 9 of the flip-flop comprised of OR 3A and 3B. This flip-flop, which has been set since the beginning of the Message header transmission routine is now reset and output 10 of OR 3B goes low, disabling the MNFP (Message Number flip-flop) signal. Output 2 of OR 3A goes high and generates the MNFN (Message Numbering Flag Not) pulse at A2A16P1-45.

c. The low MNFP, is applied through terminal A2A4P1-52 (fig. 1-6) to input 4 of OR 5A. FF12 (fig. 1-16) is still set at this point. Its low zero (9) output is applied through output terminal A2A15 P1-20, input terminal A2A4P1-53 (fig. 1-6), to input 3 of OR 5A. At time six of the baud count following transmission of Line Feed (JAN-128 mode) or shift to Letters (ACP-127 mode) the low TSXN (time six not) pulse is applied to input 5 of OR 5A. Output 2 of OR 5A is a high pulse and is extended to output terminal A2A4P1-54 as the TIFR (Transmission Identifier Flag reset) pulse. TIFR is applied through input terminal A2A11P1-23 of the Transmit Start-Acknowledge Sequence circuit (fig. 1-13) to input 5 of OR 18A. Output 2 of OR 18A goes high and is extended to output terminal A2A11P1-47 as the SMFG (Set message numbering flag) signal.

d. SMFG is applied to input terminal A2A15 P1-14 (fig. 1-16) to pulse the message numbering flag flip-flop FF12. When MNFP was disabled by FF OR 3A and 3B (*b* above), MNFN (message numbering flag not) was enabled/and extended through A2A16P1-45 (fig. 1-17) and input terminal A2A15P1-43 (fig. 1-16) to the reset level 7 (R) input of FF12. SMFG resets FF12 and the low one (2) output extended to output terminal A2A15P1-53 as MNFG. MNFG is applied to two places:

(1) First it is applied through A2A16P1-26 (fig. 1-17) input 9 of OR 25B. Input 7 of OR 25B is low since it is grounded. Input 8 of OR 25B is low since the flip-flop comprised of OR's 3A and 3B has been reset. The high output 10 of OR 25B is applied through output terminal A2 A16P1-56 as the MECR (Message Counter reset) signal to put terminal A2A15 P1-34 (fig. 1-16) to the direct reset inputs 8(c) of the message counter FF's (16, 21, 22, 23) clearing the counter.

(2) The low MNFG signal is also applied to input terminal A2A17P1-57 (fig. 1-22). This low level disables AND5A, thus disabling MENE (Message Counter Enable) and stopping the counting of the message counter.

e. As described above, MNFP and MNFG are disabled and are both low. MNFP (low) is applied to terminal 15 (fig. 1-17) and extended to terminal 54 of circuit A2A6 (fig. 1-8), and to input 3 of OR 15A. MNFG is applied to terminal 53 (fig. 1-16) and extended to terminal 53 (fig. 1-8) to input 4 of OR 15A. Output 2 of OR 15A is low and is applied as TIRE (Trans. Iden. reset Enable) to terminal 56 and extended through terminal 42 of A2A14 (fig. 1-15) to input 8 of OR 2B. Input 7 of OR 2B is low when Message Numbering is not disabled. Output 10 of OR2B is high and is applied to terminal 41 as TITE (Transmission Identifier Transfer Enable) and through terminal 52 of Circuit A2A5, Output Device Control (fig. 1-7), to input 7 of AND 4B. Input 9 of AND 4B is high due to PCDS. At the Time 6 of the Transmit Baud Counter following the Time 6 when MNFG was disabled, a high pulse is applied to input 8 of AND 4B. Output 10 of AND 4B is a high pulse and is applied to terminal 49 as MEPT (Precedence Character Transfer with Message numbering enabled). MEPT is extended through terminal 9 (fig. 1-13) to input 9 of OR 18B. Output 10 of OR 18B is a high pulse, PCTP (Precedence Character Transfer Pulse) on terminal 42. If message numbering has been disabled from the control Indicator Panel, the precedence character of the message is sent out just after the control sequence is transmitted. In this case there is no transmission identifier. After the precedence character is transmitted, the message body follows and whatever is stored on the tape of the TTY input device is sent out as part of the message body. When the control sequence A2A17 (fig. 1-22) is not in progress, CONN is applied as a high signal to input 8 of AND 5B. The MEND from the Control Indicator Panel enters this circuit on terminal 55 and is applied as a high input 7 of AND 5B. At the time 6 following the CC2P of the control sequence, AND 5B is enabled (TSIX is applied to input 9), and its 10 output is MDPT (Message Numbering Disable Precedence Character Transfer) which is applied to terminal 58. MDPT is extended to terminal 22 (fig. 1-13) to input 8 of OR 18B. The high 10 output of OR 18B is PCTP. From this point, as with message numbering, the precedence character is sent to the distant station. PCTP is applied to the character store Encoder circuit (fig. 1-19) on input terminal A2A19P1-9. This high pulse is applied to input 8 of ANDS 1B, 6B, 11B, 16B, and 21B. Input 9 of the same AND's are enabled with high levels from the baud of precedence character which has been stored on this logic card since it was sent from the input TTY Device to start the message transmit operation. Once PCTP arrives, the precedence character is decoded on this logic card and is gated to the Transmit Buffer. The TCU shifts this character out to the ADMS. The TCU is now ready to transmit the first character of the body of the message.

1-42. Preparation for Transmission of Message Body, Functional Analysis

a. Once the precedence character has been sent to the ADMS, the inhibit must be removed from the input TTY device clutch so that the message body is allowed to be sent to the TCU, and out to the distant station. PCTP (fig. 1-18) is applied through terminal 42 to the reset level input of

FF3. PCTP is applied (fig. 1–11) through terminal 47 to input 8 of OR 4B. Output 10 of OR 4B is applied to terminal 49 as the high PCFT (precedence character Flop Toggle) signal, and extended through terminal 43 (fig. 1–18) to toggle 5 (T) input of FF3. This resets FF3 and its one output, PCDS (Precedence Character detected & stored) goes low. This low level is applied to terminal 45 and extended through terminal 49 (fig. 1–15) to input 7 of OR 3B. Once the FLGS signal is disabled (by transmission of the control character which starts message transmission), input 3 of OR 3A is low. Whether FF12 (fig. 1–17) is reset due to the end of the transmission identifier or because FF12 was never set in the first place (Message numbering was disabled), output 2 of FF12 is low and is applied to terminal 53 as MNFG (Message Numbering Flag Generate Not). MNFG is extended to terminal 12 (fig. 1–15) and to input 8 of OR 3B. Since signals CANS, SRRC and ABNI-1 are disabled, output 2 of OR 2A is high and is applied to input 9 of AND 12B. The inactive condition of the TRANS HALT FF17 causes input 7 of AND 12B to be high. At every time 8 (TATE) of the Transmit Baud Counter, CLEP is generated, and applied to input 8 of AND 12B. Output 10 of AND 12B applies a positive pulse to the direct set input of FF13, CLUTCH CONTROL. The one output is CLUP which pulls the TTY input device clutch and starts device sending data to the TCU.

b. The output of AND 12B is also applied to terminal 9 as PCCP (Precedence Character Clear Pulse). This is extended to terminal 39 (fig. 1–19) and to input 8 of ORS 2B, 7B, 12B, 17B, and 22B, clearing the precedence character from the auxiliary buffer.

c. There are two points which it is necessary to discuss at this point, both of which have been previous to this point in time. In paragraph 1–30*g*, it was stated that, during transmission of the Cancel Control Character, the Transmit Buffer (fig. 1–18) is zeroed, while the control sequence characters are being shifted out. In this way if another control sequence is required to be transmitted after cancel is transmitted (in association with a received message) before the precedence character is transmitted, the buffer will be cleared. Also once the precedence character is detected and stored, the buffer must be cleared to ready the buffer to receive transmission identifier characters. Also, once the precedence character is received by the TCU from the TTY device, the blind on the receiver (distant station must be removed) so that the Transmission Identifier (if it is not inhibited), the precedence character, and the message are allowed to be sent to the distant station. Once the precedence character is detected, and stored, a high level is applied to input 7 of AND 18B (fig. 1–11). During the transmission of the first character of the control sequence which precedes the message (START or otherwise) CC1P (a high pulse) is generated by the Transmit baud counter (fig. 1–10) coincident with CCLP. This is applied to terminal A2A8P1–34 (fig. 1–10) and extended through A2A10P1 terminal 54 (fig. 1–12) to input 9 of AND 18B. Output 10 of AND 18B goes high and is applied to input 8 of OR 10B. This resets this FF and the low BLFF signal is applied to terminal A2AP1–24 and extended through terminal A2A18P1–48 (fig. 1–18) to input 8 of AND 4B. This removes the blind. When information is sent to the ADMS, it is sent by way of the Transmit Buffer (fig. 1–18) on output terminal 24, TTLG–24, as +5 volts for ones and ground for zeros. From here, it must be converted to the +6 volts (ones) and −6 volts (zeroes), respectively, used on the transmission lines to the ADMS. This conversion is done on logic card, A2A7 Timing Generator (fig. 1–9). TTLT is applied to input terminal 24. If the data is a zero, a ground is applied through Resistor R4, to the base of Transistor Q1. This shuts off Q1, placing a positive voltage (from the +12V supply through Resistor R6), at the junction of diode CR4 and R8. The −12 volt through Resistor R7 causes CR4 (a 15V zener diode) to break down. The voltage at the junction of CR4 and R7 is approximately −4 volts. The base of transistor Q3 on (NPN) becomes positive with respect to the emitter through Resistor R9. This causes transistor Q3 to conduct, placing the −6.2 volts (through R10) TTLG Terminal 23 (a zero). Also the +12 volts is applied to Transistor Q2 through Resistor R6 and R8 making Q2's base positive with respect to the emitter. This shuts off Q2. If a one is to be transmitted, +5 volts is applied through R4 to the base of Q1, causing Q1 to conduct. The collector of Q1 is at ground and this ground is applied through R8 to the base of Q2 (a PNP). Q2 conducts and +6.2 volts is applied through R10 as TTLG. Also, −12 volts is applied through R7 and R9 to the base of Q3, making the base negative with respect to the emitter (which is connected to −6.2 volts). Q3 is shut off. Diode CR4 blocks the −12 volts from having a ground path. These levels, which leave A2A7 (fig. 1-9) (TTLG, terminal 23; and TTLG TR, terminal 24) are applied to (fig. 1-21) Logic Card A2A1, Transmit Line Filter Driver. TTLG is then applied to the input of an emitter follower, the purpose of which is to provide drive, thus reducing noise. The emitter follower output is then applied to terminal 19 and extended through the Control Indicator Panel to the T&R Filter. From here the TTLT and TTLT-TR (return) signals are applied to the TTY output device.

1–43. Detection of 4N's (EOM), Functional Analysis A2A18

a. The message body includes an EOM (End-of-Message Sequence) which consists of 4 continuous N's. As each N is received, it is decoded by OR 16 (fig. 1-18). Where the first N is decoded, the output of OR 16 becomes high (Input 10 is low). The high output 2 of OR 16 is the Decode N (DECN) level which is extended through output terminal A2A18P1-34, through input terminal A2A14P1-38 (fig. 1-15) to input 9 of OR 6B. Output 10 of OR 6B goes low and is applied to input 4 of OR 6A. Input 3 of OR 6A is low since BLFF is disabled. The N's counter, which consists of FF9, 14, and 15, has been cleared since the time power was applied to the TCU. Thus, the low (one) output of FF15 is applied to input 5 OR 6A. Output 2 of OR 6A goes high and is applied to the set and reset level input of FF9, the least significant N counter FF. At Time 6 late (TSIL) following detection of the first N, FF9 becomes set. Following detection of the second N FF9 becomes reset and FF14 becomes set. Following detection of the third N, FF9 becomes set. Following detection of the fourth N FF's 9 and 14 become reset, and FF 15 becomes set.

b. At this point, the low zero output of FF15 is applied to input 9 of OR 8B. The low one output of FF9 is applied to input 7 of OR 8B. Output 10 of OR 8B goes high and is applied to output terminal 48 as EOMS (End of Message Sent). EOMS is also applied to input 4 of OR 2A. This prevents the TTY input device clutch from being pulled at this point.

1–44. Transmission of End-of-Message, Functional Analysis

a. From terminal A2A14P1-48 (fig. 1-15) EOMS is applied to terminal A2A9P1-14 (fig. 1-11) and extended to input 5 of OR 8A. Output 2 of OR 8A goes low and prevents a cancel (which may have been initiated manually) from being generated while the TCU is in the EOMS state. Also EOMS is applied to input A2A18P1-33 (fig. 1-18) and to input 10 of OR 16. This prevents any extraneous N accidentally placed on the TTY input device tape, from being interpreted as part of the EOM sequence, preventing the N's counter (fig. 1-15) being advanced further than required.

b. The EOMS signal (para 1-42) is also applied through input terminal A2A10P1-5 of the Transmit Repeat-Retransmit Sequence circuit (fig. 1-12) to input 4 of OR 25A. Output 2 of OR 25A goes high and is applied to input 8 of OR 16B which operates with OR 16A as the REP (Repeat) flip-flop. This sets the flip-flop (OR 16A and 16B) such that output 2 is high. The high 2 output of OR 16A is applied to input 5 of AND 21A. Input 3 of AND 21A is high since there is presently no RPTN (3 Repeat Condition Not).

c. When the CSSP pulse is generated (para 1-29*d*), CSSP is applied through input terminal A2A10P1-33 (fig. 1-12) to input 4 of AND 21A. AND 21A now has complete high input coincidence. Its 2 output is high and applied to the direct set input of 3 (P) of the REP (Repeat) FLAG flip-flop FF24; setting the Rep Flag flip-flop. The low zero (9) output of FF24 is applied to input 9 of OR 19, the REP PRIORITY GATE. The stop flag is disabled and input 5 of OR 19 is low. Input 3 of OR 19 is grounded. The Cancel flag is disabled and input 7 of OR 19 is low. Input 10 of OR 19 is low because a 3 Repeat condition does not exist. The RT (retransmit) flag flip-flop FF18 is reset, thus its low one (2) output is applied to input 8 of OR 19. The high one (2) output of FF24 is applied out of this logic card via output terminal A2A10P1-35, as the RPFG (Repeat Flag) level. RPFG is applied through input terminal A2A11P1-43 (fig. 1-13) to input 5 of OR 4A. Output 2 of OR 4A is high and is applied to input 9 of OR 24B. Output 10 of OR 24B is high and is applied through output terminal A2A11P1-48 as the FLGS (Control Sequence Flag Set) level to the Transmit Baud Counter and starts to initiate the action by which the repeat control sequence is eventually transmitted to the receiving device (ADMS).

d. The action is initiated by generation of CCLP (Control Character Load Pulse) (para 1-29*k*). This is applied to input terminal A2A10P1-26 (fig. 1-12) and to input 4 of OR 19 which makes all OR 19 inputs low. The high 2 output of OR 19 is applied out of this logic card on output terminal A2A10P1-51 as the LRPT (Load Repeat) signal. This loads the Transmit Buffer with the first half of the Repeat sequences. The Transmit Baud Counter initiates transmission of the second half of the sequence. Eventually the Repeat is transmitted to the ADMS. In reply to the TCU's transmission of a Repeat control sequence, the distant station transmits an ACK-1 or ACK-2, acknowledging that it has successfully received the message. When ACK-1 or ACK-2 is received and decoded the decoding of ACK-1 is performed similarly to that of ACK-2 (para 1-32) as the reply to the transmit cancel operation the AORP (ACK-1 received pulse) or ATRP (ACK-2 received pulse) is verified and applied to input terminal A2A10P1-22 as ACKV. Whether AORP or ATRP is received, depends on whether an even or odd number message has been transmitted to the distant station. The ACKV is applied to input 4 of OR 2A. Output 2 of OR 2A is high (directly or by way of output 10 of OR 3B) and this high is applied to the direct reset input 8(c) of FF's 23 and 22, which comprise the Repeat Counter. Control Character 2 pulse (which loads the second character of a control sequence, in this case repeat), also advances the repeat counter each time a repeat is generated. The REP FLAG FF24, at the time that LRPT (Load Repeat) was generated was enabled by OR 19 at its reset 7(R) and set 4(S) inputs. When CC2P is generated, it is applied to the toggle(T) input of FF24, resetting FF24. This, in turn disables RPFG, which disables FLGS-ACKV is also applied to terminal 25 (fig. 1-15) and extended to input 4 of AND 25A. Input 3 of AND 25A is high because of the presence of EOMS. Output 2 of AND 25A goes high and is applied to terminal 26 as EMVP (End of Message Verified Pulse.) EMVP is applied to terminal 54 (fig. 1-7) and extended to input 4 of OR 10A. Output 2 of OR 4A goes high and is applied to terminal 55 as EMVP-1 pulse. EMVP-1 is applied to terminal 52 (fig. 1-13) and extended to input 3 of OR 10A, resetting this FF. This in turn extinguishes the MSTI (Message Transmitted Indicated) lamp.

1-45. Blinding of Distant Stations During Intermessage State, N Decoding, and TTY Disabling, Functional Analysis

a. Recall that when the fourth N is received (fig. 1-15), the N's counter is in state 001. At the next time six late (TSIL), following receipt of the 4th N. TSIL is applied to input 3 of AND 10A. The high one output of FF15 is applied to input 4 of AND 10A. Output 2 of AND 10A is a high pulse that directly sets FF14. The now high one output of FF14 is applied to input 3 of AND 19A. The high one output of FF15 is applied to input 5 of AND 19A. Output 2 of AND 19A is high and is applied to terminal 35 as EMBS (End-of-Message Blind). EMBS is extended through input terminal A2A9P1-51 (fig. 1-11) to input 4 of the flip-flop consisting of OR 10A and B. This sets the flip-flop producing BLFF (Blind FF). BLFF is applied to terminal A2A9P1-24, and extended through terminal A2A18P1-48 (fig. 1-18) to input 8 of AND 4B. At this time presumably ENQF is present (Enquiry Response is not being sent by the TCU) and this places a high level on input 9 of AND 4B. Whether or not AND 4B conducts high (which produces the blind on the distant station) depends upon the condition of input 7, SGDN. As long as a control sequence is not being sent, the blind will exist and remain during the intermessage state, (i.e. from the completion of transmission of the current message until the beginning of transmission of the next message). This is done so that extraneous characters which may be present on the TTY input device tape during the intermessage state, will not reach the distant station. During transmission of any control sequence which may be required SGDN becomes disabled thus removing the blind and allowing the control sequence to reach the distant station. Once the precedence character for the next message is detected and stored, the blind is removed by disabling BLFF.

b. Recall that the purpose of the N's Counter (fig. 1-15) is to decode 4 consecutive N's, which is the end-of-message condition. In this regard AND 7 performs a special function. This is to assure that, if 4 N's are sent (nonconsecutively) during the course of the transmission of the message body, they will not add and be interpreted as an EOM. Input 7 of AND 7 is the zero output of FF15 which indicates that an EOM has not been received. Input 9 of AND 7 signifies that an N has not been received. Input 8 of AND 7 is CONN (Control Sequence Not Sent). Input 4 of AND 7 is time 6 late TSIL of the Transmit Baud Counter. Output 2 of AND 7 is applied to input 9 of OR 11B. Output 10 of OR 11B is applied to input 4 of OR 11A. Output 2 of OR 11A is applied to the direct clear 8(c) input of the N counter flip-flops (9, 14, 15). Thus during TSIL of every TCU cycle, if an N has not been received, if the TCU is not in the EOM state, and if a control sequence is not being sent, the N's counter becomes cleared. In this way unless consecutive N's are received, the counter will not store them. The CONN indicates that if a control sequence is required in association with a received message, it can interrupt the N count. Then after the control sequence is completed the N's count resumes.

c. As described in paragraph 1-43, where EOM is detected by the N's Counter (fig. 1-15) AND 12B is disabled, preventing FF13 from being set during End-of-Message. FF13 which is currently set must be reset to stop the TTY device during this time and during the intermessage state, following successful, complete transmission. EOMS is input 4 of OR 2A (from EOMS). Its output is low and in addition to disabling AND 12B, is also applied to input 3 of OR 8A. Output 2 of OR 8A goes high and is applied to terminal A2A14P1-23 as HALT. HALT is extended through terminal A2A8P1-19 (fig. 1-10), to input 8 of AND 14B, and to A2A19P1-54 (fig. 1-19) to input 5 of OR 19A. Output 2 of OR 19A goes high and is applied to terminal A2A19P1-37 as CLRE (Clutch Reset Enable). CLRE is extended through terminal A2A14P1-52 (fig. 1-15) to the reset level input of FF13. At the same time halt is produced (which generates CLRE), HALT is applied to terminal 17 and extended to the toggle input of FF13. This resets FF13, disabling CLUP and the TTY clutch. The character which produced SPDT is allowed to be shifted into the Transmit Buffer but once it has shifted in, TSIL advances the N's counter to 011, which produces EMBS. This then blinds the distant station from this character and the Buffer is zeroed. Once EMBS is produced the Blind FF (fig. 1-11) becomes set. BLFF and PCDN (precedence Character Detected Note) combine (fig. 1-15) to produce CPDR at the 2 output of AND 12A. CPDR is applied to terminal A2A14P1-18 and extended to terminal A2A19P1-52 (fig. 1-19) and to input 3 of OR 19A. Output 2 of OR 19A is high and again produces CLRE which keeps the TTY device OFF during the intermessage state.

1-46. Failure of ADMS to Reply in Time to a Transmitted Message Repeat Functional Analysis

a. When the TCU transmits a repeat, the ADMS may transmit an ACK in response. The ACK must be received before 3 repeats have been transmitted. When this does not occur, an alarm is generated. Before the first repeat was sent, the high output 2 of OR 19 (fig. 1-12) was applied to input 9 of OR 25B. The 10 output of OR 25B was high and applied to the set 4 (S) and reset 7 (R) level inputs of FF23. When the CC2P (a high pulse, signifying the end of transmission of the first repeat) was generated, a pulse was applied to the pulse input 5 (T) of FF23, setting FF23. This places a count of 1 in the Rep Counter (10). If the acknowledge is not received directly, ACKV (acknowledge verified) is not applied to input A2A10P1-22 and RP flip-flop (OR 16A and B) was not reset. This retains the high level to input 5 of AND 21A. Since, at this point, the Rep Counter is in count 1 (10), the low one (2) output of FF22 is applied to input 8 of AND 21B. Output 10 of AND 21B is low and applied for input 3 of OR 11A. Inputs 4 and 5 of OR 11A are grounded. Output 2 of OR 11A is high and is applied to input 3 of AND 21A. If the Acknowledge is not received by a certain time (which is the repeat) timer interval (2 to 4 seconds) another repeat will be transmitted. At the end of the 2 to 4 seconds CSSP (Control Sequence Sync Pulse) is again generated from the output of OR 18B (A2A14).

b. AND 21A is again enabled and its output 2 sets Repeat Flag FF24 (fig. 1-12). Once again repeat is transmitted to the ADMS and this eventually causes the REP COUNT (FF 23 and -22) to advance to count 2 (01). The situation now is that the TCU has transmitted a message and two repeats and the ADMS has still not acknowledged. Recall that 2 to 4 seconds are permitted between each transmission of the repeat control sequence. If the proper acknowledgement is still not obtained, another repeat is transmitted after 2 to 4 seconds and the repeat counter advances to count 3 (11). The high one (2) output of FF23 is applied to input 7 of AND 21B. The high one (2) output of FF22 is applied to input 8 of AND 21B. This causes output 10 of AND 21B to go high and is applied out of this circuit on output terminal A2A10P1-46 as REPA (repeat alarm). Output 10 of AND 21B also REPA disables OR 19 on input 10.

c. REPA is also applied to the Transmit Cancel-Stop Sequence circuit (fig. 1-11) on input terminal A2A9P1-43 and disables CANCEL FLAG FF12. This prevents CANCEL from being transmitted until the current message situation is corrected.

d. REPA is applied (fig. 1-12) through resistor R4 to the base of Transistor Q3. Q3 conducts generating an audible and visible alarm on the TCU control panel, signifying a three repeat alarm condition. REPA is also applied to input 9 of OR 15B. Output 10 of OR 15B goes high and is applied on output terminal A2A10P1-47 as the high SRRC (Stop received or 3 repeat alarm) condition.

e. SRRC is extended through input terminal A2A14P1-13 of the Input Device Control (fig. 1-15) to input 5 of OR 3A. Output 2 of OR 3A goes high and is applied to input 3 of OR 2A. Output 2 of OR 2A disables AND 12B, preventing FF13 from being set. Output 2 of OR 2A also is applied to input 3 of OR 8A. Inputs 4 and 5 of OR 8A are grounded. Output 2 of OR 8A becomes high and enables the HALT signal. At the following SPDT from the TCU after detecting an input character, CLRE is produced and is applied to the reset level input of FF13. SDPT is also applied to the pulse input of FF13, resetting it. This disables the TTY clutch while the alarm condition exists.

f. Once the alarm condition is present, and the transmission capability of the TCU has been temporarily curtailed, the repeats can be continued, three at a time, manually. This is done from the Control-Indicator Panel. The operator presses the Start Send Switch producing SSPW which extends a high on input terminal A2A10P1-13 (fig. 1-12) to input 3 of OR 3A. Output 2 of OR 3A is high and is applied to input 3 of OR 2A. Output 2 of OR 2A is high and is applied to the direct reset 8(c) inputs of the Repeat Counter FF22 and 23. This resets the repeat Counter to all zeros. AND 21A output 2 is high and sets FF24 initiating transmission of 3 more repeats as desired. If the alarm condition persists (the ADMS does not answer with its last response) more repeats can be initiated or another means may be taken to correct the situation. Until the trouble is remedied, no more data can be transmitted, although it can be received.

1-47. N's Counter Operation Subsequent to Receipt of Acknowledge from ADMS, Functional Analysis

Recall that the EMBS (End-of-Message Blind) is set when the N's counter (fig. 1-15) is in count 011 (FF9, FF14, FF15). When the acknowledge is received for the message from the distant station, signifying complete, successful transmission of the message, the TCU generates a pulse AKRP (Acknowledge Receive Pulse), described in paragraph 1-43. AKRP is applied to (fig. 1-15) terminal A2A14P1-26 and extended to input 9 of AND 10B. The one output of FF15 is applied to input 8 of AND 10B. Output 10 of AND 10B sets FF9 through the direct set input. The condition of the N's Counter at this point is 111. Under normal conditions, the N's counter remains in this condition until the character for the next message is detected and stored; at this time, PCDS is applied to input terminal A2A14P1-49, and extended to input 7 of OR 11B. Output 10 of OR 11B is applied to input 4 of OR 11A. Output 2 of OR 11A is applied to the direct reset input of FF's 9, 14, and 15, clearing the N's counter.

1-48. Send Delay Operation (TCU Mode), Functional Analysis

a. Once a precedence character has been detected and stored (signifying that a message from the TTY input device is forthcoming), and if the TCU is not in the End-of-Message condition, a character (data or control) must be sent within a certain time. If this is not done, a start control sequence is sent as a dummy character as many times as necessary until another character is ready to be sent.

b. At every TATE (Time 8) of the Transmit Baud Counter, a high pulse is applied to input 5 of OR 11A (fig. 1-10), which operates with OR 11B as the SEND DETECT FF. This sets OR 11, causing the low 2 output to be applied through Resistor R1 to the base of Transistor Q1. Transistor Q1 is the input stage of the SEND DELAY Timer, which is an adjustable 10 to 50 msec timer. When the low signal is applied through resistor R1 transistor Q1 turns off. This allows a charge to build across C5 through R3 and R4. R4 is adjustable and determines the delay time. When C5 has charged sufficiently from the +12 volt source, unijunction Q2 conducts. When Q2 conducts, a positive voltage is developed at the junction of R19 and R6 because of voltage divider R5, Q2 and R19. This positive voltage is felt at the base of Q3. Transistor Q3 conducts through resistor R7 and applies a low pulse to input 5 of OR 1A. Output 2 of OR 1A goes high and is the SDDP (Send Delay Pulse). This pulse is a short duration for as soon as unijunction Q2 starts to conduct C5 discharges, shutting off Q2. The total time from input to Q1 to output of OR 1 is 10-50 milliseconds. If, within this time, following the initiation of shifting out of a previous character, shifting of the next character is not initiated, the SDDP is applied to term in a A2A8P1-38.

c. The output from terminal A2A8P-38 is extended to terminal A2A9P1-4 (fig. 1-11) and applied to input 3 of OR 4A. If the TCU is not in the EOM state, output 2 of OR 4A (STEN) A2A9P1-37 is extended to A2A11-13 (fig. 1-13) and applied to input 8 of AND 21B. NEOM (No End-of-Message) is applied to input 9 of AND 21B. If the TCU is in the intramessage state the high output of OR 10 Flip-Flop is applied to input 7 of AND 21B. Output 10 of AND 21B supplies a high pulse to input 3 of the START flip-flop, OR 20A and B, setting it. The high output from pin 10 of OR 20B is applied to input 9 of OR 9B. Output 10 of OR 9B is high and directly sets the START FLAG FF25. This initiates transmission of a START control sequence, which is used as a dummy character. START is sent as many times as required until a normal character is ready to be transmitted.

Section V. MESSAGE RECEPTION

Note: Refer to note preceding paragraph 1-10.

1-49. Receive Initialization, Functional Analysis

a. When the ADMS is turned on it sends an initializing cancel (for Ack-2 synchronization) in much the same manner as the TCU sends an initializing cancel. The cancel received is applied to the Receive Buffer Register Decoder. The Receive Control Sequence circuit (fig. 1-5) decodes it into a Cancel Receive pulse (CARP). This is accomplished by FF11 and AND 7B, similar to the Ack 2 receive described in transmission initialization. This action results in generating a CARP on output terminal A2A3P1-17. CARP is applied to the Receive, EOM (fig. 1-6) on input terminal A2A4-P1-6. This is applied as a high pulse to input 9 of OR6B. The high 10 output of OR6B is applied to input 8 of AND 7B. If there is no abnormal output device, input 3 of OR3A is low. Output 2 of OR3A goes high and is applied to input 7 of AND 7B. The 10 output of AND7B goes high and is applied to input 9 of OR12B. Output 10 of OR12B is high and is extended to output terminal A2A4-P1-8 as the high SDAK (Send Acknowledge) pulse.

b. SDAK is applied to input terminal A2A11-P1-8 of the Transmit Start and Acknowledge Sequence circuit (fig. 1-13). This FF has previously been cleared by PWRC. Thus, SDAK sets FF22. The high one (2) output of FF22 is applied to the set level input 4(s) of ACK FLAG flip-flop FF17.

c. On the Input Device Control FF (fig. 1-15), the CCCP (Control Character Combined Pulse) is generated at time T6 of the Transmit Baud Counter in coincidence with CCLP. CCCP (fig. 1-13), a high pulse, is extended through input terminal A2A11P1-50 to the toggle 5(T) input of FF 17, setting the flip flop. CCLP (fig. 1-10), a high pulse, is extended through input terminal A2A11P1-41 to input 3 of OR 2 and to input 10 of OR 8. The low zero (9) output of FF 17 is applied to input 9 of OR 2. None of the other control character flags are (presumably) present;

thus all other inputs of OR2, except 3, are low. FF17 enables the FLGS level through OR 4B and OR 24B which is used to generate load pulses.

d. When power is first applied to the TCU, a high pulse (PWRC pin 36) is applied (fig. 1-6) to input 3(c) of OR 12A. Output 2 of OR 12A goes high and is applied to the direct set input 3 of FF17 setting this FF. The high one (2) output of FF17 is routed out of this circuit at output terminal A2A4P1-22 as AKTE (Acknowledge 2 Enable).

e. AKTE is applied, through input terminal A2A11P1-45 (fig. 1-13) to input 9 of AND 7B. AND 7B now has high input coincidence and its output 10 becomes high and is routed out of this circuit on output terminal A2A11P1-40 as the LAK2 (Load Acknowledge 2) signal. Acknowledge 2 is eventually generated (in two character stages) and transmitted to the ADMS. The procedure for generating this control character is similar to that for cancel described in paragraph 1-29.

f. As with the reception of Acknowledges, Transmit Acknowledgements (ACKS) must alternate between ACK-1 and ACK-2. That is initially the TCU responds to a received cancel with an ACK-2. The first message which the TCU receives from the ADMS, thereafter must be acknowledged with an ACK-1. The second message must be acknowledged with an ACK-2 and so on, alternately. Each received message ends with EMRP (End-of-Message-Receive Pulse) which is applied (fig. 1-6) through input terminal A2A4P1-11 through the pulse 5 (T) input to FF17. On A2A5 (fig. 1-7) when a message is received, MREE a high level, is applied to terminal A2A5P1-15 and extended through terminal A2A4P1-50 (fig. 1-6) to the set and reset level inputs of FF17, allowing the ACK Rec. flop to toggle only once per EMRP. This enables the TCU to generate alternate ACK transmissions. FF17 outputs are AKOE (ACK-1 Acknowledge) enable (FF17 reset) and AKTE (ACK-2 Acknowledge) enable (FF17 set).

1-50. Receive Start Detection, Functional Analysis

a. This paragraph describes the method by which the TCU detects the presence of data coming into the TCU, interrupting an existing idle (no information being transferred) condition.

b. During idle conditions, a continuous Mark (high signal, +5 volts) is transmitted on the incoming lines. The START condition for any incoming character is the abrupt switch to a SPACE (low signal, ground) condition. During idle conditions, the MARK, shown as TTLR-2 (fig. 1-6) is applied to input terminal A2A4P1-34 +0 input 3 of AND 7A. Input 5 of AND 7A is high. During this time, the SDRR (Start Detect Receive Reset) signal is high since SDRR was produced by the previous application of TCU primary power. SDRR applies a high level to input 4 of AND 7A. Output 2 of AND 7A applies a high level to input 8 of the flip-flop comprised of OR gates 9A and 9B. The high input results in a low output at 10 of OR 9B. This is the SPRE (Start Pulse Receive Enable) signal which places the TCU in a condition to detect a forthcoming SPACE input. The SPRE signal is also applied to input 3 of OR 9A. Input 5 of OR 9A is grounded. Input 4 of OR 9A is low since PWRC (Power on Clear) reset FF14 (fig. 1-8) disabling SDRS. The complete low input coincidence on OR 9A results in a high output at pin 2 which is applied to input 7 of OR 9B. The flip-flop (OR's 9A and 9B) insures that, when a SPACE arrives at pin 3 of AND 7A, the output, SPRE, will be retained due to the high input at 7 of OR 9B.

c. SPRE is extended from the Receive End of Message circuit through A2A4P1-21 and A2A6P1-26 to input 3 of OR 5A (fig. 1-8). Input 4 of OR 5A is HSCL (High Speed Clock which is free running and operated with the application of primary power.) This clock is used to detect for the presence of a SPACE (input) condition. Its high frequency (in excess of 5000 cps), compared to the relatively low receive baud rates of 45.45, 74.2 or 75, enables it to detect the MARK to SPACE shift as soon as the shift occurs. Input 5 of OR 5A is TTLR-2. When TTLR-2 becomes a SPACE, complete low input coincidence occurs on OR 5A, producing a high output on pin 2. This is applied to input 3 of OR 3A which along with OR 3B comprises a flip-flop Output 2 of OR 3A becomes low and is applied to input 7 of OR 3B. Input 9 of OR 3B is currently low, since PWRC is in its reset state. Because the idle (MARK) condition has existed until this time, the set (1) output of SP (START Pulse) DETECT FF14 is low and is applied to input 8 of OR 3B. Since complete input low coincidence now exists on OR 3B, output 10 of OR 3B goes high. This high is applied to the 4(S) input of SP DETECT FF14. It is also applied to input 5 of OR 3A, which keeps the 2 output of OR 3A low. In this way, output 10 of OR 3B stays high despite the fact that output of OR 5A alternates between high and low as the HSCL advances through successive high and low states. In addition to the high output of OR 3B enabling the SP DETECT FF(14), it is applied to the C (clear) input of the flip-flops 20, 19, 18, and 17, thus clearing the BAUD COUNTER, which is comprised of these flip-flops. When the HSCL advances to a high pulse condition, the SP DETECT FF14 becomes set, signifying the fact that the TCU has detected a start condition on its incoming lines. When this occurs, the O (reset) output of FF14 becomes low, disabling the SDRR signal. The high 1 output of SP DETECT flip-flop FF14 also resets the flip-flop comprised of OR 3B, and produces the SDRS (Space Detector Receive Set) signal which resets the flip-flop comprised of OR 9A and 9B (fig. 1-6). This produces SPRE which is applied to terminal 21.

d. The high SPRE input is applied to input terminal 26 (fig. 1-8) and from here applied to input 3 of OR 5A. Output 2 of OR 5A goes low and is applied to input 3 of OR 3A. Input 4 of OR 3A is grounded. Complete low input coincidence is now present; thus, output 2 of OR 3A is high. This is applied to the set (4S) and reset (7R) of the Baud Counter flip-flop.

e. When the power was initially applied to the TCU, the free running Baud Counter, which is comprised of FF19-18 and 17, starts to count. Once a detected start is received, the Baud Counter is cleared. In this way, the Baud Counter is synchronized with the incoming data. Figure 1-28 is a timing chart showing the Receive Baud Counter and Mark Interval Counter timing sequence. The purpose of FF20 is to provide frequency division. Both the BCRN and BCRP, which occur coincidentally in time, and are free running upon application of primary input power, operate at twice the baud rate. Once the set S(4) and reset R(7) inputs of FF20 are enabled, each application of BCRP will complement this flip-flop. Thus FF20 will enter the one (2) state at the same rate as the baud count. The zero (9) output of FF20 is applied to the trigger 5(T) input of FF19 the least significant baud count. Thus each time FF20 enters the one state, FF19 is complemented and FF19 counts at the baud rate. The one (2) output of FF19 is applied to the pulse 5 (T) input of FF18. Thus each time FF19 enters the zero state, FF18 complements (at one half the baud rate). The one (2) output of FF18 is applied to the pulse 5 (T) input of FF17. Thus, each time FF18 enters the zero state, FF17 complements (at one quarter the baud rate). The above action by the three FF's provides the 3 stage Baud count. The Mark Interval Counter, comprised of FF's 25, 24, and 23, operates similarly with the Baud Counter. Counting is performed the same way (but not at the same rate). The one (2) output of FF25 is applied to the pulse 5 (T) input of FF24. Likewise, the one (2) output of FF24 is applied to the pulse 5 (T) input of FF23.

1-51. Receiving Control Characters, Functional Analysis

a. When any control character is to be sent to the TCU (regarding either message transmission or reception) there must be a time range of 170 to 480 ms since the last character was sent. A MARK character is one complete cycle of Baud Counter. Thus, after the CANCEL Transmit character is sent, and after the Baud Counter (fig. 1-8) has advanced three times, the MARK Interval Counter, which consists of FF's 25, 24, and 23, is in a count of three (110), respectively.

b. When the Baud Counter is in a count of 7, the low zero (9) output of FF20 is applied to input 5 of OR 12A. The low zero (9) output of FF17 is applied to input 4 of OR 12A. The BCRN pulse is applied to input 3 of OR 12A. Complete input low coincidence is present on OR 12A; thus, its 2 output is low and is applied to input 8 of OR 11B. The low zero (9) output of FF19 is applied to input 9 of OR 11B. The low zero (9) output of FF18 is applied to input 7 of OR 11B. OR 11B now has complete input low coincidence; thus its 10 output is low and is applied to input 7 of OR 21B. Input 8 of OR 21B is grounded. As long as the MARK Interval counter is not in count 3 or count 4, a low input is applied (*c* and *d* below) to input 9 of OR 21B.

c. If the Mark Interval Counter is in count 3 (FF 25, −24, and −23 contain, respectively, 110) the low zero (9) output of FF25 is applied to input 3 of OR 10A. The low zero (9) output of FF24 is applied to input 4 of OR 10A. The low one (2) output of FF23 is applied to input 5 of OR 10A. OR 10A now has complete low input coincidence and its 2 output is low. This is applied to input 9 of OR 13B. Inputs 7 and 8 of OR 13B are connected to ground; thus, output 10 of OR 13B is high and is applied to input 7 of OR 10B. Output 10 of OR 10B goes high and is applied to input 9 of OR 21B. If the Mark Interval Counter is not in count 3, input 7 of OR 10B is low.

d. If the Mark Interval Counter is in Count 4 (FF25, −24, and −23 contain, respectively, 001), the low one (2) output of FF25 is applied to input 7 of OR 9B. The low one (2) output of FF24 is applied to input 8 of OR 9B. The low zero (9) output of FF23 is applied to input 9 of OR 9B. OR 9B has complete input negative coincidence; thus, its output 10 is low and is applied to input 3 of OR 21A. Inputs 5 and 4 of OR 21A are low due to the application of a ground. Output 2 of OR 21A goes high and is applied to input 8 of OR 10B which produces a high at output 10. If the Mark Interval Counter is not in count 4, input 8 of OR 10B is low. When the Mark Interval Counter is not in count 3 or 4, input 9 of OR 21B is low. OR 21B is enabled and its 10 output is high. This is applied to input 7 of OR 16B.

e. When the Mark Interval Counter is in Count 3 (as described in *c* above), a low signal is applied from output 2 of OR 10A to input 5 of OR 8A. When SP (START PULSE) Detect is present, a high signal is applied to input 9 of OR 22B which operates with OR 22A as a flip-flop. Output 10 of OR 22B is low and is applied to input 5 of OR 22A. Input 4 of OR 22A is low because PWRC by this time is disabled. Input 3 of OR 22A is low since the MDRE (Mark Detect Reset) level is disabled. OR 11B decodes the output of the Baud counter and is low unless the counter is in the 1111 stage. Output 10 of OR 11B is extended over the MDRN (Mark Detect Receive Not) lead at output terminal A2A6P1-46 through input terminal A2A4P1-44 (fig. 1-6) through OR 3 (inverter) to output terminal A2A4P1-43 as the MDRE lead.

f. Complete input negative coincidence is now present (fig. 1-8) on OR 22A; thus its high output 2 is applied to input 7 of OR 22B. This keeps output 10 of OR 22B low even when the SP Detect enable level leaves.

g. The low output 10 of OR 22B is applied to input 3 of OR 8A. OR 8A has complete low input coincidence; thus its 2 output is high and is applied to input 8 of OR 16B.

h. When the Mark Interval Counter is in count 4 (as described in *d* above), a low is applied to input 7 of OR 8B. Input 8 of OR 8B is grounded. When the Baud Counter is in count 6, a low is applied to input 9 of OR 8B. OR 8B now has complete low input coincidence; thus its output 10 is high and is applied to input 9 of OR 16B.

i. The foregoing subparagraphs have described three inputs to OR 16B which represent three methods by which the Mark Interval Counter is advanced. To summarize, they are:

(1) Baud Count 7 • Not Mark Count 3 or 4 (from Mark Counts 0 to 2)

(2) SP Detect • Baud Count 6 • Mark Count 3 (from Mark Count 3 to 4)

(3) Baud Count 6 • Mark Count 4 (from Mark Count 4 to 5)

j. Normally, the Mark Interval Counter will advance one step each time that the Baud Counter enters a full count (count 7). However, once it is in Mark Count 3 (or 4) it will not advance automatically when the Baud Counter reaches 7. This is because by this time (3 mark intervals), a control character can be received and the TCU must halt the Mark Counter to test for this. At Mark Count 3, the low level (Mark Count of three) is routed for input 5 of OR 1A. Input 3 of OR 1A is grounded. Input 4 of OR 1A becomes low where a BCRN (Baud Clock Receive Negative) pulse is applied. Output 2 of OR 1A is the MCOT (Mark Count of Three) pulse. This high pulse is applied out of this circuit on output terminal A2A6P1-6 to the Receive Control Sequences circuit (fig. 1-5) on input terminal A2A3P1-24. This is applied to input 3 of OR 20A which operates with OR 20B as a flip-flop. The low 2 output of OR 20A is applied to input 7 of OR 20B. Input 9 of OR 20B is grounded.

k. At Mark Count 3, a high signal is applied from output 10 of OR 10B (fig. 1-8) to input 9 of OR 1B. Output 10 of OR 1B is low and is extended through output terminal A2A6P1-7 as the COCR (Control Character Receive) signal to input terminal A2A3P1-41 (fig. 1-5) of the Receive Control Sequences circuit. COCR is applied to input 5 of OR 1A as a low signal. Recall that at Baud Count 6, SADA (Sample Data) low pulse is produced this is applied to input 4 of OR 1A from input terminal A2A3P1-33. Input 3 of OR 1A is low since COCD (Control Character Detect) is disabled since it is a high pulse of OR 22B. OR 1A has complete input low coincidence; thus its 2 output is a high pulse which is applied directly to the pulse 5 (T) inputs of FF6, −11, −12 and −17. The high pulse output of OR 1A is also applied to input 7 of OR 2B. Output 10 of OR 2B goes high and is applied to the pulse 5 (T) inputs of FF13, −24, and −22. Output 10 of OR 2B is applied as a high input to input 5 of OR 18A. Output 2 of OR 18A is high and is applied to the pulse 5 (T) input of FF19. The above flip-flops are sensing flip-flops for all the control characters which can be received. They are as follows: (They were all cleared by the PWRC signal, upon application of primary power.)

(1) FF6 REP (Repeat)
(2) FF11 CAN (Cancel)
(3) FF12 STOP (Stop)
(4) FF17 RT (Retransmit)
(5) FF19 ACK 2 (Ack 2)
(6) FF13 ACK 1 (Ack 1)
(7) FF24 START (Start)
(8) FF22 ENQ (Enquiry)

l. Depending upon which control character sequence is being received, the Receive Buffer is filled with one half (one letter) of the two contiguous characters which comprise a control sequence. This may be either ENQR (Enquiry Receive) on input terminal A2A3P1-20 STAR (Start Receive) on input terminal 48, AKOR (Ack 1 Receive) on input terminal A2A3P1-15, AKTR (Ack 2 Receive) on input terminal A2A3P1-18, RETR (Retransmit Receive) on input terminal A2A3P1-13, STPR (Stop Receive) on input terminal A2A3P1-12, CANR (Cancel Receive) on input terminal A2A3P1-9, or REPR (Repeat Receive) on input terminal A2A3P1-6. (Actually, Ack 1 and Ack 2, Retransmit, and STOP are control sequences received during transmission of data but are discussed here.) One of these high levels is applied to the set level input 4(s) of its respective flip-flop. The flip-flop which is enabled is set by output 2 of OR 1A. The high one (2) output of the FF which has been set is applied to input 5 or 9 of its associated AND (5 is the input to the A half of the AND, 9 is the input to the B half of the AND) AND 7A is associated with FF6 (REP); AND 7B, with FF11 (CAN); AND 16A, with FF12 (STOP); AND 16B with FF17 (RT); AND 8A, with FF19 (ACK 2); AND 8B, with FF13 (ACK 1); AND 23A, with FF24 (START); and AND 23B, with FF22 (ENQ).

m. When the second half (letter) of the control sequence arrives, at Mark Interval count 4, again the high output 2 of OR 1A is applied, this time to input 4 (A half) or 8 (B half) of one of the aforementioned AND's. Also the input from the Receive Buffer Register is applied to input 3 (A half) or input 8 (B half) of the AND associated with the control signal. The associated AND now has complete input high coincidence, thus its output 2 (half A) or 10 (half B) is high and is one of the control sequences as a pulse.

n. MCOT (*l* above) is applied through input terminal A2A3P1-24 to input 3 of OR 20A to test for an incoming control sequence. At the Receive Baud Counter (fig. 1-8), at Mark Interval Count 5, which is the time by which both halfs of the control sequence should have been applied to the TCU, the MARK Interval Counter FF25, −24, and −23 are in the states of 101, respectively. The low zero (5) output of FF23 is applied to input 5 of OR 9A. The low one (2) output of FF24 is applied to input 3 of OR 9A. The low zero (9) output of FF25 is applied to input 4 of OR 9A. OR 9A now has complete low input coincidence; thus its output 2 is low and is applied to input 5 of OR 2A. Input 4 of OR 2A is low due to the fact that the output of OR 22B is low. Input 3 of OR 2A is low since the TCU is not in the Received Disable condition. OR 2A now has complete input low coincidence; thus its 2 output is high and is the CCRT signal (Control Character Receive Terminate) which denotes the end of a control sequence. CCRT is applied through output terminal A2A6P1-11 to input terminal A2A3P1-53 (fig. 1-5) as a high signal to input 8 of AND 25B.

o. Recall that inputs 7 and 9 of OR 20B are low. The pulse output for the receive control character received is applied either to input 3 or 4 of OR 3A; or 7, 8, or 9 of OR 3B; or 3, 4 or 5 of OR 21A. If one of these is high, a high signal is applied to input 9 of OR 15B. Also PWRC is initially applied to input 5 of OR 3A. This resets the FF comprised of OR's 20A and 20B upon initial turnon of power. But now if the output 10 of OR 15B is low (no character was received), a low signal is applied to input 8 of OR 20B. OR 20B now has complete input low coincidence; thus its output 10 is high and is applied to input 4 of OR 20A. This locks the FF comprised of OR 20A-20B in this condition even after MCOT count 3 or 4 become disabled. The high signal output 10 of OR 20B is also applied to input 7 of AND 25B. When CCRT (denoting the end of a control character) is applied to input 8 of AND 25B, the output of AND 25B becomes high. This is the UNIX (Uniintelligible) signal and means that since a control sequence had started, it should have been finished and the fact that it did not finish indicates that it is half of a control sequence not followed by the second half and is not able to be identified. Or, it was never finished though it was supposed to, and is thus not able to be identified.

p. If UNIX is produced, it is routed through output terminal A2A3P1-22 to the Output Device Control circuit on input terminal A2A5P1-18 (fig. 1-7). This high signal is applied to input 4 of OR 15A. The output 2 of OR 15A goes high and is applied to input 5 of AND 20A. Input 4 of AND 20A is high since RTDS (Retransmit Disable Switch) located on the Simulator Panel is low when this switch is disabling the Retransmit function. Input 4 of OR 5A is low since a STOP (STPS) has not been sent, presumably. Input 3 of OR 5A is low since an end-of-message receive is not applicable for control characters. Input 5 of OR 5A is low because there has been no message received. OR 5A now has complete input low coincidence; thus its output 2 is high and is applied to input 3 of AND 20A. AND 20A now has complete input high coincidence, thus its output 2 is high. This is applied to input 9 of OR 11B which is used with OR 11A as a flip-flop. Output 10 of OR 11B is low and is applied to input 4 of OR 11A. Input 3 of OR 11A is low because Load Stop (which loads the stop transmit control sequence into the transmit Buffer and Decoder) does not apply to receive control sequences. Input 3 of OR 6A is low since MCOT (Mark Count of Three) is disabled. Input 5 of OR 6A is low because, since the character is unintelligible, neither start, Ack 1, Ack 2, RT, nor STOP pulses has been generated. Input 4 of OR 6A is low since PWRC is no longer present. OR 6A now has complete input low coincidence; thus its 2 output is low. This is applied to input 5 of OR 11A. OR 11A now has complete input low coincidence; thus its output of 2 is high and is applied to input 7 of OR 11B. This locks the flip-flop (OR's 11A and 11B) in this state so that after UNIX, output 2 of OR 11A will remain high. This is the MBLR (Maintain Blind on Receiver) level, at A2A3P1-6. It is applied (fig. 1-4) to input terminal A2A2P1-53 to terminal 4 of OR 5A. Output 2 of OR 5A is applied to input 9 of OR 5B. Output 10 of OR 5B is applied to the direct SET P(3) input of FF 25 and sets it to maintain the blind on the teletype device during this unintelligible period to prevent it from receiving the characters following the UNIX and prior to transmitting of the stop control sequence.

q. The CCRT (Control Character Receive Terminate), generated at Mark Interval Count five (signifying the termination of the received control character), is applied to input terminal A2A2P1-23 of the Receive Buffer and Decoder circuit. From here it is applied to the direct set P (3) inputs of FF3, -8, -13, -18, -23, and -24 through OR 10B. This sets these FF's so that the receiving device is blinded and does not receive the normal control sequences.

1-52. Receiving Start Control Sequence, Functional Analysis

a. The start receive control sequence is sent to the TCU to inform the TCU that a message is forthcoming. The two characters of the start control sequence are decoded as the SARP (Start pulse) (fig. 1-5). The decoding of START is similar to that of the other receive control sequences except that FF 24 and AND 23A are used in conjunction with this control sequence. The results of receiving Start causes the generation of SARP (Start Receive Pulse). SARP is applied to terminal 14 and extended through input terminal A2A5P1-37 of the Output device control circuit (fig. 1-7), to input 7 of OR 1B. Output 10 of

OR 1B goes high, is applied to input 3 of OR 1A; output 2 of OR 1A goes high, and is applied to input 4 of OR 12A, which operates with OR 12B as the intermessage flip-flop. This causes output 2 of OR 12A to go low and this low signal is applied to input 8 of OR 12B. Input 9 of OR 12B is grounded. Input 7 of OR 12B is low because both the PWRC and End-of-Message Received are disabled. Output 10 of OR 12B goes high and is applied to input 5 of OR 12A, locking the FF in this condition, even after SARP becomes disabled. The low output 2 of OR 12A is sent to output terminal A2A5P1-20 as the inverse of the BLDR (Blind Receiver) signal. This removes the blind from the output TTY device, preparing the TCU to print out the forthcoming message including the Start-of-Message sequence, which is the same as that for transmitted messages.

b. At the end of the message EOMR, and SPDR (the first character of a control sequence following EOMS), places flip-flop OR 12 to the opposite state, thus generating the Blind Receiver signal. In this way, during the intermessage state, the teletype output device will not print out extraneous data.

c. At the end of the intermessage state, provided that operation has thus far been normal, the ADMS will send a subsequent message, initiated by the Start Receive control character.

d. After the Start Control Sequence is received (fig. 1-8) COCR (Control Character Receive) which is low during its true state (when the control character is detected), goes to its "not" state which is high. COCR is applied from output 10 of OR 1B through output terminal A2A6P1-7 and A2A5P1-16 (fig. 1-7) to input 7 of AND 14B. SPCN (Start Pulse Control Not) which is a high pulse, is applied to input terminal A2A5P1-22 and to input 8 of AND 14B. SPCN is generated when a start Receive condition is detected, which is not part of an incoming control character. Thus SPCN is the result of the sensing of the receipt of data from the ADMS. Input 9 of AND 14B is high since the receive blind has been removed. When COCR, SPCN and BLDR occur, output 10 of AND 14B goes high, and is applied to input 7 of OR 22B, which is used with OR 22A as the Message Received FF. Output 10 of OR 22B goes low and is applied to input 5 of OR 22A. Input 4 of OR 22A is grounded. Input 3 of OR 22A is low provided output 10 of OR 6B is low, which occurs as long as neither PWRC, Cancel Receive pulse, nor ERAS (End-of-Message Receive Acknowledge Sent) are present. This causes output 2 of OR 22A to go high, and this is applied to input 9 of OR 22B, locking FF OR 22 in this condition, even after SPCN becomes disabled. The high output 2 of OR 22A is applied through resistor R2 to the base of Transistor Q1. This causes Q1 to conduct providing a ground path for the MREI (Message Received Indicator), located on the Control and Indicator Panel, the other end of which (at the panel) is connected to +12 volts, thus illuminating the lamp. Before Q1 conducted, the high resistance of R1 kept the lamp extinguished.

1-53. Receiving Data at Receive Buffer, Functional Analysis

a. When FF14 (fig. 1-8) becomes set denoting the detection of a space, the Baud Counter flip-flops are cleared. At the same time, the low from the one (2) output of FF20 is applied to input 3 of OR 6A. The low output from the zero (9) output of FF14 is applied to input 4 of OR 6A. When BCRN is present, a low pulse is applied to input 5 of OR 6A. Complete negative input coincidence exists on OR 6A; thus a high pulse is produced at output 2. This is the SRBC (Shift Receive Bit Clock). SRBC is extended through output terminal A2A6P1-8 to input terminal A2A2P1-14 of the Receive Buffer and Decoder circuit (fig. 1-4) to the pulse T (5) inputs of FF 3, -8, -13, -18, -23, -24 and -25 (23, 24, and 25 through OR 10A) which comprise the Receiver Buffer and Decoder. All of these flip-flops have been previously set as a result of the PWRC level.

b. SRBC gates the incoming space into FF3. The incoming space (TTLR-1) is applied to this logic card on input terminal A2A2P1-57 and converted to TCU logic levels by transistors Q3 and Q2. Refer to Logic Card, Receive Buffer and Decoder (fig. 1-4). When received data is applied to the TCU from the ADMS, the transmission line values are +6 volts for ones (mark) and −6 volts for zeros (spaces). These values must be converted to the +5 volt (one) and ground (zero) values used by the TCU logic. If a one is being transmitted, +6 volts is applied to input terminal 57 as TTLR-1, to the base of Transistor Q3 through Resistor R7. Q3 conducts, placing the base of transistor Q2 at ground. This turns off transistor Q2, thus placing the set level input 4(s) of FF 3 to approximately +5 volts, through resistor R5. This is a logical "one". If a zero (−6 volts) is applied to input terminal 57 as TTLR-1, the base of Transistor Q3 is at −0.8 volt. Thus transistor Q3 shuts off and a positive voltage is applied through Resistors R6, CR1 and R4, to the base of transistor Q2. Transistor Q2 conducts, placing a ground at the set level 4(s) input of FF3, which is a logical zero. In this case, therefore, the start bit causes the output (collector) of Q2 to be low and is applied to input 9 of OR 4B. Since input 8 and 7 of OR 4B are grounded, output 10 of OR 4B is high and is applied to the reset level input 7(R) of FF3. SRBC then gates this START into FF3. SRBC occurs at the negative transition of the beginning of BCRN. The actual loading of the START bit occurs at the end of Baud Count 0000. Thus at Baud Count 1 start is in the first stage of the Receive Buffer and Decoder.

c. Beginning with FF 3, the zero (9) output of each Buffer FF is connected to the reset level input 7 (R) of the adjoining FF, and the one (2) output of each Buffer FF is applied to the set level input 4(s) of the adjoining FF. In this way each application of SRBC to the pulse 5(T) inputs of the Buffer flip-flops loads a flip-flop with the contents of the preceding flip-flop. In this way the incoming character is serially loaded into the Buffer. Once input data reaches the buffer, it is further shifted to the TTY output device (printer or reperforator). The TCU sends levels of +5 volts (one) and ground (zero). The TTY output device accepts +6 volts (one) and −6 volts (zero). Thus the TCU includes a network to perform this level conversion. The data is applied from the receive buffer to terminal 24 as the PAPI (Punch and Printer Input) signal, and is extended through terminal 24 to terminal A2A7P1-46 of the Timing Generator (fig. 1-9). If the bit is a zero, a ground is applied through Resistor R18 to the base of Transistor Q7. This shuts off transistor Q7, placing a positive voltage (from the +12 volt dc supply through Resistor R20) at the junction of Diode CR6 and R22. The −12 volts through Resistor R21 places a negative voltage at the junction of CR6, R21, and R23. Zener diode CR6 breaks down and the voltage at the junction of CR6 and R13 is approximately −4V. The base of Transistor Q9 (an NPN) becomes positive with respect to the emitter through R23. This causes Q9 to conduct, placing the −6.2 volts (through R24) at PAPG, terminal 48. This is applied to the TTY output device. Also, the +12 volts is applied to Transistor Q8 through Resistors R20 and R22, making the base of Q8 positive with respect to the emitter. This shuts off Q8 (a PNP). If a one is to be transmitted, +5 volts is applied through R18 to the base of Q7, causing Q7 to conduct. The collector of Q7 is at ground. This makes the base of Q8 negative with respect to its emitter, and Q8 conducts placing the +6.2 volts on terminal 48, through R24 as PAPG which sends a one to the TTY output device. Also, −12 volts is applied through R21 and R23 to the base of Q9, making the base negative with respect to the emitter (which is connected to −6.2 volts). Q9 is thus shut off. Diode CR6 blocks the −12 volts from having a ground path. These levels which leave A2A7 (fig. 1-9) (PAPG, terminal 48; and PAPG-TR, pin 47) are applied to (fig. 1-21), logic card A2A1, Transmit Line Filter Driver. PAPG is applied to terminal 35 and PAPG-TR is applied to terminal 34. PAPG is then applied to the input of an emitter follower, the purpose of which is to provide filtering and wave shaping for RFI purposes. The output of the emitter follower is then applied to terminal 2 and extended through the Control Indicator Panel to the T and R Filter. From here the PAPI and PAPI-TR (return) signals are applied to the TTY output device.

d. At count 6 of the Receive Baud Counter (fig. 1-8), the START bit is in FF24 of the Receiver Buffer and Decoder (fig. 1-4). Also at count 6 of the Receive Baud Counter (fig. 1-8) (which has the state of 011 on, respectively, FF19, -18, and -17); the low zero (9) output of FF17 is applied to input 3 of OR 11A. The low zero (a) output of FF18 is applied to input 5 of OR 11A. The low one (2) output of FF19 is applied to input 4 of OR 11A. OR 11A now has complete input low coincidence; thus its output at 2 is low and is applied to input 9 of OR 12B. The low zero (9) output of FF20 is applied to input 8 of OR 12B. The low BCRN pulse is applied to input 7 of OR 12B. OR 12B now has complete input low coincidence; thus its output 10 is a low pulse which is SADA (Sample Data). In other words, when the TCU detects count 6 (011 in the Baud Counter), it knows a complete character has been shifted into the Receive Buffer and Decoder and that it can sample for this character.

e. Count 6 is applied also as a low signal to input 4 of OR 13A. The low zero (a) output of FF20 is applied to input 5 of OR 13A. BCRN places a low pulse on input 3 of OR 13A. Complete input low coincidence is now present on OR 13A, thus its 2 output is a high pulse which is applied to input 8 of OR 4B. Output 10 of OR 4B is a high pulse, which is applied to the direct reset input 3 (c) of FF14 (SP DETECT) clearing the flip-flop, and disabling shifting.

1-54. Receiving End-of-Message, Functional Analysis

a. The end of message sequence consists of 4 N's. Each time that the Receive Baud Counter and Decoder (fig. 1-8) reaches a condition where the mark count is zero, the baud count 6, the SP Detect level is received, FF20 (frequency divider) is set and the BCRN (Bit Clock Receive Negative) pulse arrives, a low EMCR (End-of-Message Receive Clock) pulse is extended to output terminal A2A6P1-12. This pulse is produced during every time 6 of the Baud counter and signifies an incoming character has been loaded into the Receiver Buffer (fig. 1-4).

b. The N Count (fig. 1-6), which consists of FF19, -20, and -18 is cleared to all zeros by initial PWRC. A level, DENR (Decode N's Receive), is applied through input terminal A2A4P1-18 to pin 5 of AND 8A each time an N is received in the Receive Buffer. When 4 consecutive N's are received, the TCU detects that the Receive EOM (End-of-Message) sequence has arrived. Each N which arrives as part of the message body will increment the N counter at EMCR.

c. Each time an N arrives during the course of a message, input 5 of AND 8A goes high. As long as FF 18 is reset its high zero (a) output is applied to input 4 of AND 8A. Input 3 of AND 8A is high as long as a stop character is not being sent. Output 2 of AND 8A goes high and is applied to input 3 of OR 13A. Output 2 of OR 13A is low and is applied to input 7 of OR 14B. Input 8 of OR 14B is grounded. Input 9 of OR 14B goes low each time EMCR arrives. Output 10 of OR 14B becomes a high pulse (each time EMCR arrives) and is applied to the pulse T(5) input of FF 19, the least significant stage of the counter. The reset 7(R) and set 4(s) level inputs of the counter (FF 19, -20, and -18) are connected to +5 volts so that once FF 19 is pulsed, counting begins. If the next character is not an N (as detected by EMCR) the counter will clear (*d* below). In this way it requires four successive message N's to reach the EOM state; thus EOM cannot be inadvertently reached.

d. Assume that during the course of receiving the body of a message one N′ has been loaded into the N counter. EMCR will be applied as a low pulse to input 4 of OR 14A. The low one (2) output of FF 18 is applied to input 5 of OR 14A. The absence of an N causes the 2 output of AND 8A to be low. Output 2 of OR 13A is high and the output 10 of OR 13B is low. The input 3 of OR 14A is thus low causing output 2 of OR 14A to be high. This is applied to input 5 of OR 6A, causing output 2 of OR 6A to be high. This clears the counter.

e. When 4 successive N's enter the TCU, the counter is in condition 4 (001). The high one (2) output of FF18 is applied to input 5 of OR 14A preventing the counter from clearing, and to output terminal A2A4P1-19 as the EOMR (End of Message Received) level. EOMR is applied to the Output Device Control Circuit on input terminal A2A5P1-40 (fig. 1-7). EOMR is a high level and is applied to input 7 of AND 2B. Input 9 of AND 2B goes high when the Mark Counter reaches 4, producing PAPD (Punch and Printer Disable). Input 8 of AND 2B goes high when SPDR of the Control Sequence (following EOM) arrives. Output 10 of AND 2B is high and is applied to input 8 of OR 7B. Output 10 of OR 7B, which is high, is applied to input 7 of OR 12B. Output 10 of OR 12B becomes low and is applied to input 5 or OR 12A, which operates with OR 12B as a flip-flop. Input 3 of OR 12A is grounded. Assuming that at this time no control sequences are being received (start, ack 1, ack 2, Rep, or Stop) all inputs to OR's 1A and 1B are low causing output 2 of OR 1A to be low which causes input 4 of OR 12A to be low. Output 2 of OR 12A becomes high and is applied to input 8 of OR 12B locking the flip-flop (OR's 12A and 12B) in this state even after PAPD is disabled. The high 2 output of OR 12A is also applied on output terminal A2A5P1-20 as the BLDR (Blind Receiver) signal. The significance of this is to blind the receiver (TTY device) from receiving characters when in the EOM state and CLEP has been received.

f. BLDR is applied as a high level to input terminal A2A2P1-54 of the Receive Buffer Decoder circuit (fig. 1-4). From here it is applied to input 3 of OR 5A. Output 2 goes high and is applied to input 9 of OR 5B. Output 10 of OR 5B becomes high and is applied to the direct set 3 (P) input of FF25, setting it. This applies a continuous mark to the receiving TTY device until BLDR is removed.

g. Since the ADMS (transmitter) follows its transmission of EOM with transmission of a Repeat, the TCU must provide an acknowledge. When the cancel was first sent to the TCU at the beginning of the current operation, CARP-2 (Cancel Receive Pulse) was applied to input terminal A2A5P1-41 (fig. 1-7) and to input 4 of OR 16A which operates with OR 16B as the POWER ON flip-flop. Output 2 of OR 16A became low and was applied to input 9 of OR 16B. Since, at the time cancel was received, no other control sequence was being received, a low level was applied to input 3 of AND 2A. The low 2 output of AND 2A was applied to input 7 of OR 16B. The low disabled PWRC level was applied to input 8 of OR 16B. Output 10 of OR 16B became high and was applied to input 3 of OR 16A, locking the POWER ON flip-flop in this condition despite the fact that CARP-2 became disabled. (The PWRC had originally set this FF and CARP as shown, above had cleared it.) This is the present condition of the POWER ON flip-flop.

h. The low output 2 of OR 16A is applied to input 9 of OR 17B. The fact that the INTER MESSAGE flip-flop is set (by EOMR), places a low level on input 8 of OR 17B. Once the Repeat Control character is received by the TCU, and decoded, RERP (Repeat Receive Pulse) is applied through input terminal A2A4P1-37 (fig. 1-6) as a high pulse to input 3 of OR 1A. Output 2 of OR 1A is low and is routed to output terminal A2A4P1-38 as the disabled RRPN (Repeat Received Pulse Not) signal.

i. RRPN is applied to input terminal A2A5 P1-11 of the Output Device Control circuit (fig. 1-7). From here, RRPN is applied to input 7 of OR 17B. OR 17B now has complete input low coincidence; thus, output 10 of OR 17B goes high and is applied to input 8 of AND 18B. Input 9 of AND 18B is high due to presence of EMRD (End-of-Message Received Delay) which is a normal operating condition. Output 10 of AND 18B goes high and is applied to input 3 of OR 17A. Output 2 of OR 17A becomes low and is applied to input 9 of OR 13B. Input 7 of OR 13B is low since presumbly at this time, the output TTY device is not operating abnormally. Input 8 of OR 13B is low since SMRT is open. Output 10 of OR 13B becomes high and is applied to output terminal A2A5P1-12 of this logic card as the high EMRP (End of Message Received Pulse).

j. EMRP is applied through input terminal A2A4P1-11 (fig. 1-6) to the pulse 5(T) input of FF 17, complementing the FF from its previous state. EMRP is also applied to input 7 of OR 12B. Output 10 of OR 12B becomes high and is extended to terminal A2A4P1-8 as the SDAK (Send Acknowledge) signal. SDAK in combination with the new state of FF 17 (AKOE or AKTE) initiates TCU transmission of either ACK-1 or ACK-2, acknowledging the received message. The actual generation of ACK is accomplished similarly to that of other control sequences.

k. At this point, the TCU is in condition to receive another message from the ADMS. During the intermessage state, when the repeat is received from the ADMS and the output device is not operating abnormally, output 10 of OR 1B is high and is applied to input 3 of AND 10A. If EMRD is true (the End-of-Message Received is not being used), input 5 of AND 10A is high. If the TCU has not sent a stop during the current message, input 4 of AND 10A is high. Output 2 of AND 10A is high and is applied to input 8 of OR 12B. Output 10 of OR 12B is high and is applied to terminal 8 as SDAK. This initiates TCU transmission of the appropriate acknowledge to the ADMS.

Section VI. ENQUIRY RESPONSE/DISCONNECT LOGIC

Note: Refer to note preceding paragraph 1-10.

1-55. Disconnect Line Logic Card (Enquiry Response/Disconnect Equipped TCU's Only) Functional Analysis

a. The TCU can operate with AUTOVON on a time-shared basis; that is, many TCU's share the same common line and as such, during extended idle periods, the TCU is disconnected from the ADMS. Once the TCU has not transmitted a message for 15 seconds, the disconnect signal is produced within the TCU. This prohibits the TCU from being able to start transmission of messages again until action is taken by the TCU through the disconnect logic system. When this is done, the carrier (work) on the lines between the TCU and ADMS, which was removed during disconnect, is applied again and by sending a manual cancel and receiving ACK-2 verification, message transmission can be restarted.

b. Refer to logic card A2A13, Disconnect Line (fig. 1-14). Once a transmitted message has been successfully completed (including receipt of correct acknowledge from the ADMS), the EMVP-1 (End-of-Message Verified Pulse) is applied to input terminal A2A13P1-26. From here it is applied to two places. First, it is applied to input 3 of OR 21A, which operates with OR 21B as an FF. Output 2 of OR 21A goes low and is applied to input 7 of OR 21B. Input 9 of OR 21B is low because PWRC is disabled. Input 8 of OR 21B is low because the 15 second timer is dormant; thus, its Q4 collector is low. Output 10 of OR 21B goes high and is applied to input 4 of OR 21A, locking the flip-flop in this condition, after EMVP is disabled. The low output 2 of OR 21A is applied through resistor R14 to the base of transistor Q7. This shuts off transistor Q7 placing the DISC (Disconnect) level (output terminal A2A13P1-56) in its high (approx +6 volts) not condition (DISC).

c. To summarize, the entrance of EMVP serves to reset flip-flop OR 21 and DISC from a previous timed-out operation. The high output of OR 21B is also applied to input 8 of AND 11B.

d. FMVP-1 is also applied to input 9 of OR 16B, which operates with OR 16A as a flip-flop. Output 10 of OR 16R goes low and is applied to input 4 of OR 16A. Input 5 of OR 16A is low because SSPW is disabled. As long as a start pulse detected transmit pulse is disabled, output 10 of AND 11B is low, which is applied to input 3 of OR 16A. Output 2 of OR 16A goes high and is applied to input 7 of OR 16B, locking the flip-flop in this condition, even after EMVP-1 becomes disabled. The low 10 output of OR 16B is applied through resistor R1 to transistor Q1, starting the 15-second timer. The starting of the 15-second timer occurs each time an EMVP-1 pulse (signifying the successful completion of a transmitted message) occurs. The low output 10 of OR 16B is applied through resistor R1 to the base of transistor Q1. The base goes negative with respect to the emitter due to the −6.2 volt supply through resistor R2. This shuts off Q1, removing ground through resistor R3 from the emitter of the unijunction Q2. Previously, the ground had been holding unijunction Q2 off and also had provided a path through resistor R3 to discharge capacitor C9. Refer now, to unijunction Q6. At some starting point when Q6 is shut off, the +9.3 volts flows through resistor R17 (pot), through resistor R12, and charges capacitor C11. Unijunction Q6 conducts at approximately one-half the source voltage or about 4.7 volts. Thus, in approximately one time constant (R17 x R12 x C11), the voltage across C11 is sufficiently positive to fire unijunction Q6. One time constant is approximately .023 second if R17 is set to about 18K. At this time, Q6 conducts, providing a positive pulse (about 4.7 volts in amplitude) through resistor R13 to the base of transistor Q3, causing Q3 to conduct for a few microseconds. This time depends upon how fast C11 discharges through L9 to ground. At this point Q6 shuts off and C11 begins to recharge. Thus, approximately every 0023 second, Q3 is on for a few microseconds. When Q3 conducts, a path is provided for the +9.3 volts through resistor R4 to ground. Once Q3 is off capacitors C10 and C9 start to charge through resistor R4 and diode CR1. The time constant of R4, C11 and C9 is

$(180)\ \frac{(.022)\,(27)}{.022+27} \times 10^{-6}$. The time constant is approximately 4 microseconds. The time required to place full charge across C10 and C9 is approximately 5 time constants, or 20 microseconds. Thus, in the time during which Q3 is off (0023 second), there is ample time for C10 and C9 to fully charge.

When C10 and C9 have fully charged, the voltage stored by each capacitor is in the inverse ratio of the capacitances, since the charge across each capacitance, which is the product of voltage and capacitance, remains constant. Thus when C10 and C9 are fully charged, there is approximately 9.293 volts across C10 and .007 volt across C9. At the end of the .023 second when Q3 conducts, a discharge path is provided for C10 through Diode CR2 to ground and C10 discharges very rapidly. Diode CR1, however, prevents C9 from discharging. Thus C9 holds its .007 volt. During the next .023 second, when Q3 is off, charging resumes but this time .007 volt is added to the .007 volt already across C9. Thus, in steps C9 charges toward 9.3 volts. At the threshold voltage for unijunction Q2 which is approximately half of 9.3 (4.7) Q2 will conduct. Therefore, once the voltage on C9 builds to approximately 4.7 volts, Q2 will conduct. In order to build from .007 volt to 4.7 volts, C9 has to charge in approximately 670 steps. Since the time between each charge is approximately .023 second in 670 steps, approximately 15 seconds is consumed.

e. This is the 15 second disconnect time out. The position of R17 is adjusted to provide a final time delay of close to 15 seconds. When this time (at 4.7 volts) is reached, Q2 conducts, discharging C9 and producing a short duration positive pulse. This is applied to the base of Transistor Q5 through Resistor R8, turning on Q5. This puts the collector of Q5 at ground and turns Q4 off. Previously the base of Q4 was at a positive voltage through R6 and R7, keeping Q4 on. Since Q4 is now off, a positive voltage is provided through Resistor R5 to input 8 of OR 21B.

f. Once unijunction Q2 starts to conduct, C9 discharges through Q2 and Resistor R9 to ground, turning off Q2. The high pulse applied to input 8 of OR 21B resets FF21, resulting in a high output 2 of OR 21A. Output 2 is applied through resistor R14 to the base of Transistor Q7, turning it on. Previously Q7 had been off by the −6.2 volts through Resistor R15. Once Q7 conducts a path is provided for the +6.2 volts through Resistor R16 to ground and the Collector of Q7 is grounded. This is the true state of the DISC signal, which is routed to output terminal 56 to the AA1 logic to halt transmission of messages to the ADMS.

g. If, at any time during the countdown, a message is to be transmitted, the SPDT (Space Pulse Detect Transmit) is applied as a high pulse to input terminal A2A13P1-24 and to input 7 of AND 11B. As previously described, input 8 of AND 11B is high. Output 10 of AND 11B goes high and is applied to input 3 of OR 16A, resetting the flip-flop (OR 16) from its previous state, and resulting in a high output 10 of OR 16B. This is applied through Resistor R1 to the base of Transistor Q1, turning Q1 on. This places the emitter of the unijunction oscillator through Resistor R3 to ground and enables any charge which was built up on Capacitor C9 to discharge through R3 to ground. This interrupts the 15 second timer, requiring it to start over at the next EMVP-1.

1-56. TCU Response to ADMS Enquiry Functional Analysis

a. When the ADMS sends an enquiry to the TCU (which it sends only to TCU's which are equipped with Enquiry Response/Disconnect interface logic cards A2A20, and A2A21), the TCU is required to send back to the ADMS, its routing indicator. The routing indicator varies for each enquiry response/disconnect connected TCU. The enquiry is received by the TCU in the form of a control sequence character. This is placed into the receive Buffer and decoded (fig. 1-4). This is sent to a figure 1-5 Receive Control Sequence, where two contiguous ENQR characters (sent to terminal A2A20P1-24) are converted to ENRP (Enquiry Receive Pulse). This pulse is generated similarly to that for other control characters except that in this case, FF22 and AND 23B are used. ENRP is applied to terminal A2A3P1-19 and extended to input terminal A2A3P1-24 of the Enquiry Response Sequence Generator Logic card (fig. 1-20). ENRP from here is applied to input 7 of OR 20B which operates with OR 20A as a FF. Output 10 of OR 20B goes low and is applied to input 4 of OR 20A. Input 3 of OR 20A is low since it is grounded. Input 4 of OR 15A is low since PWRC is disabled. Input 5 of OR 15A is low since it is grounded. As long as the output of OR 8B is high, which will be proven later, the input to OR 10B will be high. Output 10 of OR 10B is thus low. This is applied to input 3 of OR 15A. The output 2 of OR 15A is thus low. This results in the 2 output of OR 20A being high which is applied to input 9 of OR 20B. This locks the flip-flops (OR 20A and 20B) in this state, even though ENRP is disabled.

b. Earlier, the output of OR 10B was low. This could only be the case when the counter, consisting of flip-flops 24, 23, 22, and 21, which counts the enquiry response characters, as they are transmitted to the ADMS, are all ones (the counter was in its maximum count 15 during the end of a previous enquiry response operation). In this case the low zero (9) output of FF 24 is applied to input 9 of OR 8B. The low zero (9) output of FF 23 is applied to input 7 of OR 8B. The low zero (9) output of FF 22 is applied to input 8 of OR 15B. The low zero (9) output of FF 21 is applied to input 7 of OR 15B. Input 9 of OR 15B is low since it is grounded. The 10 output of OR 15B is thus low, and is applied to input 8 of OR 8B. OR 8B now has complete low input coincidence; thus, its 10 output is low and is applied to input 7 of OR 10B. Input 9 of OR 10B is low due to the fact that it is grounded. At the next time 6 Late (TSIL) of the Transmit Baud Counter, following the point at which the Enquiry Counter reached all ones, a low pulse is applied to input 8 of OR 10B, as the TSLN Time Six Late Not pulse. Output 10 of OR 10B becomes high and is applied to input 3 of OR 15A. Output 2 of OR 15A is high and is applied to the direct reset 8(c) input of FF 25, resetting it. The high output 2 of OR 15A is also applied to input 5 of OR 20A. This causes output 2 of OR 20A to be low which is applied to input 8 of 49 19B. Since FF 25 is now reset, the low one (2) output of FF 25 is applied to input 7 of OR 19B. Input 9 of OR 19B is low since it is grounded. Output 10 of OR 19B is thus high, and is applied to two places. First it is applied to the direct reset 8(c) inputs of flip-flops 22 and 21, resetting them. Second, it is applied to input 8 of OR 17B. Output 10 of OR 17B is high and is applied to the direct reset 8(c) inputs of flip-flops 24 and 23, resetting them. The counter is now cleared to all zeroes.

c. At this point, the output 10 of OR 8B becomes high, causing the output of OR 10B to go low (regardless of the status of TSIL pulse), supporting the original assumption. As previously described, once ENRP enters, the output of OR 20A is high. This is applied to the set level input 4(s) of FF 25.

d. Refer to logic card Transmit Start-Acknowledge sequence (fig. 1-13). When ENRP is produced it is applied to input terminal A2A11P1-49 of this logic card and to input 8 of OR 9B. Output 10 of OR 9B goes high and sets the START FLAG flip-flop 25. This initiates transmission of a start control sequence as described previously. When the transmission of the second character of the control sequence is about to be completed, CC2P (Control Character 2 Load Pulse) is applied to input terminal A2A11P1-51 of this logic card and eventually to input 4 of OR 18A. CC2P also clears the START FLAG flip-flop. Output 2 of OR 18A goes high and is applied out of this logic card on output terminal A2A11P1-47 as the SMFG pulse.

e. SMFG is applied via A2A20P1-26 (fig. 1-20). From here it is applied to the pulse input T(5) of FF25. FF25, which is set enabled, becomes set. The high one (2) output of FF25 is applied to input 3 of AND 16. As long as no control character is being transmitted, CONN is high and is applied to input 5 of AND 16A.

f. As previously mentioned, the ENQ counter (flip-flops 24, 23, 24, and 21) is cleared. During the forthcoming transmission of the enquiry response to the ADMS, the Enquiry Counter will be incremented as each character is transmitted. Each count of the enquiry character is decoded into a LOED level (Load Enquiry Device) which selects each character. This decoding is done by OR 2A, OR's 7A and 7B, OR 12A, OR 6A, OR 3A, OR 13A, OR's 4A and 4B, OR 3B, OR's 9B and 9A, and OR 8A. The particular decoding process will not be described each time the enquire counter is advanced. However, for the first count, all zeros, the decoding will be described in detail.

g. When the ENQ counter is cleared to all zeros, the low one (2) output of FF24 is applied to input 5 of OR 2A. The low one (2) output of FF23 is applied to input 3 of OR 2A. The low one (2) output of FF 22 is applied to input 7 of OR 2B. The low one (2) output of FF 21 is applied to input 9 of OR 2B. Input 8 of OR 2B is low since it is grounded. Output 10 of OR 2B goes low and is applied to input 4 of OR 2A. Output 2 of OR 2A goes low and is routed out of this logic card on output terminal A2A20P1-11 as the LOED-0 (Load Enquiry Device) -0 level.

h. Refer to logic card A2A21 Enquiry Response-Encoder (fig. 1-23). LOED-0 is applied via input terminal A2A21P1-12 to input 7 of OR 8B. Input 9 of OR 8B is low since it is grounded. Refer back to logic card A2A20 Enquiry Response Generator (fig. 1-20). At time T6 LATE (TSIL) of the Transmit Baud Counter, a high pulse is applied to input 4 of AND 16. Output 2 of AND 16 produces a high pulse which is applied to input 3 of OR 10A. Output 2 of OR 10A becomes low and sends a low pulse out of this logic card on output terminal A2A20P1-23 as the LOEN (Load Enquiry). LOEN is applied to input terminal A2A21-19 of the Enquiry Response-Encoder logic card (fig. 1-23), and from here, to input 8 of OR 8B. Output 10 of OR 8B now goes high and this is applied to input 4 of OR 22A. Output 2 of OR 22A is a high pulse and is applied to input 3 of OR 23A. Output 2 of OR 23A is high and is applied out of this logic card on output terminal A2A21-25 as the high TSEI-2 (Transmit Shift Enquiry Input 2) pulse. The high 10 output of OR 8B is also applied for input 9 of OR 22B. The high 10 output of OR 22B is also applied to input 9 of OR 24B. Output 10 of OR 24B is applied out of this logic card on output terminal A2A21P1-24 as the TSEI-3 pulse. Output 10 of OR 8B is also applied to input 7 of OR 20B. Output 10 of OR 20B is high and is applied to input 3 of OR 24A. Output 2 of OR 24A is high and is routed out of this logic card on output terminal 23 as the TSEI-4 pulse. Output 10 of OR 8B is also applied to input 4 of OR 20A. Output 2 of OR 20A goes high and is applied to input 9 of OR 25B. Output 10 of OR 25B is high and is sent out on output terminal A2A21P1-22 as the high TSEI-5 pulse. TSEI-2 through 5 are applied to the Character Store-Encoder logic card (fig., 1-19). From here the first enquiry response character is selected and loaded into the transmit Buffer (fig. 1-18). This process has been described previously in detail. From the Transmit Buffer, the character is shifted out to the ADMS. The first enquiry response character is a U and the U is decoded from TSEI-2 through 5 which in baudot is 01111.

i. Refer to logic card Enquiry Response Generator (fig. 1-20). As previously mentioned, when the 2 output of AND 16 generates a high pulse (at time T6 of the Transmit Baud Counter) the first enquiry character transmission is initiated. Also at this time a high pulse is applied to input 4 of OR 17A. Output 2 of OR 17A becomes high and is applied to input 5, the pulse (T) input of FF 24. This is the least significant stage of the enquiry counter. The set 4(s) and reset 7(R) level inputs of the four counter FF's are connected to +5 volts. Thus at the trailing edge of the high pulse (input to FF 24), when it starts to go negative, FF 24 is complemented to the 1 state. By this time the first enquiry character has been sent to the Transmit Buffer. This was done at the leading edge of the high pulse. Now that FF 24 is set, the counter is in count 1 (1000). This is decoded by OR 12A as the LOED-1 level. Note that the condition of FF 23 is not an input to OR 12A. The reason for this is shown later. LOED-1 is applied out of this logic card on output terminal 10 to input terminal 9 of logic card Enquiry Response Encoder (fig. 1-23). When the next Time 6 (TSIL) arrives, LOED-1 is encoded by OR 2A into TSEI-1 and into TSEI-5. This is applied eventually to the Transmit Buffer as upper case Z (baudot 10001) which is the second character of the Enquiry Response. The process for encoding of the LOED outputs from the Enquiry Response Generator (fig. 1-19) logic card has been described previously in detail for the first character (V) and it is not necessary to repeat this. However the encoding into TSEI pulses (which are in turn converted to baudot) is done by OR's 7A, 7B, 2B, 8B, 8A, 3B, 3A, 2A, 9A, 9B, 4B and 4A; which enable the final encoding from one of the LOED inputs; and by OR groups 23B, 16A, and 16B; 23A, 21A, 21B, and 22A; 24B, 17B, 17A, and 22B; 24A, 18B, 18A, and 20B; and 25B, 19B, 19A, and 20A; which, respectively select TSEI-1 through TSEI-5 from the LOED inputs.

j. At T Six, which as previously mentioned, transmits the second enquiry response character (Z), also, as previously described, increment the enquiry counter to count 2 (0100). This produces a high output at 2 of OR 7A. This is in turn applied to input 3 of OR 1A. Output 2 of OR 1A goes low and is the LOED-2 level. This is in turn encoded in the Enquiry Response Encoder logic card (fig. 1-23) into TSEI-2, -3, and -4 at T Six, which is baudot 01110, character C. T Six also advances the enquiry counter into count 3 (1100). At this time OR 12B, which was enabled during enquiry count 1, is again enabled, producing again LOED-1. Note that, as was the case during enquiry count 1, the condition of FF 23 is not applied to OR 12B. The reason for this is that LOED-1 must be generated twice, during enquiry counts 1 (1000) and 3 (1100); thus the condition of FF 23 is of no consequence. As described before, LOED-1 eventually transmits the fourth enquiry response character to the ADMS, which is another Z.

k. At T Six, when the transmission of the fourth character (Z) is initiated, the enquiry counter is advanced to count 4 (0010). At count 4 the fifth enquiry response character is to be transmitted and it is another C, which was also the third character transmitted, by LOED-2. Thus LOED-2 must again be produced. At enquiry count 4, OR 6B output 10 is low and applied to input 9 of OR 7B. Enquiry Count 4 enables the other inputs to OR 7B causing its 10 output to be high. This in turn causes the 2 output of OR 1A to be low, producing again, the LOED-2 pulse. Thus LOED-2 as with LOED-1 is generated twice. Two OR's (7A and 7B) however, are necessary in this case (as opposed to one gate, OR 12A, for two generations of LOED-1) since now two FF states change from a count 2 (0100) to a count 4 (0010), flip-flops 23 and 24. At T Six of the Transmit Baud Counter and the second LOED-2, the fifth enquiry response character, a second C, is generated and ultimately transmitted to the ADMS. To summarize the five enquiry response characters generated thus far have been VZCZC which, incidentally, are the same as the first five SOM characters. A summary of the operation thus far of the enquiry response is tabularized below:

Enquiry Count	*LOED*	*Character Sent*
0(0000)	0	V
1(1000)	1	Z
2(0100)	2	C
3(1100)	1	Z
4(0010)	2	C

l. The next group of enquiry response characters to be transmitted consist of from four to seven letters which are peculiar for a particular site and which are wired into the TCU during initial TCU installation. As the fifth character is transmitted, the enquiry counter is advanced to count 5 (1010) by T Six. Count 5 enables OR 6A negatively, producing at the 2 output, a low level, LOED-5. (Note that there is neither LOED 3 or LOED 4 since enquiry counts 3 and 4 generate LOED 1 and LOED 2, respectively.) LOED-5 is routed out of this logic card on output terminal A2A20 P1-9 to input terminal 16 of the Enquiry Response Encoder (fig. 1-23), to input 7 of OR 9B. At the following T Six, LOED is applied as a low pulse, to input 8 of OR 9B. The output 10 of OR 9B goes high and is applied to input terminal 1 of the WORD 1 jumpering board. Whichever pins (11, 12, 13, 14, or 15) terminal 1 is connected to, determines what the character will be, since a connection means that the corresponding TSEI signal will be generated. This is then transmitted as the sixth enquiry character to the ADMS.

m. Also, at T Six, the enquiry counter (fig. 1-20) advances to count 6 (0110). This enables OR 3A, producing LOED-6. LOED-6 in turn is applied to (fig. 1-23) input 7 of OR 3B. At the following T Six, the low LOEN pulse is applied to input 8 of OR 3B. The high output 10 of OR 3B is applied to terminal 2 of the WORD 2 jumpering Board. The connections to terminals 21, 22, 23, 24, or 25, select corresponding TSEI signals, which in turn, select the seventh enquiry response character. This character is then sent to the ADMS.

n. Also, at T Six, the enquiry counter is advanced to count 7 (1110) (fig. 1-20). This enables OR 13A, generating LOED-7. LOED-7 is then applied to input 7 of OR 7B (fig. 1-23). At T Six, the LOEN pulse causes a high 10 output of OR 7B to be applied to terminal 3 of the WORD 3 jumpering board. The connections from terminal 3 to terminals 31, 32, 33, 34, or 35 then select which TSEI's are generated. This results in the transmission of the eighth enquiry response character from the TCU to the ADMS.

o. Also, at T Six, the enquiry counter is advanced to count 8 (0001) (fig. 1-20). This enables OR 4A, generating LOED-8. LOED-8 is applied to input 5 of OR 7A in logic card A2A21 (fig. 1-23). At T Six, the LOEN pulse causes a high output of OR 7A to be applied to the input terminal of the WORD 4 jumpering board. The connections from this terminal to terminals 41, 42, 43, 44, or 45 then select which TSEI's are generated. This results in the transmission of the ninth enquiry response character from the TCU to the ADMS.

p. Also, at T Six, the enquiry counter is advanced to count 9(1001). At this point a decision is made. LOED 9 is generated (fig. 1-20) by the negative enabling of OR 4B. LOED 9 is connected (fig. 1-23) to input 3 of OR 3A and to terminal 4 of the jumper board located at the bottom center of this logic diagram. If the enquiry response sequence consists of VZCZC 4 letters, two carriage returns and a line feed, a connection has been made between terminal 4 and terminal C of the jumper board located at the bottom center of this logic diagram. The low LOED-9 signal is then applied out of this logic card on output terminal 21 as the ERAD (Enquiry Routing Advance) signal. ERAD is applied to input terminal A2A20P1-12 of logic card Enquiry Response Sequence Generator (fig. 1-20).

q. If the enquiry response consists of VZCZC, 5 letters, two carriage returns, and a line feed, terminal 4 of the jumper at the bottom center of (fig. 1-23) is not connected to the C terminal. In this case LOED 9 enables OR 3A the output of which in turn is applied to the input terminal of the word 5 jumper board. The appropriate connections to terminals 51, 52, 53, 54 or 55 then select TSEI signals which in turn select a character which is transmitted (at T Six) to the ADMS as the 10th enquiry response character. Also at T Six the enquiry counter is advanced to count 10 (0101). In this case count 10 enables OR 3B (fig. 1-20) which causes LOED 10 to be generated. LOED 10 is in turn applied to terminal 5 of the jumper board at the bottom center (fig. 1-23), which is in turn connected to terminal C. This causes the ERAD signal to be applied out of this logic card on output terminal A2 A21P1-21 to input terminal 12 of logic card Enquiry Response Sequence Generator (fig. 1-20).

r. If the enquiry response consists of VZCZC, 6 letters, two carriage returns and a line feed, terminal 5 (fig. 1-23) is not connected to the C terminal. In this case LOED 10 enables OR 9A the output of which in turn is applied to the input terminal of the WORD 6 jumpering board. The appropriate connections to terminals 61, 62, 63, 64 or 65 then select the TSEI signals which, in turn, select a character which is transmitted at T Six to the ADMS as the 11th enquiry response character. Also, at T Six the enquiry counter is advanced to count 11 (1101). In this case count 11 enables OR 9B (fig. 1-20), which in turn, causes LOED 11 to be generated. LOED 11 is in turn applied to terminal 6 of the jumper board (fig. 1-23) which in turn is connected to terminal C. This causes the ERAD signal to be applied out of the logic card on output terminal 21 to input terminal 12 of logic card Enquiry Response Generator (fig. 1-20).

s. If the enquiry response consists of VZCZC, 7 letters (which is the maximum number), 2 carriage returns, and a line feed, terminal 6 of the jumper board (fig. 1-23) is not connected to the C terminal. In this case LOED 11 enables OR 8A, the output of which is in turn applied to the input terminal of the WORD 7 jumpering board. The appropriate connections to terminals 71, 72, 73, 74 or 75 then select the TSEI signals which, in turn, select a character which is transmitted at the following T Six to the ADMS as the 12th enquiry response character. Also at T Six, the enquiry counter is advanced to count 12 (0011). In this case, the ERAD signal is not generated since terminal 7 of the jumper board at the bottom center is connected to +5 volts, disabling ERAD.

output of FF 24 is applied to input 9 of OR 18B.

t. Refer to logic card Enquiry Response sequence Generator (fig. 1-20). To summarize, if the number of letters in the variable portion of the enquiry response was four, ERAD was generated at LOED 9. If the number of letters in the variable portion of the enquiry response was five, ERAD was generated at LOED 10. If the number of letters in the variable portion of the enquiry response was six, ERAD was generated at LOED 11. If the number of letters the variable portion of the enquiry response was 7, ERAD was not generated.

u. If ERAD is generated, it is applied as a low pulse to input 3 of OR 18A. Inputs 4 and 5 of OR 18A are low since they are grounded. Output 2 of OR 18A is high and is applied to input 5 of OR 14A. Output 2 of OR 14A is thus low and is applied to input 4 of OR 19A. Input 5 of OR 19A is low since it is grounded. When the high speed clock (fig. 1-9) goes low, a low pulse is applied to input 3 of OR 19A. OR 19A for a short period has complete low input coincidence. Its 2 output thus goes high. This is applied to the direct set 3 (P) input of FF 22, setting it. The high 2 output of OR 19A is also applied to input 9 of OR 17B. The

10 output of OR 17B is high and is applied to the direct reset 8(C) input of flip-flops 24 and 23, clearing them. FF 21, which contained a one, is unaffected; thus, the counter now contains count 12 (0011). This means that regardless of whether the counter was in count 9, 10, or 11, it advances to count 12, provided that ERAD was generated. Once the counter reaches count 12, the low one (2) output of FF 24 is applied to input 9 of OR 18B. The low one (2) output of FF 23 is applied to input 8 of OR 18B. The low zero (9) output of FF 22 is applied to input 7 of OR 18B. Output 10 of OR 18B thus goes high and is applied to input 7 of OR 14B. Output 10 of OR 14B goes low and is applied to input 4 of OR 14A. Input 3 of OR 14A is low since it is grounded. Since ERAD is gone, input 3 of OR 18A is high. Output 2 of OR 18A is thus low. Output 2 of OR 14A is thus high. This locks the output 2 of OR 19A low, regardless of the high speed clock, thus stopping the counter. At this point, VZCZC and 4, 5, 6, or 7 letters of the enquiry response have been transmitted to the ADMS.

v. Once the enquiry counter is in count 12, OR 9A is enabled negatively, and generates LOED 12. LOED-12 is applied to A2A21P-20 (fig. 1-23), and to input 4 of OR 4A. At the following T Six of the Transmit Baud Counter, OR 4A is enabled and selects TSEI-4 (baudot 00010). This generates a carriage return character and transmits it to the ADMS.

w. Also at T Six, the enquiry counter is advanced to count 13 (1011) (fig. 1-20). This enables OR 9A (as during count 12) again generating LOED-12. LOED-12, as during count 12, generates a carriage return character (at T Six), transmitting it eventually to the ADMS. One more Enquiry response character is needed.

x. Also at T Six, the enquiry counter is advanced to count 14 (0111). Count 14 negatively enables OR 8A, whose output is LOED-14. LOED-14 is applied to input 7 of OR 2B through A2A21P1-8 (fig. 1-23) whose output then selects TSEI-2 (baudot 01000) at the following T Six. This is encoded in the Transmit Buffer section of the TCU as a line feed character, which is then transmitted to the ADMS as the final enquiry response character. A summary of the enquiry counter states, LOED's and characters are tabulated below.

Counter State	*LOED*	*Character Sent*
0(0000)	0	V
1(1000)	1	Z
2(0100)	2	C
3(1100)	1	Z
4(0010)	2	C
5(1010)	5	Letter
6(0110)	6	Letter
7(1110)	7	Letter
8(0001)	8	Letter
9(1001)	9	Letter*
10(0101)	10	Letter*
11(1101)	11	Letter*
12(0011)	12	Carriage return
13(1011)	12	Carriage return
14(0111)	14	Line feed

*If needed.

y. Also during T Six, the counter is advanced to its maximum count 15 (1111). This, as previously described, causes output 10 of OR 8B to A2A20 be low which is applied to input 7 OR 10B. Input 9 of OR 10B is low since it is grounded. At time T Six late not (TSLN) immediately following Time Six a low pulse is applied to input 8 of 10B. Output 10 of OR 10B produces a high pulse which is applied to input 3 of OR 15A. Output 2 of OR 15A is high, is applied to the direct reset 8(C) input of FF 25, and resets this FF, thus inhibiting the counting process until a future enquiry response is required by the ADMS. The high output 2 of OR 15A is also applied to input 5 of OR 20A, whose output 2 goes low. This is applied to input 8 of OR 19B. Input 9 of OR 19B is low since it is grounded. Since FF 25 is now reset, its low one (2) output is applied to input 7 of OR 19B. Output 10 of OR 19B goes high and this is applied to two places. First it is applied directly to the direct reset input 8(C) of flip-flops 22 and 21 of the enquiry counter, clearing them. The high 2 output of OR 19B is also applied to input 8 of OR 17B. Output 10 of OR 17B goes high. This is applied to the direct reset 8(C) input of FF's 24 and 23, which resets both these FF's. The enquiry counter is now cleared until the next enquiry response routing indicator is requested by the ADMS.

Section VII. CONTROL AND INDICATOR CIRCUITRY

1-57. Simulation Test Unit, Functional Analysis

a. This section describes in detail the operation of the various lamps and switches on the Simulation Test Panel. Figure 1-3 (sheets 1 through 6) contains the schematic for the panel. The MONITOR lamp and the ACKNOWLEDGE lamps (ACK-2T, ACK-1T, ACK-2R and ACK-1R) are lit when the associated conditions become true. All these lamps are connected to +12 at one terminal, and through a transistor (in the associated logic card) to ground when the corresponding function occurs.

b. The LAMP TEST Control is a press-to-test pushbutton. When it is pressed, +5 volts is connected through contacts 2 and 4 of the switch, through resistor R1 to transistors on the logic cards. From here the transistors provide ground paths through which the various Simulator Test Panel lamps, which are connected to +12 volts, are illuminated.

c. The ENABLE/DISABLE AUTOMATIC RT control is a toggle switch. In its ENABLE position, it applies ground through terminals 2 and 3, and esistor R2, producing SSPS, thus allowing automatic generation of RT. Also through switch terminals 5 and 6 and resistor R3, +5 volts produce the RTDS which also allows automatic generation of RT. If the switch is placed to the DISABLE position, SSPS and RTDS are placed to +5 volts and ground, respectively, through terminals 2 and 1, 5 and 4 of the switch. This disables automatic generation of RT.

d. In the position shown, MANUAL SYSTEM CLEAR is disabled. When power is first applied to the TCU, the SYSC signal is applied through contacts 1 and 2 of S5 and out, as PWRC (power clear), clearing all essential TCU elements. If it is desired to clear the TCU during operation, S5 is placed to the SYSC position. This causes +5 volts to be applied through contacts 3 and 2 of S5 out as PWRC. Filters R1-C1, R2-C2, R3-C3, and R4-C4 are used to reduce bounce noise caused by switch closures (S2, S3, and S5).

e. The REC (J4) and SEND (J5) jacks enable the input to and the output from the ADMS to be monitored during normal and abnormal TCU operations.

f. The SPEED SEL control is a rotary switch, actuated before operation begins, which allows the baud rate at which data is to be transmitted and received to be selected. The switch has three positions. In the 45.45 position, +9.3 volts is connected through contacts 6 and 12 to 7 and 1, respectively enabling the low 45.45 baud transmission and reception rates. In the 74.2 position, +9.3 volts is connected through contacts 6 through 12, to 8 and 2, respectively, enabling the MBD74.2 baud transmission and reception rates and on 9 and 3 for the high rate.

g. The CONT SEQ SIMULATOR control is a 3-deck rotary selector switch. It enables control sequences to be manually simulated, provided the TCU is in the test mode of operation. The selected control sequence is transmitted from the TCU; since in the TEST mode the TCU transmit section is connected back to the receive section, the selected control sequence is received by the TCU. The TCU logic then processes the control sequence which would normally be the reply (if any), transmits it, and receives it. For example, if the STOP control sequence is selected, STOP is transmitted and received, then, REPEAT is transmitted and received. This sequence will continue until the switch is placed to another position (OFF or another control sequence), or the TCU is taken out of the TEST.

h. The switch (S1) has two separate knobs: XMIT and RECEIVE. Positioning of the XMIT knob initiates the action described above, including the reception of the control sequence. The RECEIVE knob allows the reception of the control sequence (either that received as a direct result of the TRANSMIT switch position, or that received in reply) to be monitored by a lamp, when the RECEIVE knob is in one of the corresponding positions.

i. As figure 1-3 is viewed, sections 1 FRONT and 1 REAR of S1 are mechanically one switch that results in the transmission and reception of the control sequence. An example will best illustrate the TRANSMIT switch operation. Assume a START is selected. Normally, in the OFF position of the TRANSMIT switch, a ground is applied from pin 11 of J1 to pin 11 of S1 (SEC. 1 FRONT). This applies a ground through pin 8 of S1 to terminal 27 of J1 which is extended (fig. 1-13) as the disabled TSTT (TEST START) signal. Also in the OFF position, pin 8 of S1 (SEC. 1 REAR) is open, which keeps it disconnected from pin 1. Pin 1 is in turn connected to pin 12 J1, MSWE (MAINTENANCE SWITCH EN-

ABLE), which is connected to +5 volts through the TEST position of the mode switch on the Control Indicator Panel. When the TRANSMIT switch is placed to the START position, pin 8 of S1 SEC. 1 FRONT is disconnected from ground, and pin 8 of S1 SEC. 1 REAR is connected to +5 volts. This enables the TSTT signal, initiating the transmission of START.

j. As figure 1-3 is viewed, SEC. 2 REAR of S1 is physically one switch (RECEIVE) and results in the monitoring of the received control sequence. As an example, assume that the TRANSMIT switch has been placed in the START position. When the RECEIVE switch is placed in the START position pin 11 of S1 SEC. 2 REAR (normally grounded in the OFF position) becomes connected to pin 8. When the SARP (START RECEIVE PULSE) is generated by the TCU, as a result of receiving START, a high pulse is applied from pin 23, J1, through pins 8 and 11 of S1 SEC. 2 REAR, to pin 16, J1. This enables MSWR (Maintenance Switch Receive). MSWR is, in turn, extended through terminal 25 (fig. 1-4) to input 5 of FF OR15. This sets this FF. Q1 conducts and supplies a ground path to terminal 7, MCSI (Maintenance Control Switch Indicator). MCSI is extended to (fig. 1-3) terminal 1, J1 and results in the illumination of the MONITOR lamp.

1-58. Control Indicator Panel, Functional Analysis

a. This section describes in detail the operation of the various lamps and switches on the Control Indicator Panel. Figure 1-3 is the schematic for the panel. Switch S2 is a test switch for the audible alarm. When it is actuated, +12 volts is connected through its contacts to one terminal of the alarm, LS1. The other terminal is connected to −12 volts. The 24 volts then sound the alarm. During actual operation, LS1 sounds from the presence of AUDA (Audible Alarm which is extended from terminal 13, J1 as +12 volts). Potentiometer R4 allows the volume of the audible alarm to be adjusted when an actual alarm condition occurs during operation by varying the +12 volts from AUDA.

b. Switch S4 is the ALARM RESET switch for the audible alarm, LS1. When, during operation, the alarm sounds, actuation of S4 sends an alarm reset (ALAR) signal through pin 20, J1 back to the TCU logic, stopping the audible alarm. Resistor R10 and capacitor C3 are used for noise suppression.

c. DS15 and DS16 are, respectively, the message transmitted and message received indicators. When data is received or transmitted (or both) MREI or MSTI is extended through pin 18 or 14 of J1 and to the appropriate lamp (or both). This causes the lamp(s) to light.

d. Switch S10 is the LAMP TEST switch. When it is actuated, +5 volts is connected through one set of its terminals as the LPTE signal to the associated logic card providing a ground for certain Control Indicator Panel lamps (DS1, DS2, DS3, DS4, DS5, DS6, DS7, DS8, DS15 and DS16) which are connected at the other terminal to +12 volts, illuminating them. Other lamps on the Control Indicator Panel (DS9, DS10, DS11, DS12, DS13, DS14 and DS17) are illuminated directly through diodes CR3, CR4, CR5, CR6, CR7, CR8, and CR9. These diodes prevent any other than the affected lamp from lighting during actual operation. Resistor R21 and capacitor C9 are used for noise suppression.

e. When the STOP AT EOM switch (S1) is placed to the STOP at EOM position, EMRD (End-of-Message Receive Delay) is disabled (switched from +5 volts to ground) and EMRD-1 is enabled (switched from ground to an open position). Also, lamp DS14 STOP AT EOM is grounded, illuminating it. This prevents the end-of-message pulse from being received stopping message reception at the end of the message before the acknowledge is sent from the TCU. When S1 is placed to the CONTINUE position, EMRD is enabled, EMRD-1 is disabled, and message reception proceeds normally. Resistors R2 and R3 and capacitors C1 and C2 are used for noise suppression.

f. The position of S3 (a pull to operate 4PDT toggle switch), TCU/CRYPTO switch determines whether or not transmission of data is dependent upon the receipt of pulses from the crypto device. In the TCU position, the TCU does not require this pulse. In the CRYPTO position, this pulse is required. In the TCU position, pin 2 of S3 is connected to pin 3. This applies a ground to the TCU lamp (DS9) (the other terminal of which is connected to +12 volts), illuminating it. Pin 5 of S3 is connected to pin 6. This applies a ground to pin 61, J3 disabling TCUD (TCU DISABLE) which is used in the CRYPTO mode. Pin 11 of S3 is connected to pin 12, applying +5 volts to pins 4-1, 4-2 and 4-6 of S6, Mode Select switch. This simulates the CRST pulse (pin 14, J4) supplied by the CRYPTO during CRYPTO operation. The +5 volts is applied to pin 42, J3 as the simulated CRST-1 signal, allowing message transmission during TCU operation.

g. In the CRYPTO position, pine 2 of S3 is connected to pin 1. This applies a ground to pin 10, J1 which enables the CRSE (CRYPTO STEP ENABLE) signal for crypto operation. Pin 5 of S3 is connected to pin 4, applying +5 volts to pin 61 of J3, enabling the TCUD (TCU DISABLE) signal for crypto operation. Pin 11 is connected to pin 10. This connects J4, pin 14 to pins 4-1, 4-2 and 4-6 of S6. The crypto step pulse from the CRYPTO is appied to pin 14, J4. Through the switch S6 CRST becomes CRST-1 at J3, pin 42. This applies the crypto step pulse as required, throughout the TCU logic during CRYPTO operation.

h. Upon turn on of power, +5 volts is applied through normally closed pins 8 and 9 of Relay K1 and out to J1 pin 1 as SYSC (SYSTEM CLEAR) which is sent to the CONT SEQ SIMULATOR panel or the logic as PWRC, clearing all essential components. This lasts only momentarily for as soon as power is turned on, the +5 volts applied to Diode CR2 (a 13-volt Zener) causes CR2 to break down. This completes a path for the −12 volts and K1 energizes. R27 is used as a series limiting resistor, and diode CR1 is employed to suppress arcing of the contacts. When K1 energizes, the −5 volts is disconnected from pin 9 of K1 and ground is connected through pin 10 to pin 9 instead. This holds system clear low and disabled during operation (except when the TCU is manually cleared by operation of a Simulator Test Panel SYSTEM CLEAR switch. Also, K1 being energized causes ground to be connected through K1 pins 7 and 6 to lamp DS13, POWER ON, which illuminates while power is on.

i. Switch S5 is the TRANSMIT CANCEL switch. When it is depressed, +5 volts is sent through its contacts to pin 56 of J1 as the CAMA (Cancel Manual) signal. CAMA is then applied to Card A2A9 sending a cancel to the ADMS. Resistor R14 and Capacitor C5 are used for noise suppression.

j. Switch S7 is the START XMIT switch. When it is actuated, +5 volts is sent through its contacts to pin 29 and J1 as the SSSW (START XMIT) signal. This is applied to card A2A23, initiating the START SEND operation. Resistor R17 and Capacitor C6 are used for noise suppression.

k. Switch S8 is the TRANSMIT STOP AT EOM switch. When it is depressed, +5 volts is sent through its contacts to pin 30 of J1 as the EOMH (END-OF-MESSAGE HALT) signal. This is applied to card A2A23, initiating the TRANSMIT INTERRUPT operation. Resistor R18 and Capacitor C7 are used for noise suppression.

l. Switch S9 is the REQ MESS RT switch. When it is depressed, +5 volts is sent through its contacts to pin 31 of J1 as the SMRT (SEND MANUAL RETRANSMIT) signal. This initiates the manual retransmit operation. Resistor R19 and Capacitor C8 are used for noise suppression.

m. Switch S6, a push-to-turn rotary switch, determines in which of the three modes, NORMAL, TEST, or EMERGENCY, the TCU is to operate. In the test mode, the switch is in the position shown. Ground is connected to pin 3-9 providing a path through pin 4-7 to the test lamp DS10, lighting it. Also +5 volts is connected to pin 4-10 through pin 3-12 providing +5 volts enabling MSWE, which allows control characters, which are simulated, to be monitored. In the normal mode, ground is applied through pins (3-9) to (4-8) to DS11 normal lamp, illuminating the lamp. In the emergency mode, ground is applied through pins (3-9) to (4-9) to DS12, Emergency Lamp, lighting the lamp.

n. In the test mode, +5 volts is applied through R16 to S3 (pin 12 to 11) which is in the TCU position, to pin 42 of J3, simulating crypto step (CRST-1) for test purposes. Observe that the CRYPTO/TCU switch, S3, will not be in the CRYPTO position. Also, through pins (4-4) and (3-6) CLUP is connected to CLUP-1 (pin 47, J3 to pin 58, J3), allowing the clutch of the TTY input devices to be pulled for testing purposes as it is during NORMAL operation. In the normal mode, through pins (3-2) and 4-2) CRST-1 (pin 42, J3) is connected through S3 to CRST (pin 14, J4). In this way, data transfer depends upon either a pulse from the crypto, or simulated from the TCU depending upon the position of S3, TCU/CRYPTO switch. Also, through pins (4-5) and (3-6), CLUP is connected to CLUP-1, (pin 47, J3 to pin 58, J3), allowing the TTY input device clutch to be pulled in for normal data transfer operation. In the emergency position, through pins (3-6) and (4-6) CLUP-1 is connected to CRST (pin 58, J3 to pin 14, J4). This allows the CRST pulse to be simulated if S3 is in the crypto position. In either case the transmission lines are connected directly to the input TTY device, thus bypassing the TCU.

o. In the TEST mode, through pins (2-7) and (1-9) PAPI-1 is connected to PAPI-2 (pin 55, J3 to pin 2, J4), allowing the printer to operate for test purposes, as it does during NORMAL operation.

Also, through pins (2-10) and (1-12) DATI-1 is connected to DATI (pin 37, J3 to pin 10, J4) allowing input data to be received, as it is during normal operation. In the NORMAL mode, through pins (2-8) and (1-9) PAPI-2 is connected to PAPI-1 (pin 2, J4 to pin 55, J3), allowing the printer to be operated for normal data reception. Also, through pins (2-11) and (1-12) DATI-1 is connected to DATI (pin 37, J3 to pin 10, J4) allowing input data to be received. In the EMERGENCY mode, through pins (2-9) and (1-9) PAPI-2 is connected to TTLR, allowing incoming data to bypass the TCU, and go directly to the Output TTY device. Also through pins (2-12) and (1-12) DATI (pin 10, J4) is connected to pin (2-6). The purpose of this is described below.

p. In the TEST mode, through pins (1-3) and (2-1) TTLT-1 is connected to TTLR-1 (pin 50, J3 to pin 52, J3) connecting the TCU back to back for Test purposes by allowing outgoing data from the Transmit Buffer (by way of the Timing Generator A2A7) to enter the Receive Buffer. Also, through pin (2-4) connect through R15 to +5 volts at pin J-11 and (1-6) (pin, J4) TTLT-2 is +5V keeping a MARK on the outgoing lines, thus blinding the distant station during testing. In the NORMAL mode, through pins (1-6) and (2-5) TTLT-2 is connected to TTLT-1 (pin 4, J1 to pin 50, J3) enabling data to be transmitted normally. Also, through pins (2-2) and (1-3) TTLR is connected to TTLR-1 (pin 8, J4 to pin 51, J3) enabling data to be received normally. In the EMERGENCY mode, through pins (1-12) and (2-12) DATI and pins (2-6) and (1-6) are connected to TTLT-2 (pin 4, J4), allowing data to be sent directly from the TTY input device to the distant station bypassing the TCU.

q. Switch S15 when in the position shown (grounded), disables messages from being manually numbered, by applying ground through terminal 46 of J1 to card A2A16. When S15 is depressed, +5 volts is connected through its contacts, to enable MENS (Message Numbering Switch), thus allowing messages to be manually numbered. Resistor R24 and Capacitor C19 are used for noise suppression.

r. Switch S14 enables or disables message numbering. Normally, message numbering is done during the transmission of messages. The switch is normally in the position shown and ground disables MEND (Message Numbering Disable) through pin 45 of J1 to A2A16. When the switch is depressed, +5 volts is applied through the switch contacts, producing MEND, disabling message numbering. Also, the ground is applied to pin 2 of lamp DS17, removing the shunting Resistor R23 and illuminating D17. Resistor R22 and Capacitor C10 are used for noise suppression.

s. Switches S13, S12, and S11 are two deck, 10 position, rotary switches, each of which is numbered from zero to nine. Refer to the hundred select switch S11. (The 10's select, S12, and the units select, S13, operate the same as S11 and will not be described in detail.) Once a decimal number from 0 to 9 is set up on S11, S11 provides the corresponding binary representation of that decimal output. These are the SND (Select Number Deck) signals. That is, if number 9 is selected, SND A-3 becomes ground (zero), SND B-3 becomes open (which to the input of an associated AND gate in the TCU Message Identifier Sequence Generator appear as a one), SND C-3 becomes ground (zero), and SND D-3 becomes open (one). This provides a binary array of 1001 (decimal nine), to respectively terminate 40, 39, 38, and 37 of J1 and extended to card A2A15. Once S11, S12, and S13 are set up to the desired preselected message number, operation of S15 places this number in the TCU Message Identifier Sequence Generator number Register. At this point, the Message Identifier Sequence Generator generates MIN (Message Indicator Numbering) outputs, also in binary, corresponding to the selected 3 decimal numbers. These signals are routed back to the Control Indicator Panel. From here, the signals are applied to three sets of nixie tubes, and converted to a digital readout from 0 to 9. The readout is provided through three windows on the Control Indicator Panel. In addition, even if message numbering has not been manually preselected, the normal automatic numbering (and advance thereof after each transmitted message) is displayed at these windows, as decoded by the nixie tubes.

Section VIII. ABNORMAL CONDITION OPERATION

NOTE

Refer to note preceding paragraph 1-10.

1-59. Alarm Conditions

a. Certain abnormal TCU conditions result in the generation of an audible and visual alarm. The result of one of these alarm conditions will be described first, followed by a detailed explanation of the various causes of the alarm condition.

b. Refer to Character Store Encoder (fig. 1-19). When any of the following trouble conditions is present (they are high signals) the Alarm Sent (ALAS) is generated.

(1) AIOA—Input or Output Abnormal Device
(2) RTSA—Retransmit Send Alarm
(3) RTRA—Retransmit Receive Alarm
(4) REPA—Repeat Alarm
(5) TEMA—Transmit End-of-Message Alarm
(6) REMA—Receive End-of-Message Alarm

c. When AIOA occurs, it is applied to input terminal A2A19P1-58. From here it is applied to two places. First, it is applied through resistor R9 and through the network comprised of C17, C16 and diode CR6, to input 8 of OR 24B. Capacitor C17 and R9 integrate the level change felt at the junction of R9 and C17. Capacitor C16 couples this change to input 8 of OR gate 24B. Diode CR6 clips any negative peaks. By integrating input signals, false alarms at the time of power turn on are prevented since the alarm condition is cleared before OR gate 24B is activated. Output 10 of OR 24B is applied to input 3 of OR 23A. Output 2 of OR 23A is applied to input 8 of OR 18B, which operates with OR18A as an FF. Output 10 of OR 18B goes low and is applied to input 4 of OR 18A. Input 3 of OR 18A is low because PWRC is disabled. Input 5 of OR 18A is low because of the alarm reset switch (S4) is disabled. Output 2 of OR 18A goes high and is applied to input 9 of OR 18B, locking the FF in this condition, even after the alarm signal becomes disabled. Output 10 of OR 18B is low and is routed to output terminal 11 as the ALAS (Alarm Sent) signal.

d. AIOA is also applied to input 7 of OR 23B. Output 10 of OR 23B is applied through resistor R3 to the base of transistor Q1. Transistor Q1 conducts and provides a return (ground) for the Control and Indicator Panel ALARM lamp, the other end of which is connected to +12 volts. This illuminates the lamp. Prior to the conduction of Q1, R1 provided a high resistance to the lamp to keep its filaments hot and extend bulb life. Due to the high resistance of R1, the lamp will appear extinguished.

e. RTSA, RTRP, REPA, TEMA, and REMA also generate ALAS and illuminate the ALARM lamp, except that the input gating is comprised of different logic elements. The following table shows the particular logic elements which are associated with each of the above other alarm conditions. Note that some alarm signals have the same logic element.

Alarm signal	Filter components	Signal or-	Lamp or-
RTSA	R7, C13, C12, CR4.	24A, pin 5	25B, pin 8.
RTRP	R8, C15, C14, CR5.	24B, pin 7	25B, pin 9.
REPA	R6, C11, C10, CR3.	24A, pin 3	25B, pin 7.
TEMA	R5, C9, C8, CR2	23A, pin 5	25A, pin 4.
REMA	R4, C7, C6, CR1	23A, pin 4	25A, pin 3.

f. ALAS is applied to input terminal 50 of logic card A2A14 Input Device Control (fig. 1-15). From here, it is applied to input 3 of OR 18A. Input 4 of OR 18A is low because it is grounded. When the reply timer FF20 is in the reset state (every ¼ to ½ second), its low one (2) output is applied to input 5 of OR 18A. Every ¼ to ½ second output 2 of OR 18A goes high (for from ¼ to ½ second). This alternating high level is applied to through resistor R4, diode CR1, and resistor R5 to ground. This causes Q2 to conduct, placing the base of Transistor Q3 through resistor R7 to ground. This causes Transistor Q3 to conduct providing a low resistance path from +12 volts to the Indicator and Control Panel audible alarm, the other end of which is connected to −12 volts. This results in the periodic sounding of the audible alarm.

g. The details of events which cause each of the alarm conditions to occur are described in *h* through *o* below.

h. For AIOA, refer to logic card A2A11 Transmit Start-Acknowledge Sequence (fig. 1-13). When the input TTY device is operating abnormally, a high signal is applied to input terminal A2A11P1-58 from the device. From here, ABNI is applied through Resistor R9 to the base of Transistor Q3. Transistor A3 conducts, placing the base of Transistor Q4 at ground. Transistor Q4 shuts off, causing a positive voltage to be placed at the collector of Q4 through Resistor R7. This is applied to output terminal A2A11P1-21 as the high ABNI-1 signal. This is sent to A2A14 (fig. 1-15) and causes the TTY clutch to be disabled. It is also applied to illuminate the INPUT indicator lamp on the Control and Indicator Panel. ABNI (fig. 1-13) is also applied to input 3 of AND 21A from Q4. If a precedence character has been checked and stored, input 5 of AND 21A is high. Output 2 of AND 21A goes high and is applied to input 3 of OR 16A which disables AND 19A. The output of OR 21A is also applied to input 3 of OR 9A. Output 2 of OR 9A is applied to input 4 of OR 20, setting the START FLOP (OR 20). This sets the START FLAG flip-flop FF25 through OR 9B. The one output of FF25 is applied to input 9 of AND 19B. The START is inhibited however from being transmitted until NABN goes high after the ABNI is removed.

i. Output 2 of AND 21A, GIAB (Gated Input Abnormal) is applied from terminal 7 to input terminal A2A14P1-53 of logic card, Input Device Control (fig. 1-15). From here it is applied to input 5 of OR 4A. Output 2 of OR 4A goes high and is applied to output terminal A2A14P1-21 as the AIOA (Abnormal Input or Output Device) signal.

j. Refer to logic card Receive-End-of-Message (fig. 1-6). If the output TTY device is operating abnormally, a high signal (ABNO) is applied to input terminal A2A4P1-58. From here the high signal is applied to the base of Transistor Q3. Q3 conducts, causing a ground to be placed at the base of Transistor Q2. Q2 shuts off, causing a positive voltage to be placed at its collector through resistor R5. This is the ABNO-1 (Abnormal Output device) signal and it is applied to output terminal A2A4P1-42. ABNO also causes the abnormal output device lamp, located on the Control and Indicator Panel, to light. ABNO-1 is applied to input terminal 20 of logic card A2A14 Input Device Control (fig. 1-15). From here ABNO-1 is applied to input 4 of OR 4A. Output 2 of OR 4A goes high and is applied to output terminal A2A14P1-21 as the AIOA (Abnormal Input or Output Device) signal. To summarize, either ABNI or ABNO will produce AIOA which is one of the alarm conditions.

k. RTSA. Refer to (fig. 1-12). Whenever the retransmit control sequence is automatically generated by the TCU, the high one (2) output of FF20, AUTO RT SENT, is applied to output terminal A2A10-24 as the RTSA (Retransmit sent alarm) signal. Also, the high output of FF20 lights the Control and Indicator Panel AUTO MES RT indicator lamp.

l. RTRP. Refer to A2A3 (fig. 1-5). When a retransmit receive control sequence is received from the ADMS, the RTRP (retransmit Receive Pulse) is sent to input terminal A2A19P1-26.

m. REPA. Refer to (fig. 1-12). Whenever a count of three is in the repeat counter (flip-flops 23 and 22) is reached (due to three repeats or three cancels), an alarm condition exists. This condition causes the output 10 of AND 21B to be high, which is applied out of this logic card on output Terminal A2A10P1-46 as the REPA (Repeat Alarm) condition. Also REPA causes the Control and Indication Panel Repeat Alarm indicator lamp to light.

n. TEMA. Refer to A2A14 (fig. 1-5). If it is desired to manually stop transmission of messages, the operator depresses the Control and Indicator Panel Transmit Stop at EOM switch. In this way, the current message will be completed, then message transmission will stop. Operation of this switch causes a momentary high level (EOMH) to be applied to input terminal A2A14P1-33. This is applied to input 7 of OR 16B, which operates with OR 16A as a flip-flop. Output 10 of OR 16B goes low and is applied to input 3 of OR16A. Input 5 of OR16A is low because it is grounded. Input 4 of OR 16A is low because SSSW (the Control and Indicator Panel start send switch) is off. Output 2 of OR16A goes high and is applied to input 8 of OR16B, locking the flip-flop in this condition, even after EOM stop is disabled. The high 2 output of OR16A is applied to the set level input 4 (S) of the TRANS HALT flip-flop FF17. When EOMS state is reached, it is applied to the pulse input 5 (T) of FF17, setting the flip-flop. The high one (2) output of FF17 is applied to output terminal A2A14P1-6 as the TEMA signal. The high output 2 of OR16A also causes the Control and Indicator Panel TRHI (Trans halt Indicator) to light. Note that later, when the SSSW (Start send switch) is operated (generating SSPW), the flip-flop (OR 16) is reset, clearing FF17 and removing the set level input.

o. REMA. Refer to A2A5 (fig. 1-7). When the operator wishes to manually transmit a stop control sequence, he causes the inhibiting of the End-of-Message Receive Pulse. This has been previously described. This is done by generating GEMD (Gated End-of-Message Delay). GEMD (a high signal) is also applied to input 9 of OR 23B, which operates with OR 23A as a flip-flop. Output 10 of OR 23B is applied as a low signal to input 5 of OR 23A. Input 4 of OR 23A is low because PWRC is disabled. Input 3 of OR 23A is low since EMRD (End-of-Message Received delay) has been disabled by operation of the EOM delay switch. Output 2 of OR 23A goes high and is applied to input 7 of OR 23B, locking the flip-flop in this condition, even after ERMD-1 becomes disabled. The high 2 output of OR 23A is applied to output terminal 47 as REMA (Received EOM Alarm).

1-60. Abnormal Responses to Repeat, Functional Analysis

a. When the TCU has transmitted its message, and has transmitted Repeat, the ADMS replies with its last response which can be—

(1) ACK-1 or ACK-2 (if the message has been successfully received).

(2) STOP if, for instance, the receiving hand copy device (or reperforating device) is temporarily out of paper or tape and cannot receive subsequent data until this condition is alleviated.

(3) Also if during transmission of a message, the ADMS sends a stop, the TCU sends a repeat and ADMS sends an RT. This indicates that the ADMS has not successfully received the message and desires to have it retransmitted.

b. Whenever the reply to repeat is Retransmit (RT), the RT is first preceded by a stop. This halts operation of the TCU in preparation for the retransmission. After the retransmit control sequence has been received, the TCU is not operating, and the tape reader has been reloaded with the message to be transmitted, the TCU sends a cancel which directs the ADMS to scrap the previous message and which reachieves acknowledge synchronization on the lines. The ADMS is required then to send an ACK-2.

c. When a stop is received by the TCU it is placed in the Receive Buffer and decoded into STPR (Stop Receive). Two of these are required to obtain the Stop Receive pulse (STRP) which signifies that the control sequence has been fully received. The generation of STRP is similar to that of other receive control sequences (fig. 1-5) except that FF12 and AND 16A are used in conjunction with STOP. This process is described in paragraph 1-32. Ultimately, STRP is routed out of this card on output terminal A2A3P1-7. STRP is applied to input terminal A2A10P1-15 of the Transmit Repeat-Retransmit Sequence circuit (fig. 1-12). It is applied as a high level to input 9 of OR 4B. Output 10 of OR 4B is high and is applied to three places as follows:

(1) To input 7 of OR 3B. Output 10 of OR 3B is high and through OR 2A, resets the repeat counter (FF's 23 and 22) to all zeroes.

(2) To input 4 of AND 8A. Input 3 of AND 8A is high since, at this time, a cancel is not being transmitted (CANN is true). Output 2 of AND 8A goes high, and is applied to input 7 of the REP FF (which consists of ORS 16A and 16B), setting this FF thus enabling automatic generation of the repeat control sequence.

(3) To input 5 of OR 10A, which operates with OR 10B or the STOP RCVD flip-flop. Output 2 of OR 10A goes low and is applied to input 7 of OR 10B. Input 8 of OR 10B is low since it is grounded. Since neither ACKV (ACK verified) nor PWRC are present inputs 5 and 4, respectively, of OR 9A are low. Input 3 of OR 9A is grounded. Thus output 2 of OR 9A is low and is applied to input 9 of OR 10B. OR 10B now has complete input low coincidence, thus its output 10 is high. This is applied to input 4 of OR 10A, locking the flip-flop in this state even after STRP is disabled.

d. The high 10 output of OR 10B is also applied to input 7 of OR 15B. The high output 10 of OR 15B is extended to output terminal A2A10P1-47 as the SRRC (Stop received alarm) level. SRRC disables the input TTY device from transmitting anything further to the TCU until the current situation is corrected.

e. Output 10 of OR 10B is also applied to input 9 of AND 7B. Each time FF20 of the Input Device Control (fig. 1-15) enters the one state (every $\frac{1}{4}$ to $\frac{1}{2}$ second), its high one (2) output is applied through output terminal A2A14P1-56 as the LMPF (Lamp Flash) signal to input terminal A2A10P1-45 (fig. 1-12), to input 8 of AND 7B. Thus every $\frac{1}{4}$ to $\frac{1}{2}$ second, output 10 of AND 7B goes high and is applied to the base of Q2 through the voltage divider consisting of Resistors R7 and R8. This results in flashing of the Control and Indicator Panel STOP RCVD lamp.

f. When CSSP enters input 4 of AND 21A is high. Input 5 of AND 21A is high since FF OR 16 is set. Input 3 of AND 21A is high since the rep counter is cleared. The high 2 output of AND 21A sets FF 24, sending a repeat to the ADMS. This time the response from the ADMS should cause RTRP (Retransmit Pulse) to be generated. This control character is received and converted into the RTRP in the Receive Control sequences circuit (fig. 1-5). Generation of RTRP is similar to that of other receive control sequence pulses, except that FF 17 and AND 16B are used for retransmit. RTRP is applied out of this logic card on output terminal A2A3P1-8.

g. RTRP is applied through input terminal A2A10P1-12 (fig. 1-12) to input 7 of OR 2B. Output 10 of OR 2B is high and is applied to input 5 of AND 7A. Input 4 of AND 7A is high since FF OR 10 is set. Output 2 of AND 7A is high and through OR 9B, resets the REP FF OR 16. RTRP is also applied through OR 3A and OR 2A to clear the REP counter.

h. RTRP is also applied through input terminal A2A9P1-12, to input 3 of OR 3 (CNCL FLOP) of the Transmit Cancel-Stop Sequence, circuit (fig. 1-11). This causes output 2 of OR 3 to go low. This is applied to input 9 of OR 8B. Input 7 of OR 8B is low since ACK-2 is not being received. Input 8 of OR 8B is grounded. Output 10 of OR 8B goes high and is applied to input of OR 3. This locks the FF (comprised of OR 3 and OR 8B) in this condition even after RTRP is disabled. The low 2 output of OR 3 is applied to input 3 of OR 8A. Input 4 of OR 8A is low since REPA (Repeat Alarm) is not present. Input 5 of OR 8A is low since EOMS (End-of-Message Sent) is not present. Output 2 of OR 8A goes high and is applied to the set 4(S) input of the CNCL FLAG FF 12.

i. When CSSP is generated (pin 41) it is applied to input 4 of OR 17A. Output 2 of OR 17A is a high pulse and sets FF12 through the pulse 5(T) input. At this time, a cancel is transmitted to the ADMS. This tells the ADMS that the TCU agrees that the transmitted message was erroneous and must be repeated. The ADMS responds with ACK-2 to achieve ACK resynchronization. Next, the previous message is manually reloaded into the input TTY device in preparation for retransmission. After this is done, the initiation of message retransmission must be done manually sinc the TCU is still in the stop (halted) mode.

j. This is done by operation of the START SEND switch. SSSW is generated and applied to input terminal A2A9P1-11 (fig. 1-11). This resets

FF OR 11. This disables CANN. Since SRRC (A2A14P1-13) is also disabled (from the recent RTRP pulse) AND 12B (fig. 1-15) is enabled, setting FF 13 and restoring the TTY device at CLEP (from the Transmit Baud Counter). This causes the TCU to begin Searching for a precedence character, initiating the actual retransmission of the message.

k. In the case where the ADMS does not require a retransmission, it will keep sending stops to the TCU, followed alternately by Repeat from the TCU, until the ADMS either sends an acknowledgement (ACK-1 or ACK-2) for the message or does not acknowledge, causing other steps to be initiated to alleviate the problem.

l. Once the proper Acknowledge is received from the ADMS, the TCU is in condition to send a subsequent message which it does as soon as the next precedence character is received from the TTY input device. During the intermessage transmit state (the time between receipt of ACK response from the ADMS for the previous message and receipt of a precedence character for a subsequent message), the ADMS is blinded so that extraneous characters which may be on the TTY input device tape preceding the precedence character, are not sent to the ADMS.

1-61. Canceling In-Progress Transmitted Message by TCU, Functional Analysis

a. Due to certain abnormal conditions, the TCU may desire to cancel a message which it is sending to the ADMS during processing. This is initiated by the TCU operator using the Control Indicator Panel SEND CANCEL switch. This sends a high signal to input terminal 15 of A2A10 (fig. 1-12). This in turn initiates transmission of a cancel control sequence, interrupting the message. From this point the operation is the same as if the TCU had sent an initializing cancel. That is, the ADMS sends back an ACK-2, showing ACK synchronization. Then the TCU may resume transmitting that message (from the beginning); or may read a new message, depending upon the situation.

b. The logic description of this process is described in paragraph 1-29.

1-62. Transmission of Stop by TCU During Message by TCU, Functional Analysis

When the TCU is receiving a message from the ADMS, and adverse conditions occur at the TCU, the TCU sends a STOP control sequence to the ADMS. Depending upon the type of trouble, the TCU may either send the stop in the middle of the message, in which case the ADMS will be required to later retransmit the message: or the TCU may send the Stop at the end of the message in which case the TCU will eventually acknowledge (after the problem is corrected) or, if the message is bad, request retransmission.

1-63. Stop Transmitted While Receiving Message, Functional Analysis

a. The TCU interrupts the received message when the reset (MARK) intervals are not present. SADA (Sample Data) is generated and applied through input terminal A2A3P1-33 (fig. 1-5) to input 4 of OR 1A. RECN occurs at each Count 6 of the Receive Baud counter. When the Receive Buffer is filled with a character, and TTLR-2 is applied to input terminal A2A3P1-39, its level is present on input 9 of OR 1B. Since when RECN occurs, the TTLR should be a Mark (rest), if a space (low) is the condition of TTLR-2, there is an error condition. If the Simulator Panel Spacing stop switch is off (RT is enabled), a low level SSPS is present on input terminal A2A3P1-40 and from here, to input 7 of OR 1B. Output 10 of OR 1B goes high and is applied to input 4 of OR 15A. Output 2 of OR 15A goes high and is extended on output terminal A2A3P1-54 as the STOP signal.

b. STOP is applied through input terminal A2A9P1-20 of the Transmit Cancel-Stop Sequence (fig. 1-11) to the direct set 3(P) input of FF14, STOP COMMAND FLOP setting it. The one (2) high output of FF14 is applied to input 9 of OR7B. Output 10 of OR 7B is high and is applied to the set level input 4 (S) of FF 13, STOP FLAG. When the CCSP (Control Character Sync Pulse) occurs, it is applied through input terminal A2A9P1-41 to input 4 of OR 7A. Output 2 of OR 7A goes high and is applied to the pulse 5(T) input of FF13, setting it. The low zero (9) output of FF 13 is applied to input 7 of OR 6B. The low one (2) output of the CNCL FLAG FF 12 is applied to input 8 of OR 6B. (After the initial cancel was sent to the ADMS, FF 12 was reset. Input 9 of OR 6A goes low as soon as the CCLP (Control Character Load Pulse) is produced, at Baud Count T6 Late. Output 10 of OR 6B goes high and is applied to output terminal A2A9P1-18 as LSTP (Load Stop). LSTP is also applied to input 5 of OR 15A, which operates with OR 15B as a flip-flop. Output 2 of OR 15A goes low and is applied to input 9 of OR 15B. Input 8 of OR 15B is SDAK which is low. Input 7 of OR 15B is low because PWRC is disabled. Output 10 of OR 15B goes high and is applied to input 4 of OR 15A, locking the flip-flop in this condition, even after LSTP becomes disabled. The high output 10 of OR 15B is extended to output terminal A2A9P1-26 as the STPS (Stop Sent) level.

c. LSTP ultimately loads the first half of the Stop control sequence into the Transmit Buffer and later the second character is transmitted, completing the transmission of the STOP to the ADMS. STPS is applied through input terminal A2A4P1-40 of the Receive-End-of-Message circuit (fig. 1-6) to input 3 of AND 2A. Input 4 of AND 2A is high, because EMRD (End-of-Message Receive Delay) from the Control Panel is enabled. The output device (TTY) is presumably not abnormal, thus a low level is applied to input 7 of OR 1B. Input 9 of OR 1B is grounded.

d. In answer to the TCU STOP, the ADMS sends a Repeat Control sequence which requests that the TCU send its last (final) response. When the TCU receives the repeat, RERP (Repeat receive pulse) is applied to input terminal A2A4P1-37, as a high pulse, which is applied to input 3 of OR 1A. Output 2 of OR 1A goes low and is applied to input 8 of OR 1B. Output 10 of OR 1B goes high and is applied to input 5 of AND 2A. Output 2 of AND 2A goes high and is applied to output terminal A2A4P1-41 as the high SRTP (Send Retransmit) pulse.

e. SRTP is applied also through input terminal A2A10P1-38 (fig. 1-12) to input 8 of OR 1B Output 10 of OR 1B goes high and is applied to input 7 of OR 6B. Output 10 of OR 6B, which operates with OR 6A as the RT flip-flop, goes low and is applied to input 4 of OR 6A. Inputs 3, 4, and 5 of OR 1A are low, and output 2 of OR 1A is low and is applied to input 5 of OR 6A. Currently FF 18, RT FLAG, is reset; thus, its high zero (a) output is applied to input 7 of OR 14, the RT PRIORITY GATE. Output 2 of OR 14 is low and is applied to input 3 of OR 6A. Output 2 of OR 6A goes high and is applied to input 9 of OR 6B, locking the FF in this condition even after SRTP becomes disabled. The high 2 output of OR 6A is applied to the set level input 4 (s) of FF 18, RT FLAG. When CCCP (Control character combined pulse) is generated (at the same time as CSSP), it is applied through input terminal A2A10P1-19 to the pulse 5(T) input of FF 18. This sets FF 18. The low zero (9) output of FF 18 is applied to input 7 of OR 14. Provided that neither STOP nor CANCEL is being transmitted, which have higher priority than RT, inputs 3 and 4 of OR 14 are low. Inputs 8, 9, and 10 of OR 14 are grounded. When CCLP (Control character Load Pulse) arrives through input terminal A2A10P1-26 from the Transmit Baud Counter as a low pulse, input 5 of OR 14 goes low. This causes output 2 of OR 14 to go high, producing the LDRT (Load Retransmit) pulse which loads the first half of the RT control sequence into the Transmit Buffer. The high 2 output of OR 14 is also applied to the reset level input 7(R) of FF 18. At CC2P, when the second character of the RT control sequence is loaded into the Transmit Buffer, CCCP is again produced (this time by CC2P), and applied to the pulse 5(T) input of FF 18, and resets FF 18. The RT control sequence has now been transmitted to the ADMS. Also during this time, the Manual RT FF 13 is reset. Its high zero (9) output is applied to the set level input 4(S) of FF 20, AUTO RT SENT. When LDRT is generated it is also applied to the pulse 5(T) input of FF 20, setting it. The high one (2) output of FF 20 is applied through resistor R1 to the base of transistor Q1. This causes Q1 to conduct providing a ground return for the Control Panel RT lamp, illuminating the lamp.

f. Before the message can be retransmitted, ACK synchronization must again be established between the TCU and the ADMS. In direct reply to the RT, the ADMS sends to the TCU a Cancel which means that the ADMS agrees that the message should be retransmitted, scraps the current message, and asks for ACK-2 in return prior to actually retransmitting the message. Once the TCU sends the ACK-2, the ADMS retransmits the message.

1-64. Stop After Message Has Been Received, Functional Analysis

a. When the TCU, TTY output device is for any reason abnormal the STOP transmission by the TCU does not occur until the full message has been received, regardless of its condition. Generally, the TCU sends STOP, then receives Repeat and transmits either ACK if the message was correctly received, or RT if the message has to be retransmitted.

b. Transistor Q3 (fig. 1-6) monitors the output device. When the device is functioning properly the base of Q3 is at a negative level. When an abnormal condition exists a high ABNO (Abnormal Output) signal (positive) is applied to the base of Q3. Q3 conducts placing ground on the base of Q2. Q2 stops conducting and allows +5 volts to be extended to input of OR 3A. Output 2 of OR 3A goes low and is applied through ouput terminal A2A4P1-14 as the low ABON (Abnormal Output Device Not) signal. ABON is applied through input terminal A2A5P1-14) (fig. 1-7) to input 5 of OR 13A. Input 4 of OR 13A is grounded.

c. When the end-of-message has been received, this condition is stored by the N's counter, FF's 19, 20, and 18 (fig. 1-6). The condition of 4 consecutive N's received produces EOMR which is applied to output terminal A2A4P1-19. EOMR is applied through input terminal A2A5P1-40 (fig. 1-7) to input 7 of AND 2B. At Receive Mark count 4 (PAPD), a high pulse is applied through input terminal A2A5P1-9 to input 9 of AND 2B. Receipt of SPDR (first bit of repeat receive following EOMR) applies a high pulse to input 8 of AND 2B. Output 10 of AND 2B goes high and is applied to input 8 of OR 7B. Output 10 of OR 7B goes high and is applied to input 7 of OR 12B. Output 10 of OR 12B goes low and is applied to input 5 of OR 12A, which operates with OR 12B as the INTERMESSAGE flip-flop. Input (3) of OR 12A is grounded. Input 4 of OR 12A is low because neither START, ACK 1 or 2, RT, nor STOP receive control sequences are being received. Output 2 of OR 12A goes high and is applied to input 8 or OR 12B, locking the FF in this condition even after SPDR is disabled. The low 10 output of OR 12B is applied to input 8 of OR 17B. Since, after the arrival of the first cancel pulse from the ADMS (initially), the POWER ON FF (OR 16A and B) have been reset, input 9 of OR 17B is low. When the Repeat arrives from the ADMS, following the end-of-message (4N's) the RRPN (Repeat Receive Not) level is disabled and goes low. This is applied to input terminal A2A5P1-11 and from there to input 7 of OR 17B.

d. The output 10 of OR 17B is applied to input 8 of AND 18B. The Control Panel End-of-Message Receive delay is high, since the manual STOP at EOM is disabled. Thus, input 9 of AND 18B is high (EMRD). Output 10 of AND 18B goes high and is applied to input 3 of OR 17A. Output 2 of OR 17A goes low and is applied to input 3 of OR 13A. Input 4 of OR 13A is grounded. Output 2 of OR 13A goes high and is applied to output terminal A2A5P1-48 as the SSTO-1 (Send Stop Once) signal.

e. SSTO-1 is applied through input terminal A2A4P1-48 (fig. 1-6) to input 9 of OR 4B. Output 10 of OR 4B goes high and is applied through output terminal A2A4P1-47 to input terminal A2A9P1-26 (fig. 1-11) to input 8 of OR 9B, which operates with OR 9A as a flip-flop. Output 10 of OR 9B goes low and output 2 of OR 9A goes high and it remains this way even after SSTO is disabled. The high output 2 of OR 9A is applied to input 7 of OR 7B. Output 10 of OR 7B is high and is applied to the set level input 4(5) of FF 13, STOP FLAG.

f. When CSSP arrives, FF 13 becomes set. A STOP transmission is then executed. The ADMS then answers with a Repeat control sequence. Again, the repeat is applied to the TCU on input terminal A2A5P1-11 (fig. 1-7) as the low inverse of the RRPN (repeat not) level. Output 2 of OR 17A goes low and is applied to input 9 of OR 13B and input 3 of OR 13A. If the abnormal condition still exists (of the TTY output device) ABON is applied as a low level to input 5 of OR 13A. In this case output 2 of OR 13A goes high and the STOP is transmitted again and repeat is received. If the Abnormal condition of the output TTY device is cleared, ABNO-1 is applied as a low level to input 7 of OR 13B. Output 10 of OR 13B, in this case is high, and applied to output terminal A2A5P1-12 as the EMRP (End-of-Message Received pulse). This means that the TCU has now successfully received the message and that it can now acknowledge. EMRP is applied to input terminal A2A4P1-11 (fig. 1-6) of the Receive-End-of-Message circuit. From here, it is applied to input 5(T) of FF 17. Since the set level input 4(S) and the reset 7(R) input of FF 17 is high because of the presence of MREE (Message Received), FF 17 is complemented from its previous state placing either its one (2) output or its zero (9) output high. The former is AKTE (ACK-2 Enable) and is sent to output terminal A2A4P1-22. The latter is AKOE ACK- Enable) and is sent to output terminal A2A4P1-23. EMRP is also applied to input 7 of OR 12B. Output 10 of OR 12B becomes high and is applied to output terminal A2A4P1-8 as the SDAK (Send Acknowledge) level.

g. The TCU will also generate the STOP Control Sequence when a power clear/systems clear (PWRC) is generated. This protects against the loss of receive data or a received message. PWRC is applied to input 8 of A2A5 Latch 16 storing a High on output 2 of A2A5 Latch 16 until a CANCEL is received. The High output level from Latch 16 is applied to input 9 of A2A5 AND 20B. Input 8 of

A2A5 AND 20B will be High because a STOP has not been stored (STCN). The START pulse controlnot level from pin 50 of A2A6 generates a High whenever a START space is detected, except for control characters. This results in the first character received (STCN) to pass a High through A2A5 or 15B completing the conditioning of A2A5 AND 20B. The High output (STOP 1) will cause a STOP control character to be generated. The control character sequence will result in the following order:

Control character	From	To
CANCEL	Power Clear in TCU	ADMS
ACK-2	ADMS	TCU
START (II)	ADMS	TCU
Text Characters		
STOP	TCU	ADMS
REPLAY	ADMS	TCU
RETRANSMIT	TCU	ADMS
CANCEL	ADMS	TCU
ACK-2	TCU	ADMS

The receipt of CANCEL will clear A2A5 Latch 16 enabling receipt of traffic.

h. The TCU may also generate the STOP Control Sequence by two other methods. STCN (Stop Control Sequence Not) is applied to input terminal A2A5P1-34 (fig. 1-7) signifying that a stop thus far has not been sent. It is applied as a high level to input 8 of AND 20B. Input 9 of AND 20B is the 2 output of the POWER ON flip-flop OR 16. This has been previously set by application of PWRC (power on clear) to input 8 or by application of a Start Receive Pulse (SARP) pertaining to a received message, or a RTRP, ATRP, AORP, or STRP, pertaining to a transmitted message. These are applied by way of OR 1 to input 3 of AND 2A. Input 4 of AND 2A is the output of a flip-flop consisting of OR 19. The output 10 of OR 19B is applied to input 4 of AND 2A. The input to OR 19 is by way of pin 4, which is the output of AND 14A, pin 2. Input 4 of AND 14A is SPCN (Start pulse Control Not) from the Receive Baud Counter. The significance of this is that a Rep control sequence is not being followed by data while in the intermessage state. Input 5 of AND 14A is from output 10 of FF OR 9 which has been previously set by way of AND 4A. The inputs to AND 4A are on pin 4 from the reset state of the INTERMESSAGE flip-flop (OR 12) and on pin 3 from a previous receipt of CARP-2, ENRP, or RERP. The output 10 of AND 20 is thus high and is applied to terminal 17 as STOP-1.

i. Upon receipt by the TCU of a repeat control sequence or an unintelligible character, either pin 5 or pin 4 of OR 15A is high. Output 2 is high and is applied to input 5 of AND 20A. If the automatic retransmit capability of the TCU is not disabled, input 4 of AND 20A is high. If no stop has been sent by the TCU, the TCU is not in the end-of-message receive mode, and data is being received, inputs 4, 3, and 5, respectively, of OR 5A are low. Output 2 is thus high and is applied to input 3 of AND 20A. Output 2 of AND 20A is high and is applied to input 9 of flip-flop OR 11. This places the flip-flop in position where its 10 output is low and this is applied to input 9 of OR 5B. If a receive control sequence is not presently being received and, but a character is being received, inputs 8 and 7, respectively of OR 5B are low. Output 10 is thus high and is applied to terminal A2A5-23 as STOP-2 signal.

j. STOP-1 is applied to terminal 36 and STOP-2 to terminal 37 of A2A3 (fig. 1-5). STOP-1 is applied to input 9 of OR 21B. STOP-2 is applied to input 8 of OR 21B. Either input produces an output at pin 10 which is applied to input 3 of OR 15A. Output 2 is high and applied to terminal 54 as STOP. STOP, in turn, initiates the retransmit sequence, the message is acknowledged, and subsequent message receptions by the TCU can be made.

k. When the cancel receive control sequence is received by the TCU, the TCU sends ACK-2 if the output TTY device is not acting abnormally. The TCU may, under the opposite condition, transmit a STOP to the ADMS in response to a cancel. The high 10 output of OR 6B (fig. 1-6), due to the cancel receive pulse, is applied to input 8 of AND 2B. If the output TTY device is abnormal, a high level is applied to input 7 of AND 2B. Output 10 of AND 2B goes high and is applied to input 7 of OR 4B. The high 10 output of OR 4B is then applied out of this logic card as SSTO (Send Stop once), a stop is sent, and the ADMS sends a repeat to which the TCU answers with STOP again or sends an ACK-1 or ACK-2. Both SDAK, and either AKTE or AKOE are applied to input terminals A2A11P1-8 and -45 or -46 (fig. 1-13), respectively. The appropriate ACK is generated.

Section IX. MESSAGE PROCESSING PRIORITY CONTROL

NOTE

Refer to note preceding paragraph 1-10.

1-65. Control Sequence Priorities, Functional Analysis

a. During simultaneous message transmission, the TCU may send any one of seven control sequences. Four of these are associated with the TCU's role as receiver of the message from the ADMS: Stop, Retransmit, and ACK-1 or ACK-2. The remaining three are associated with the TCU's role as a transmitter of the message to the ADMS:

Cancel, Repeat, and Start. It is possible that the TCU is required to send a control sequence associated with a received message, and to send a control sequence associated with a transmitted message at the same time. When this occurs, the control sequences are transmitted on a priority basis. The priority, from high to low, is: Cancel, Stop, Retransmit, Repeat, ACK (1 or 2), and Start.

b. Assume the TCU is attempting to establish ACK synchronization by sending a cancel to the ADMS. Assume also that the TCU desires to stop a message which is being received, by generating a Stop Control Sequence. In this case the Cancel takes priority and is sent first. Then the stop may be sent.

c. Associated with each control sequence is a Flag flip-flop. More than one Flag FF (for the associated control sequence) can be set at the same time. The actual loading of the control sequence (LCNL, LSTP, etc.) are tied to the priority scheme. In this way, the lower priority control sequence may be sent as soon as the higher priority control sequence has been sent before data (which is the lowest priority) is sent. If a Cancel is to be sent, the Cancel Flag FF12 (fig. 1-11) is set and its low (a) zero output is applied to input 5 of OR 6A. When CCLP (Control Character Load Pulse) (which is a low pulse) is generated, it is applied to input 3 of OR 6A. The output 2 of OR 6A then generates the LCNL (Load Cancel) pulse.

d. If a stop is to be sent, the Stop Flag FF 13 is set and its low (9) zero output is applied to input 7 of OR 6B. The CCLP is then applied to input 9 of OR 6B, generating LSTP (Load Stop) as long as the high cancel flag is not applied to input 8 of OR 6B. If CNFG is present it temporarily disables OR 6B.

e. If a Retransmit is to be sent, the RT Flag FF18 (fig. 1-12) is set and its zero (a) output is applied to input 7 of OR 14. The CCLP is then applied to input 5 of OR 14, generating LDRT (Load Retransmit) as long as either the high Cancel Flag or high stop flag is not applied, respectively, to input 3 or 4 of OR 14. If either CNFG or STPF is present, OR 14 is temporarily disabled.

f. If a Repeat is to be sent, the REP flag FF 24 is set and its zero (9) output is applied to input 9 of OR 19. The CCLP is then applied to input 4 of OR 19, generating LRPT (Load Repeat) as long as either the high Cancel Flag, Stop Flag, or Retransmit Flag is not applied, respectively, to input 7, 5, or 8 of OR 19. If either CNFG, STPF, or RTFG is present, OR 19 is temporarily disabled.

g. If an ACK-1 or ACK-2 is to be sent, the ACK FLAG FF17 (fig. 1-13) is set and its low zero (9) output is applied to input 9 of OR 2. The CCLP is then applied to input 3 of OR 2, generating either LAK1 (Load Acknowledge 1) or LAK2 (Load Acknowledge 2) as long as neither the high Cancel Flag, Stop Flag, Retransmit Flag, or Repeat Flag is applied, respectively, to input 8, 7, 5, or 4 of OR 2. If either CNFG, STPF, RTFG, or RPFG is present, OR 2 is temporarily disabled.

h. If a start is to be sent, the START FLAG FF 25 is set and its low zero (9) output is applied to input 3 of OR 8. The CCLP is then applied to input 10 of OR 8, generating Start, as long as neither the high Cancel flag, Stop flag, Retransmit flag, Repeat flag, or Acknowledge flag is applied, respectively, to input 4, 5, 7, 8, or 9 of OR 8. If either CNFG, STPF, RTFG, RPFG, or ACK FLAG is present, OR 8 is temporarily disabled. Notice that Start is the lowest priority control character.

1-66. Priority of Control Characters Over Data, Functional Analysis

a. If the TCU is in the process of sending data to the ADMS and a control sequence must be sent to the ADMS because of the TCU's receive section (STOP, RT, or ACK 1 or 2), the transmission of data is interrupted, the control sequence is sent, and data transmission is resumed.

b. Among the inputs to OR 2A (fig. 1-15) is FLGS. If this becomes true (a control sequence flag is set), FLGS is applied as a high level to input terminal A2A14P1-10, and to input 3 of OR 3A. Output 2 of OR 3A goes high and is applied to input 3 of OR 2A. Output 2 of OR 2A goes low and is applied to input 3 of OR 8A. Since inputs 4 and 5 of OR 8A are low (grounded), output 2 of OR 8A goes high and becomes the HALT signal. This, by way of logic previously described enables the reset level input of FF 13. When SPDT for the following character is generated by the TCU, a pulse is applied to the pulse 5(T) input of FF 13, setting the FF and disabling the TTY device clutch. Also at this time, the previous data character has been loaded into the Transmit

Buffer, and at the ensuing Time 8 (Transmit Baud Counter), the data character is shifted out. The resetting of FF 13, however, disables the TTY input device clutch so that no more data characters will be sent to the ADMS until after the control sequence is sent. This is done by again setting FF 13, CLUTCH CONTROL, which pulls the input TTY device clutch, enabling data characters again.

Section X. MANUAL OPERATION CIRCUITRY

Note: Refer to note preceding paragraph 1-10.

1-67. Manual Transmission of Control Characters

a. Stop.

(1) In order to manually stop the TCU from receiving data from the distant station, the TCU operator momentarily actuates the STOP AT EOM switch to the STOP position. This momentarily places a high level on input terminal A2A5P1-42 (fig. 1-7). This is EMRD-1 and it disables EMRD. EMRD (now disabled) disables AND 18B, eventually causing the output of OR 13B to be low, thus disabling EMRP (end of message pulse). This, in turn, disables the appropriate acknowledge to be sent to the ADMS. EMRD-1 is applied to input 5 of AND 18A. The ADMS will continue to transmit the complete message, including the repeat to the TCU, even though the TCU's acknowledgment is disabled. Thus, RRPN, EOMR, SPDR, and PAPD are true. Also, the power on FF (OR 16) is still reset. Thus, OR 17B has complete input low coincidence and its output 10 goes high. This is applied to input 3 of AND 18A. Output 2 of AND 18A goes high and is applied to output terminal 5 as GEMD (gated end-of-message delay). GEMD is applied to input 9 of OR 23B, which operates with OR 23A as an FF. Output 10 of OR 23B goes low and is applied to input 5 of OR 23A. Input 4 of OR 23A is PWRC which is disabled. Input 3 of OR 23A is low because the EMRD signal has been disabled. Output 2 of OR 23A goes low and is applied to input 7 of OR 23B, locking this FF in this condition even after EMRD-1 becomes disabled. Output 2 of OR 23A is applied on output terminal A2A5P1-47 as the REMA (Receive EOM) Alarm.

(2) GEMD is also applied through input terminal A2A4P1-45 (fig. 1-6) to input 4 of OR 4A. Output 2 of OR 4A is high and is applied to input 8 of OR 4B. Output 10 of OR 4B is extended on output terminal A2A4P1-47 as the SSTO (send stop once) signal. This causes the transmission of a stop control sequence to the ADMS. The ADMS then replies to the TCU with a repeat control sequence.

(3) The TCU operator may then decide to resume message reception while stops are being transmitted and repeats are being received. When this occurs, the End of Message Delay switch is returned to its original position, which enables EMRD and disables EMRD-1. This, in turn, respectively produces EMRP and disables GEMD, resulting in the transmission of the appropriate acknowledge signal to the ADMS, provided that the output device is not operating abnormally.

b. Retransmit.

(1) The RT transmit control sequence may be sent manually by the TCU. If, for instance, the printer (TTY output) device is printing out information which is incorrect, the message may have to be retransmitted from the ADMS (fig. 1-12). The operator initiates manual transmission of RT by pressing the Control and Indicator Panel RT switch. This causes a high signal to be applied to input terminal A2A10P1-9 (SMRT). This is applied to the direct set input 3(P) of flip-flop 13 MANUAL, RT, setting FF13.

(2) SMRT is applied to input terminal 23 of logic card Receive Control Sequences A2A3 (fig. 1-5). From here, SMRT is applied to input 5 of OR 15B. Output 2 of OR 15A goes high and is applied to output terminal 54 as STOP. A stop con-

trol sequence is transmitted to the distant station. The detailed operation of this transmission has been described previously. When stop is sent, the signal STPS (stop sent) is applied to input terminal A2A4P1-40 (fig. 1-6). Once the ADMS has transmitted a repeat to the TCU, if EMRD is present and if the output device is not operating abnormally, AND 2A is enabled and generates SRTP (Send Retransmit Pulse). This results in the transmission of the RT control sequence to the ADMS. The ADMS replies with a cancel, to which the TCU replies with ACK-2. The distant station may then retransmit the message to the TCU.

c. Cancel. The TCU operator may manually transmit a cancel control sequence. If, for instance, the TCU is in the process of sending a message when it is determined that another message of higher priority has to be sent immediately, the current message transmission may be interrupted. The operator depresses the Control and Indicator panel cancel switch. This causes a high CAMA (CANCEL MANUAL) signal to be applied to input terminal 15 of logic card A2A9 Transmit Cancel, Stop Sequence (fig. 1-11). CAMA from here is applied to input 9 of OR 3, which operates with OR 8B as the CNCL FF. From this point, the transmission of cancel is similar to that for an automatic transmission. If the proper conditions exist, the CNCL FLAG flip-flop FF 12 becomes set (when CSSP is generated). This ultimately causes a cancel control sequence to be sent to the ADMS. The ADMS then replies with ACK-2 and at this time the higher priority message may be sent.

d. Repeat. When a repeat is sent to the ADMS, it can be transmitted 3 times before the ADMS is obliged to reply with its final response. Once this limit is reached, an alarm condition becomes present which is visually and audibly sent to the operator. From this point, subsequent repeats must be sent manually. This is done by manual operation of the Control and Indicator panel START SEND switch. Operation of this switch sends a high level (SSPW) to input terminal A2A10P1-13 of logic card, Transmit Repeat-Retransmit Sequence (fig. 1-12) SSPW (which is the OR condition of SSSW or PWRC, fig. 1-18) is applied to input 3 of OR 3A. Output 2 of OR 3A goes high and is applied to input 3 of OR 2A. Output 2 of OR 2A goes high and is applied to the direct reset 8(c) inputs of flip-flop 23 and 22 (Repeat Counter), clearing it. The counter in its alarm state was in count 3. The fact that the repeat counter is no longer in count 3 causes AND 21B to be disabled which sends a low level to input 3 of OR 11A. Inputs 4 and 5 of OR 11A are low because they are grounded. Output 2 of OR 11A goes high and is applied to input 3 of AND 21A. Input 5 of AND 21A has been high since the TCU first entered the repeat mode. When CSSP is produced (whose generation has been previously described), a high pulse is applied to input 4 of AND 21A. Output 2 of AND 21A goes high and is applied to the direct set 3(P) input of FF24, REPEAT FLAG, setting it. This initiates transmission of up to three more repeats to the ADMS. The detailed operation of this operation has been described previously. If the ADMS does not reply with its final response by the time 3 more repeats have been sent, the operator may either send more or may initiate corrective action by other means.

1-68. Testing Control Character Sequences, Functional Analysis

a. During periods of nonprocessing of messages, maintenance personnel check the operation of the TCU by manually sending control sequences while the TCU is in the TEST MODE. In this mode the TCU is connected back-to-back between its transmit and receive sections; thus, when a control sequence is sent, another is received as if normal operation was taking place. *For example,* when a cancel is sent by the transmit section, the receive section sees a cancel receive, thus must respond with ACK-2. These manual controls, called test switches, are located on the TCU Simulator Test panel. Each of the seven control sequences transmittable by the TCU during operation can also be test transmitted. These are CANCEL, START, STOP, REPEAT, RETRANSMIT, ACK-1 and ACK-2.

b. Cancel. When the test cancel maintenance switch is operated, a high signal, TCAN (Test Cancel) is applied to input terminal 45 of logic card A2A9 Transmit Cancel-Stop Sequence (fig. 1-11). From here, TCAN is applied to input 7 of OR 3 which operates with OR 8B as the CNCL flip-flop from this point, the actual transmission of cancel occurs similarly to that during normal operation.

c. When the test stop manual maintenance switch is operated, a high signal, TSTP (Test Stop), is applied to input terminal A2A9P1-17 of Transmit Cancel-Stop Sequence (fig. 1-11). From here, TSTP is applied to input 7 of OR 9B, which operates with OR 9A as a flip-flop. From this point the actual transmission of Stop occurs similarly to that during normal operation.

d. Retransmit. When the test retransmit maintenance switch is operated, a high signal, TRTS (Test Retransmit) is applied to input terminal A2A10P1-39 of Transmit Repeat-Restransmit Sequence (fig. 1-12). From here, TRTS is applied to input 7 of OR 1B. Output 10 of OR 1B goes high and is applied to input 7 of OR 6B, which operates with OR 6A as the RT flip-flop. From this point, the actual transmission of RT occurs similarly to that (of an automatic RT) during normal operation.

e. Repeat. When the test repeat maintenance switch is operated, a high signal, TREP (Test Repeat) is applied to input terminal A2A10P1-11 of Transmit Repeat-Retransmit Sequence (fig. 1-12). From here, TREP is applied to input 5 of OR 3A and input 3 of OR 25A. From this point, the actual transmission of repeat occurs similarly to that during normal operation.

f. Start. When the test start maintenance switch is operated, a high signal, TSTT (Test Start), is applied to input terminal A2A11P1-20 of logic card, Transmit Start-Acknowledge Sequence (fig. 1-13). From here TSTT is applied to input 4 of OR 9A. Output 2 of OR 9A goes high and is applied to input 4 of OR 20A, which operates with OR 20B as the START FF. From this point the actual transmission of START occurs similarly to that during normal operation.

g. ACK-1. When the ACK-1 maintenance switch is operated, a high signal, MAOE (Manual Ack-1 Enable) is applied for input terminal A2A4P1-24 of Receive-End of Message (fig. 1-6). From here, MAOE is applied to the direct reset input 8 (c) of FF17, resetting FF7. The high zero (9) output of FF 17 is applied to output terminal A2A4P1-23, as the AKOE (Ack one enable) level. AKOE is applied to input terminal A2A11P1-46 of logic card Transmit Start-Acknowledge Sequence (fig. 1-13). From here AKOE is applied to input 3 of AND 7A. MAOE is applied to input terminal A2A11P1-57 of this logic card and from here to input 5 of OR 24A. Output 2 of OR 24A goes high and is applied to the direct set 3 (P) input of FF 22 ACK FF, setting it. The high one (2) output of FF 22 is applied to the set level input 4 (s) of FF 17, ACKFLAG. When CCCP (Control Sequence Combined Pulse) is generated and applied to the pulse 5 (T) input of FF 17, FF 17 becomes set. From this point the actual transmission of ACK-1 occurs similarly to that during normal operation.

h. Ack-2. When the Ack-2 maintenance switch is operated, a high signal, MATE (Manual Ack-2 Enable), is applied to input terminal A2A4P1-7 of logic card, Receive-End of Message (fig. 1-6). From here, MATE is applied to input 5 of OR 12A. Output 2 of OR 12A is applied to the direct set input 3 (P) of FF 17, setting FF 17. The high one (2) output of FF 17 is applied to output terminal 22 as the AKTE (Ack-2 Enable) signal. AKTE is applied to input terminal 45 of logic card A2A11 of the Transmit Start-Acknowledge Sequence (fig. 1-13). From here AKTE is applied to imput 9 of AND 7B. MATE is applied to input terminal A2A11P1-54 of this logic card. From here, MATE is applied to input 4 of OR 24A. Output 2 of OR 24A goes high and is applied to the direct set 3 (P) input of FF 22, setting it. From this point, the actual transmission of Ack-2 occurs similarly to that during normal operation.

1-69. Precession of TCU Message Number, Functional Analysis

a. When the message count proceeds normally, each EMVP-1 (signifying the completion of a successful message transmission) advances the Message Counter one step. To reset the counter and start numbering messages from count 000. The message number switch on the TCU Control and Indicator Panel is operated. This causes a high level (MENS) to be applied through terminal A2A16P1-33 (fig. 1-17) to input 8 of OR 23B, which operates with OR 23A as a flip-flop. Output 10 of OR 23B goes low and is applied to input 3 of OR 23A. Input 4 of OR 23A is low since PWRC is disabled. Input 5 of OR 23A is low since LOND-8 is disabled. This causes output 2 of OR 23A to go high which is applied to input

9 of OR 23B locking the FF in this state, even after the message number switch is disabled (MENS goes low). The high 2 output of OR 23A is also applied to inputs 7 and 5 of ANDS 1B and 1A, respectively.

b. When the message leader transmission operation begins, LOND-0 is produced and generates a high level which is applied through input terminal A2A16P1-6 to inputs 3 and 8 of ANDS 1A and 1B. Output 2 and 10 of ANDs 1A and 1B go high. Output 2 of AND 1A is applied to the direct reset input 8 (C) of FF -2, -6, -11, -16, -21, and -22; and the output of AND 1B is applied to the direct reset input C (8) of FF -4, -5, -9, -10, -15, and -20. This clears the entire counter to all zeros, enabling a new counting sequence to be started.

c. To start message numbering at a specific count, the TENS, UNITS, and HUNDREDS rotary switches on the Control Indicator panel are set to the desired position. Operation of these switches (fig. 1-3) places a mark (high or low) on each of four wires per switch. Each group of four wires are identified as 1, 2, or 3, with each wire within the group identified as A, B, C, or D. These leads are the SND—leads which are applied to the Message Identifier, Sequence Generator circuit (fig. 1-16) A2A15P1- on the terminals listed below.

Mnemonic	Input terminal	Associated wire (decimal digit)
SNDA-1	36	LSD
SNDB-1	37	LSD
SNDC-1	48	LSD
SNDD-1	35	LSD
SNDA-2	39	
SNDB-2	7	
SNDC-2	16	
SNDD-2	44	
SNDA-3	9	MSD
SNDB-3	45	MSD
SNDC-3	12	MSD
SNDD-3	18	MSD

d. The signals are each applied to one input of one of 12 half AND gates (6 AND gates) which are used to decode the four signals of each decimal digit. The half AND gete and its associated input signal are as follows:

Mnemonic	AND gate	Input terminal	Digit
SNDA-1	1A	3	LSD
SNDB-1	6B	9	LSD
SNDC-1	3B	9	LSD
SNDD-1	6A	3	LSD
SNDA-2	1B	9	
SNDB-2	7A	3	
SNDC-2	3A	3	
SNDD-2	7B	9	
SNDA-3	2A	3	MSD
SNDB-3	8A	3	MSD
SNDC-3	2B	9	MSD
SNDD-3	8B	9	MSD

e. When the message numbering switch S15 (fig. 1-3) is depressed, +5 volts is extended through resistor R24 and out through A1J1-46 as the MENS (Message Number Select) leads. The high MENS lead enters A1A16P1-33 (fig. 1-17) and is applied to input 8 of OR 23B which operates with OR 23A as a flip-flop. Output 2 of OR 23A goes high and is applied to output terminal A2A16P1-34 as the PREE (Preset Enable) signal. It also partially enables AND gate 1. PREE is applied through input terminal A2A15P1-49 (fig. 1-16) to input 5 of AND 1A, input 8 of AND 1B, and input 8 of AND 3B. PREE is also applied to input terminal A2A5P1-58 of the Output Device Control circuit (fig. 1-7). From here it is applied to input 5 of OR 25A and input 9 of OR 25B. The high output 2 of OR 25A is the PREE-1 (Preset Enable 1) signal which is extended to output terminal A2A5P1-26. The high output 10 of OR 25B is the PREE-2 (Preset Enable 2) signal which is extended to output terminal A2A5P1-57. Both are extended to the Message Identifier-Sequence Generator circuit (fig. 1-16). PREE-1 appears on input terminal A2A15 P1-42 and PREE-2 appears on input terminal A2A15P1-19. PREE-1 is applied to input 4 of AND 3A, input 5 of AND 2A, input 8 of AND 2B, input 7 of AND 6B, and input 5 of AND 6A. PREE-2 is applied to input 5 of AND 7A, input 7 of AND 7B, input 5 of AND 8A, and input 7 of AND 8B.

f. During the generation of previous LOND pulses, their AND gates have been set up to prepare for the precession of the message numbers. Specifically, the following message numbering counts have enabled the following AND gates:

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(1) LOND-1 (7 of 3B, 5 of 3A, and 7 of 2B)
(2) LOND-2 (8 of 6B, 4 of 7A, and 4 of 8A)
(3) LOND-4 (8 of 8B)
(4) LOND-5 (4 of 2A)
(5) LOND-6 (8 of 7B)
(6) LOND-7 (7 of 1B)
(7) LOND-8 (4 of 6A)
(8) DEMN-9 (4 of 1A)

g. Where a binary one existed (due to manual switch action) the outputs 2 or 10 of these ANDS produced high pulses which were routed out of this circuit as follows:

AND output	Signal mnemonic	Output terminal
6B-10	PREB-1 (Preset) B-1	38
1A-2	PREA-1	6
6A-2	PRED-1	5
1B-10	PREA-2	40
7A-2	PREB-2	8
3B-10	PREC-1	47
7B-10	PRED-2	13
3A-2	PREC-2	46
8A-2	PREB-3	15
2A-2	PREA-3	10
8B-10	PRED-3	17
2B-10	PREC-3	11

h. These apply individually to either the LSD, middle, or MSD decimal digit as described above and all are routed to the A2A16 logic card (fig. 1-17). Once inside this logic card, the signals are routed to the direct set P(3) inputs of the associated message numbering counter FF's as follows:

Signal	Input terminal	FF	Associated with (decimal counter)
PREA-1	11	2	LSD
PREB-1	5	6	LSD
PREC-1	7	11	LSD
PRED-1	8	16	LSD
PREA-2	9	21	
PREB-2	43	22	
PREC-2	21	4	
PRED-2	24	5	
PREA-3	22	9	MSD
PREB-3	50	10	MSD
PREC-3	55	15	MSD
PRED-3	25	20	MSD

i. This action sets the flip-flops preselected by the operator, placing the desired count into the message numbering counter. The counting will thus begin from this point and continue to advance by one, unless the operator presets it to another number.

j. DEMN-10 when generated, was applied to this logic card, to input 5 of OR 23A as a high pulse. This reset the FF comprised of OR's 23A and 23B so that during the remainder of this operation (message transmission) a clear to zero and presetting of the message numbering counter disabled from reoccurring.

Section XI. MISCELLANEOUS LOGIC CIRCUITRY

1-70. TCU Lamp Test Feature, Functional Analysis

a. Located on the TCU Control and Indicator Panel, is a Lamp Test pushbutton, which, when depressed, lights various Control Indicator Panel lamps. Located on the Simulator Test Panel is a Lamp Test Pushbutton which, when actuated, lights various Simulator Test panel lamps. The particular lamps illuminated by operation of either of these pushbuttons are described in this section. When the Control Indicator Panel pushbutton is depressed, a high level LPTE (Lamp Test) is applied to the logic cards. Depression of the Simulator Test Panel Switch produces level LPTE-1.

b. LPTE-1 is applied to input terminal 8 of logic card A2A2 (fig. 1-4). From here it is applied through Resistor R3 to the base of Transistor Q1. This places the base at a positive value with respect to the emitter (which is grounded), causing Q1 to conduct. This provides a ground path for the Maintenance Control Switch Indicator Lamp which is connected on the other end to +12 volts, thus lights the lamp. Unless otherwise specified all logic card lamp test circuits consist of the same type resistors and transistor as the above and thus, the detailed operation will not be repeated. Instead a table will be provided which shows the source panel signal (LPTE or LPTE-1), the logic card, the input terminal, and the lamp name.

Source	Logic card	Input terminal	Lamp name
LPTE-1	A2A3	57	ACK-1 Received.
LPTE-1	A2A3	57	ACK-2 Received.
LPTE	A2A4	25	ABNORMAL-OUT.
LPTE	A2A5	46	Message Received.
LPTE	A2A9	58	Cancel Sent.
LPTE	A2A10	53	RT Sent.
LPTE	A2A10	53	3 RPT (Alarm).
LPTE	A2A10	53	Stop Received.
LPTE-1	A2A11	37	ACK-1 Transmitted.
LPTE-1	A2A11	37	ACK-2 Transmitted.
LPTE	A2A11	34	Message Transmitted.
LPTE	A2A11	34	Abnormal Input.
LPTE	A2A14	55	Transmit Halt.
LPTE	A2A19	34	Alarm Set.

1-71. DC Power Filters, Functional Analysis

a. The TCU includes a total of 19 logic cards when the three enquiry response/disconnect logic cards (1 disconnect and two enquiry response) are included. With the exception of logic cards A2A7 (Timing Generator), A2A13 (Disconnect) and A2A15 (Message Identifier Sequence Generator), all cards have at least two filters for the input dc power. Each of these two filters services approximately half the logic on the card. Refer to logic Card Receive Buffer and Decoder (fig. 1-4) for typical filters. One filter includes a series inductor L2 and two parallel capacitors C1 and C2; the other includes a series inductor L3 and two series capacitors C3 and C4. On each filter the positive side of the capacitor is connected to pin 6 of the connected logic elements includes a series inductor L3 and two parallel capacitors C3 and C4. On each filter the logic elements.

b. Logic card A2A7 (fig. 1-9) contains one filter for the +5 volts, which includes series inductor L1 and parallel capacitors C1 and C2. This logic card also includes filters for + and — 12 volt dc inputs for certain time delay circuits. The +12 volt filter includes two series inductors L2 and L3 and four parallel capacitors C3, C4, C5, and C6. Also included is a voltage divider network, connected off the +12 volt filter, consisting of Resistor R2, Capacitor C7 and Diode CR1, from which +9.3 volts dc is obtained. Also included is a voltage divider network, connected off the +12 volt filter, consisting of Resistor R1, Capacitor C8, and Diode CR2, from which +6.2 volts dc is obtained. The —12 volt dc filter consists of series inductor L4 and parallel capacitors C9 and C10. Also included is a voltage divider network, connected off the —12 volt filter, consisting of Resistor R3, Capacitor C11, and Diode CR3, from which −6.2 volts dc is obtained.

c. Logic card A2A13 (fig. 1-14) contains four filters. One is comprised of series inductor L2 and parallel capacitors C1 and C2 to filter +5 volts dc. One filter consists of series inductor L3 and parallel capacitors C3 and C4 to filter the −6.2 volts (obtained from card A2A7). One filter consists of series inductor L6 and parallel capacitors C5 and C6 to filter the +6.2 volts (obtained from card A2A7). The final filter consists of series inductor L8 and parallel capacitors C7 and C8 to filter the +9.3 volts dc (obtained from card A2A7).

d. Logic card A2A15 (fig. 1-16) consists of one filter for the +5 volts dc input. This filter consists of series inductor L2 and parallel capacitors C1 and C2.

1-72. Transmit Baud Counter Operation in Crypto Mode, Functional Analysis

a. When the TCU is operated in the TCU mode with a 75 baud device, a 7.42 unit code is used. This provides a total character time of about 98 milliseconds. In the crypto mode, a TTY device which operates at 75 baud, 7 units code, could be used. This provides a total character time of about 93 milliseconds. In the TCU mode, the Transmit Baud Counter (fig. 1-10) counts almost eight times per character, which consumes about 98 milliseconds. In the Crypto Mode, the Transmit Baud Counter is allowed seven counts (0 to 6), then under most conditions, is reset. The seven counts consume a total time of about 93 milliseconds, which matches the 7 unit character time.

b. In the crypto mode, transmission of data (and control sequences) depends upon the crypto supplying a crypto step pulse to the TCU. The crypto supplies this pulse about every 98 milliseconds, the effect of which is to slow down operation about 5 milliseconds per character, but which has no adverse effect upon TCU operation. On (fig. 1-3). When the Control Indicator Panel TCU/CRYPTO Switch has been placed to the CRYPTO position, the effects are: (1) CRSE is grounded to provide CRYPTO Step Enable; (2) TCUD is connected to +5 volts providing Crypto Enable; (3) CRST (Crypto Step Pulse) is applied from the Crypto Device through the NORMAL position of the MODE switch as CRST-1.

c. CRSE is applied through input terminal

A2A9P1-58 (fig. 1-11) to the emitter of Transistor Q4. CRST-TR-1 is applied through terminal A2A9P1-34 and resistor R10 to the base of Q4. When the CRST pulse enters the TCU (approximately every 98 milliseconds) it is a wide, square pulse. The network consisting of Q4 and Q3 differentiate it to a narrower, sharper pulse. CRSE places the Q4 Emitter at ground. When CRST-1 enters, Q4 conducts, applying a +5-volt signal to the differentiating network consisting of R7 and C7. Q3 is normally conducting (when CRSE is present) by the +5 volts through resistor R7. The differentiated leading edge of the pulse generated at the collector of Q4 cuts off transistor Q3 for approximately 150 microseconds. This produces a +5-volt, 150-microsecond CRST-2 pulse at collector of Q3.

d. CRST-2 is applied to terminal 26 of A2A8 (fig. 1-10) and extended to input 8 of AND 20B. During data transmission periods, data or control characters, the distant station is not blinded. This applies BLFN (Blind Flag Not) signal to input 7 of AND 20B. And 20B produces a high pulse at output 10 which is applied to input 9 of OR 25B. Output 10 of OR 25B produces a high pulse and generates the following signals (that would be normally generated at Time 8 in TCU mode): (1) CLEP (TTY device clutch enable pulse); (2) one enabling input to AND 14B so that, when the TTY input device is halted and the Transmit Buffer (fig. 1-18) is filled with the first character of a control sequence, shifting is enabled; (3) the pulse inputs to control character flip-flops (23 and 22); (4) a signal to input 8 of AND 9B so that, during the proper time, the SEND GENERATE FF OR15 is reset.

e. CRST-2 is also applied to input 4 of AND 20A. Input 3 of AND 20A is high when FF 23 or 22 (or both) is set (meaning that a control sequence is being transmitted). Output 20B AND 20A goes high and results in the following (1) generation of items (1) through (4) of *d* above; (2) resetting of SEND DELAY FF OR11 as control sequence is being transmitted; (3) OR 10B, resets Transmit Baud Counter so that Baud Counter stays synchronized with crypto.

f. TCUD is applied to input 7 of AND 19B. Input 9 of AND 19B is the nonblinded condition of the distant station. Input 8 of AND 19B is the SEND DETECT enable signal, signifying that at this time the Transmit Baud Counter has reached count 7 (111), it is cleared (*g* below).

g. TCUD is also applied to input 4 of AND 19A. Input 5 of AND 19A is high at Transmit Baud Counter Count 7. Output 2 of AND 19A goes high and sets the SEND DETECT FF OR11. In this way the Baud Counter is cleared (see *f* above).

h. During periods of the intermessage state (neither control or data characters are being transmitted), BLFN is disabled, thus allowing the Transmit Baud Counter to count to eight. This does not adversely affect crypto operation as long as characters are not being transmitted.

i. Other than the special conditions, resulting from TCUD and CRST-2 described above, the Transmit Baud Counter operates similarly to that when the TCU is in the TCU condition.

Section XII. POWER SUPPLY AND ISOLATOR ASSEMBLY

1-73. General

This section provides a functional description of Power Supply, filter PP-4571/G and Isolator Assembly RE-216/G. The power supply has four dc power supplies all physically contained within assembly A3, and all supplied from a 120/230-volt, 60-cycle ac input. Each power supply and its associated function is listed below and discussed separately under subsequent paragraph:

+5.5-volt TCU logic voltage
+12-volt TCU lamp voltage
—12-volt TCU negative bias voltage
—180-volt NIXIE counting tube voltage

1-74. Power Supply Functional Analysis

(fig. 1-24)

a. Primary ac power is applied to the TCU AC input filter (fig. 1-24). The filter output is connected to terminals E6 and E7. These terminals, and all referenced components in this power supply discussion, are located on assembly, A3. Ac power is coupled from the terminals through switch S1 and fuses F5 and F6 to terminals E2 and E3. The ac potential at terminals E2 and F3 is applied directly to terminals A1TB1-18 and -19 which are connected to the primary side of power transformer

A1T1. This transformer provides four secondary output voltages; one for each dc power supply.

b. The ac output from terminals 5 and 7 of transformer A1T1 is full wave rectified by diodes CR1 and CR2, and the resulting dc is coupled through paralleled series regulators Q1 and Q2 to provide the +5.5 vdc regulated output. In addition, rectifiers A1CR1 and A1CR2, rectify this secondary-winding voltage of A1T1 to provide collector potential for transistors Q2, A1Q1, and base bias voltage to transistor A1Q2.

(1) The +5.5-volt rectified output of the power supply is developed across resistor A1R25, in parallel with the series-parallel combination of potentiometers A1R8 and R2, and resistors A1R26 and A1R9 which form a voltage divider network. The voltage divider provides a sample of the output voltage as base potential for transistor A1Q3, one-half of a differential amplifier. Transistor A1Q2, the second half of the differential amplifier has a constant base potential established by zener diode A1CR5. Any change in current flow through either half of the differential amplifier causes a change in voltage drop across the common emitter resistor, A1R7.

(2) When the output voltage begins to change (assume an increase) the base potential of A1Q3 increases. As A1Q3 increases conduction, a decrease in collector potential occurs; for the voltage drop across the collector load impedance, consisting of transistors A1Q1 and resistor A1R1, increases. The base of control emitter follower Q3 decreases in potential, which in turn, lowers the base potential of series regulators A3Q1 and Q2. Series regulator current flow decreases; and the voltage drop across the parallel transistors increases, offsetting the attempted increase in output voltage.

(3) Transistor A1Q1 is a PNP transistor in series with the NPN differential amplifier A1Q3. It is a current source with a temperature coefficient opposite to that of its series counterpart A1Q3. Voltage deviations, as a function of thermal excursions, as well as the effects of ripple in the control circuit supply voltage are eliminated. Series diodes A1CR3 and A1CR4 along with collector resistor A1R1 maintain a constant voltage at the base-emitter junction of transistor A1Q1. The diodes are forward biased, permitting a positive base potential to be developed across resistor A1R3.

c. The ac output from terminals 8 and 10 of transformer A1T1 is full wave rectified by diodes A1CR6 and A1CR7, and the resultant dc potential is coupled through series regulator Q4 to provide the +12 vdc regulated output.

(1) The +12-volt regulated output is developed across the voltage divider network consisting of resistors A1R13, A1R27, in parallel with potentiometer R3, and A1R14. Base bias voltage for control transistor A1Q5 is provided by this voltage divider network. This voltage is an adjustable sample of the output voltage.

(2) If the output voltage attempts to change (assume an increase) the base potential of transistor A1Q5 would increase. As A1Q5 increases conduction, a decrease in collector potential occurs; for the collector load resistor, A1R10, drops a greater amount of the applied voltage. The base of control transistor A1Q4 decreases in potential, and its emitter follows, which in turn, lowers the base potential of series regulator Q4. Series regulator current flow decreases, which causes it to appear as a higher series impedance; and more of the voltage is dropped across it, offsetting the attempted increase in output voltage.

(3) Capacitors A1C2 and A1C3 filter the dc voltage before regulation; which capacitor A1C7 filters the regulated +12-volt output. Zener diode A1CR8, in series with resistor A1R12 maintains a constant emitter potential on transistor A1Q5, insuring that all current fluctuations in the transistor are the result of regulation requirements.

d. The ac output from terminals 11 and 13 of transformer A1T1 is full wave rectified by diodes A2CR9 and A2CR10, and the resultant dc potential is coupled through series resistor A2R15 and series regulator A2Q6 to provide the −12 vdc regulated output.

(1) The −12-volt regulated output is developed across the voltage divider network consisting of resistors A2R18, A1R28 in parallel with potentiometer R1, and A2R19. Base bias voltage for control transistor A2Q7 is established by the setting of potentiometer R1 of the voltage divider network which, in turn, sets the output voltage level. The provided base potential is a sample of the output voltage.

(2) If the output voltage attempts to change (assume that it tries to go more negative) the base of transistor A2Q7 becomes more positive with respect to the emitter and current flow through the transistor increases. A decrease in collector potential occurs, for collector load resistor A2R16

drops a greater amount of the applied voltage. The base of series regulator A2Q6 becomes more negative and series regulator current decreases, which causes it to appear as a higher series impedance. A greater amount of negative voltage is dropped across it, offsetting the tendency to go more negative.

(3) Capacitor A2C4 filters the dc voltage before regulation. Zener diode A2CR11, in series with resistor A2R16, maintains a constant emitter potential on transistor A2Q7.

e. The ac output from terminals 14 and 15 of transformer A1T1 is full-wave rectified by a bridge rectifier consisting of diodes A2CR12 through A2CR15. The resultant dc output is coupled through series resistor A2C20 and series regulator A2Q8 to provide the +180-volt dc regulated output.

(1) The +180-volt regulated output is developed across the voltage divider network consisting of resistor A2R23 and potentiometer A2R24. Base bias voltage for control transistor A2Q9 is established by the setting of potentiometer A2R24 which, in turn, sets the output voltage level. This base potential is a sample of the output voltage.

(2) If the output voltage should attempt to change (assume an increase) the base of transistor A2Q9 becomes more positive and current flow through the transistor increases. A decrease in collector potential occurs, for the collector load resistor, A2R21, drops a greater amount of the applied voltage. The base of series regulator A2Q8 becomes more negative and series regulator current decreases, which causes it to appear as a higher series impedance. A greater amount of voltage is dropped across it, offsetting the attempted increase in output voltage.

(3) Capacitor A2C5 filters the dc voltage output of the bridge rectifier. Zener diode A2CR16, in series with resistor A2R22, maintains a constant emitter potential on transistor A2Q9.

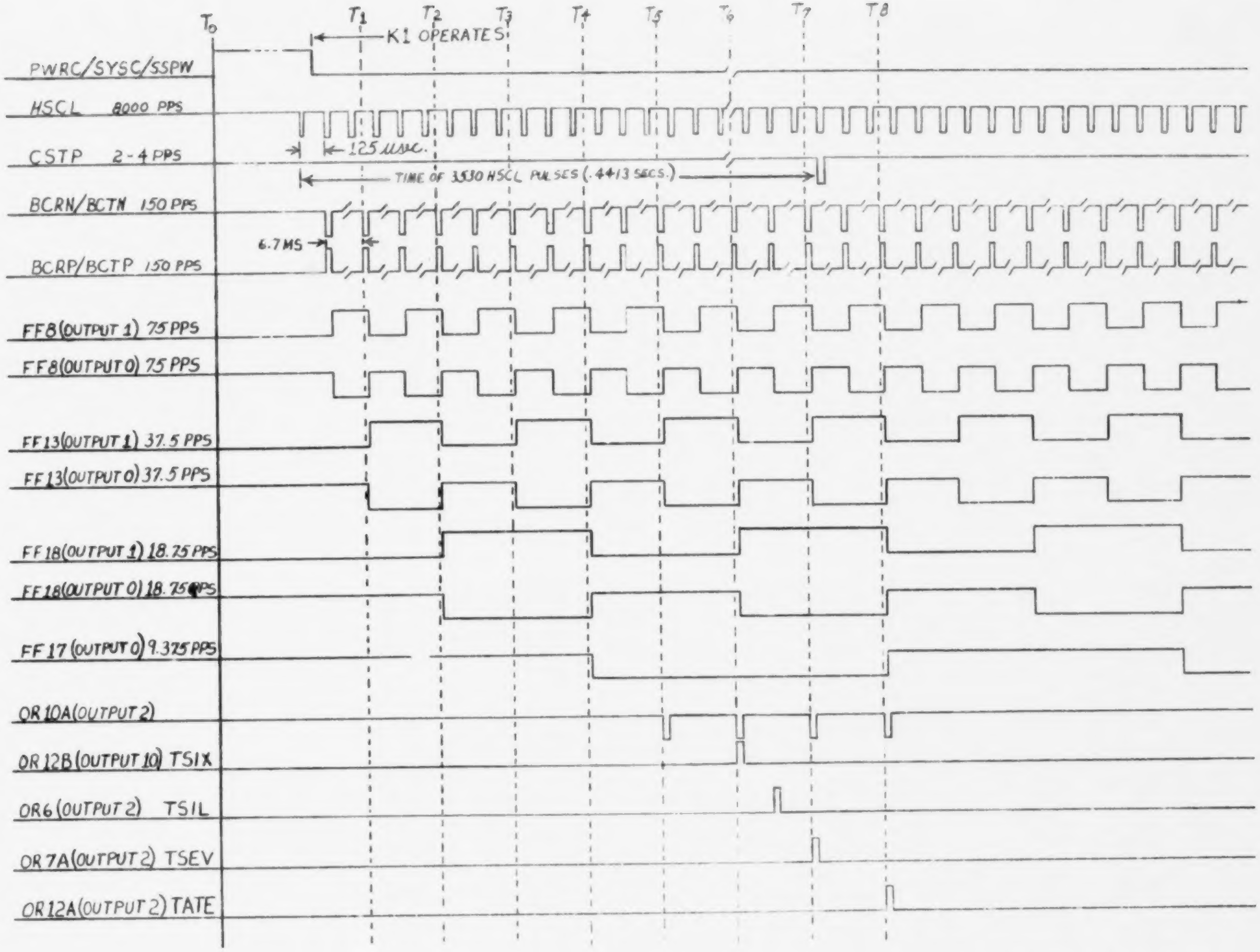
1-75. Isolator Assembly RE-216/G(A6) Functional Analysis

(fig. 1-25)

a. The Isolator Assembly contains the component required to filter the DISC (disconnect) signal prior to leaving the TCU. This filtering is accomplished in FL3. FL3 is a sealed unit which utilizes two (2) input power sources to filter the DISC signal. One of the power supplies is contained within Isolator Assembly A6 (PSI). This delivers +6 volts and −6 volts to one-half of FL3. The other power supply, the TCU power supply (A3), delivers +6 volts to the other half of FL3. The DISC signal from A2A13 enters FL3 through J3. The DISC signal leaving FL3 is extended to the external equipment through J2.

b. The 120/230 volts ac enters assembly A6 on J1 pins A and B. Pin C of J1 provides an ac protective ground for assembly A6. During 120-volt ac operation, fuses F1 and F2 are 0.125 ampere; for 230-volt ac operation, fuses F1 and F2 are 0.062 ampere. Switch S1 is the ac power on/off switch and is shown in the open position. When S1 is closed 120/230 volts ac is filtered by FL1 and FL2 and applied to PS1.

c. The output of PS1 is +6 volts dc on terminal 5, −6 volts ac on terminal 7, and common (RTN) on terminal 6. The +6 and −6 volts dc are applied to DS1 and DS2 respectively, which light indicating power output. Fuses F3 and F4 (0.125 amp) ensure that the power supply is not overloaded. The +6 vdc and −6 vdc is applied to one section of FL3 through P1 pins C and A respectively.


T0
T1
T2
T3
T4
T5
T6
T7
T8
K1 OPERATES
PWRC/SYSC/SSPW
HSCL 8000 PPS
125 usec.
CSTP 2-4 PPS
TIME OF 3530 HSCL PULSES (.4413 SECS.)
BCRN/BCTN 150 PPS
6.7 MS
BCRP/BCTP 150 PPS
FF8(OUTPUT 1) 75 PPS
FF8(OUTPUT 0) 75 PPS
FF13(OUTPUT 1) 37.5 PPS
FF13(OUTPUT 0) 37.5 PPS
FF18(OUTPUT 1) 18.75 PPS
FF18(OUTPUT 0) 18.75 PPS
FF17 (OUTPUT 0) 9.375 PPS
OR10A(OUTPUT 2)
OR12B(OUTPUT 10) TSIX
OR6(OUTPUT 2) TSIL
OR7A(OUTPUT 2) TSEV
OR12A(OUTPUT 2) TATE

TM 5895-438-35-209

Figure 1-26. Transmit Band Counter PL-1143/G waveforms.

CHAPTER 2

TROUBLESHOOTING

Section I. GENERAL TROUBLESHOOTING INFORMATION

Warning: When troubleshooting or making repairs in this equipment, be extremely careful. Voltages as high as 230 volts are present internally. Use insulated test probes when making the required voltage measurements.

2-1. General Instructions

a. Troubleshooting includes all the techniques outlined for organizational maintenance and any special or additional techniques required to isolate a defective part. These procedures are not complete within themselves but supplement the procedures described in organizational maintenance. The systematic troubleshooting procedure, which begins with the operational and sectionalization checks performed at an organizational level, must be completed by further localizing and isolating techniques.

b. Troubleshooting is performed in an operational TCU after it has been removed from service. When trouble occurs, certain observations can be made which will help in determining whether the local equipment is at fault or if the trouble exists elsewhere in the system. Usually, when troubleshooting is performed while the equipment is operating as part of a system, it is done at the organizational level (TM 11-5815-335-12). Troubleshooting at the DS and GS level is usually done with the component removed from the equipment with which it is normally associated.

c. Troubleshooting of the assemblies of the TCU is performed normally within an off-line operational TCU. When the on-line TCU is utilized for troubleshooting, consideration must be given to return the equipment to an on-line status. To accomplish this, entire assemblies of the TCU should be replaced when they are suspected, and the defective subassemblies later maintained in an off-line TCU.

2-2. Organization of Troubleshooting Procedures

a. General. The first step in servicing a defective equipment is to sectionalize the fault. Sectionalization means tracing the fault to the major component. Refer to TM 11-5815-335-12 for sectionalization procedures. The second step is to localize the fault. Localization means tracing the fault to the defective subchassis or stage. The third step, isolation, means tracing the fault to the defective part. Some faults, such as burned-out resistors, arcing or shorted transformers, can often be isolated by sight, smell, or hearing. The majority of faults, however, must be isolated by checking lamp and printout indications.

b. Localization. The tests listed below will aid in localizing the trouble. First, localize the trouble to a stage or subassembly. Then isolate the trouble within that stage or subassembly by voltage, resistance, and continuity measurements. Use the following methods of trouble localization:

(1) *Troubleshooting charts.* The trouble symptoms listed in these charts will aid in localizing trouble to a component part.

(2) *Signal substitution.* Signal substitution procedures enable the repairman to localize a trouble quickly. Positive 3.7 vdc and an oscilloscope may be used in signal substitution procedures.

c. Isolation.

(1) *Voltage and resistance measurements.* This equipment is all solid-state. Observe all cautions given to prevent semiconductor damage. Make voltage and resistance measurements in this equipment only as specified. When measuring voltages, use tape or sleeving to insulate the entire test prod, except for the extreme tip. A momentary short circuit can ruin a device being tested. (*For example,* if the bias is shorted out, excessive current could ruin a transistor.) Use resistor and capacitor

color codes (figs. 2-1 and 2-2) to find value of components.

(2) *Intermittent troubles.* In all tests, the possibility of intermittent troubles should not be overlooked. If present, this type of trouble often may be made to appear by tapping or jarring the equipment. Check the wiring and connections to the units of the set.

2-3. Test Equipment Required for Troubleshooting

Table 2-1 lists the test equipment required for troubleshooting.

Table 2-1. Test Equipment Required for Troubleshooting

Test Equipment	Common name
Card Extender	Card Extender.
Multimeter AN/USM-162	Multimeter.
Oscilloscope (Hewlett-Packard model 140A) equipped with:	Oscilloscope.
Dual-trace amplifier (Hewlett-Packard model H06-1405A).	Preamp.
Time base and delay generator (Hewlett-Packard model 1421A).	Time base.
Multimeter ME-26A/U (Hewlett-Packard Model 410B), or equal vacuum tube voltmeter.	VTVM.

2-4. Integrated Circuit Modules

a. Nine integrated circuit modules are used in the TCU. Table 2-2 lists the module nomenclature and describes its logic function.

Table 2-2. Integrated Circuit Module Functions

Nomenclature	Function
Integrated Circuit Module-C7968K	Dual 3-input Expander.
Integrated Circuit Module-C7969K	6-input AND.
Integrated Circuit Module-C7970K	Dual 3-input AND.
Integrated Circuit Module-C7971K	7-input NOR.
Integrated Circuit Module-C7972K	Dual 3-input NOR.
Integrated Circuit Module-C7973K	Dual Expandable NOR.
Integrated Circuit Module-C7974K	J-K flip-flop.
Integrated Circuit Module-C7975K	Dual Expandable OR.
Integrated Circuit Module-C7976K	Dual 3-input OR.

b. Each integrated Circuit Module has ten terminals which are numbered 1 through 10, pin 10 being identified by a key on the element. The pins are numbered clockwise when viewed from the bottom of the can, and counterclockwise when viewed from the top.

2-5. Printed Circuit Board Integrated Circuit Module Locations

The components located on printed circuit boards, other than Integrated Circuit Module are normally located at convenient positions on the board. The integrated circuit modules, however, have specific locations numbered 1 through 25 on a 5 x 5 matrix arrangement. These positions may or may not be equipped with a logic element. When not equipped, the position is left vacant and the number assigned to the position is omitted.

Section II. TROUBLESHOOTING PROCEDURES

2-6. Troubleshooting Procedures, General

a. When troubleshooting the TCU during control sequence testing, message testing, or as a result of a malfunction which occurs during actual operation, there is a common rule to follow. In each case the setup during which the malfunction took place, should be duplicated, or simulated as closely as possible during troubleshooting. In this way the symptoms should recur during trouble analysis and the maintenance man will have some assurance that measurements to be made should yield similar results to those which occurred during the initial malfunction.

b. The tables and text which follow provide maintenance personnel with procedures to follow for isolating malfunctions below the card level. Also provided are the symptoms of the malfunction.

c. During performance of the troubleshooting procedures, it is often required to perform continuity checks. Figures 2-3 through 2-28 are wiring diagrams which aid in continuity testing. In addition, figures 2-4 through 2-22 and figure 2-28 provide part locations on the logic card.

d. It is advisable to complete the troubleshooting test on a particular card before changing logic elements, as the following steps will assist in narrowing down the possible number of logic elements which may be causing the malfunction.

2-7. Isolation of Logic Card Malfunctions

a. Once it is determined during organizational maintenance that a particular card has malfunctioned, the malfunction must be isolated to the logic on that card to the closest possible extent. Using the card extender, the malfunctioned card is inserted into its appropriate logic rack position to facilitate isolating the trouble on this card to a logic circuit, or group thereof. The conditions under which this card exhibited failure during monthly preventive maintenance or during normal operation can often provide a valuable clue as to a specific area of trouble on the card.

b. The following tables and text provide the method of checking logic cards. The item numbers shown in these tables apply to those during which the malfunction originally occurred at the organizational level (TM 11-5815-335-12). These tables are as follows:

(1) Table 2-3, Routing Indicator Trouble Chart.

(2) Table 2-4, Control Sequence Trouble Chart.

(3) Table 2-5, Message Checking Trouble Chart. This table provides detailed procedures for isolation of logic card malfunctions encountered during message checking. This table is split up into the malfunctions encountered during the preliminary message-checking procedure followed by the troubleshooting procedures of trouble encountered during the different types of message checks. The latter is divided into six (6) subsections which provide trouble analysis for—

- (*a*) Sending of two consecutive messages.
- (*b*) Use of stop-at-EOM Transmit Capability.
- (*c*) Use of stop-at-EOM Receive Capability.
- (*d*) Testing Message with Abnormal Input Device.
- (*e*) Testing Message with Abnormal Output Device.
- (*f*) Manual Canceling and Retransmitting of Message in Process.

(4) Table 2-6, Disconnect Line Trouble Chart. Whenever a trouble is indicated by the failure of a lamp to light, check the lamp by pressing the LAMP TEST switch before proceeding with any troubleshooting routine.

(5) Table 2-7, Disconnect Line Trouble Chart for Isolator Assembly, RE-216/G.

Table 2-3. Routing Indicator Trouble Chart

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
11	The TCU does not correctly generate its routing indicator.	*a.* Card A2A20....	*a.* Because all the characters of the routing indicator are generated by the LOED (Load Enquiry Data) pulses, perform the following: (1) Remove Card A2A3 from the logic rack. (2) Remove Card A2A20 from the logic rack. (3) Insert the Card Extender into the A2A20 slot. (4) Connect Card A2A20 to the card extender. (5) Connect oscilloscope channel A INPUT Lead to Terminal 11 of A2A20. Place oscilloscope TIME/CM Switch to 20 msec. (6) Connect oscilloscope EXT INPUT Lead to Terminal 7 of A2A20 and select positive sync. (7) Connect oscilloscope channel B INPUT Lead to Terminal 10 of A2A20. (8) On the Control and Indicator Panel, place the MODE Switch to TEST position. (9) Obtain a lead terminated at both ends with alligator clips. (10) Connect one end to terminal 24 (of Card A2A20). (11) Connect the other end to the junction of C1 and L2 (on Card A2A20). (12) On the Simulation Test Unit, momentarily place the SYS CLR Switch to the SYS CLR position. (13) The trace obtained on the oscilloscope should be a negative pulse resulting from Channel A and a negative pulse resulting from Channel B. These should be separated by ≈106 milliseconds (for 75 or 74.2 baud operation) or ≈176 milliseconds (for 45.45 baud operation). *Note.* These pulses occur 3 times during this test (until a 3 RPT.); to repeat operate SYS CLR again. (14) If the trace is obtained and no pulses are present, any one of Logic Elements 24, 23, 22, 21, 2, 15, 17, 18, 14, 12, 19, 16, 10, 20, or 25 may be bad. If a VTVM reading at TP1 yields +3.7 volts, logic elements 10, 20, 15, and 25 are good. In this case, disconnect oscilloscope setup. (15) If only one of the pulses required in the trace of step (13) is not obtained, the following conclusion can be made. (*a*) If the trace from Terminal 11 is correct, but that from Terminal 10 is not, Logic Element 12 is bad. (*b*) If the trace from Terminal 10 is correct but that from Terminal 11 is not, Logic Element 2 is bad. In either case, disconnect the oscilloscope setup. (16) If both of the pulses required in step *a*(13) are present connect the oscilloscope Channel A INPUT Lead to Terminal 10. (17) Connect the Channel B INPUT Lead to Terminal 42. The trace obtained should be similar to step (13). (18) If the trace at Terminal 42 is not obtained, Logic Element 1 or 7 is bad. In this case, disconnect oscilloscope setup.

Table 2-3. Routing Indicator Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
			(19) Successively connect the oscilloscope Channel A INPUT Lead and Channel B INPUT Lead to respectively: (*a*) 42 and 9. (*b*) 9 and 13. (*c*) 13 and 15. (*d*) 15 and 16. (*e*) 16 and 17. (*f*) 17 and 14. (*g*) 14 and 19. (*h*) 19 and 18. (*i*) 18 and 44. (20) In each case the trace should be two negative pulses spaced apart by 106 milliseconds (for 74.2 or 75 baud operation) or 176 milliseconds (for 45.45 baud operation). (21) If, in any case, the trace associated with the B Channel INPUT Lead is not present, the following Logic Elements are defective: *Terminal* .... *Logic element* (*a*) .... 9 .... 6 (*b*) .... 13 .... 3 (*c*) .... 15 .... 13 (*d*) .... 16 .... 4 or 13 (*e*) .... 17 .... 4 (*f*) .... 14 .... 3 (*g*) .... 19 .... 9 (*h*) .... 18 .... 9 or 15 (*i*) .... 44 .... 8 (22) If all outputs check out successfully, there may be a discontinuity problem somewhere between Card A2A20 and Card A2A21.
11	The TCU does not correctly generate its routing indicator.	*b.* Card A2A21	(1) Remove Card A2A21 from the logic rack. (2) Insert the Card extender into the A2A21 slot. (3) Connect Card A2A21 to the Card Extender. (4) Disconnect Card A2A20 from the logic rack. (5) Using alligator clips, connect terminal 28 (of Card A2A21) to Terminal 19. (6) Using alligator clips, connect terminal 27 to Terminal 12. (7) Connect the VTVM common Lead to Terminal 3. (8) Successively connect the VTVM DC lead to Terminals 25, 24, 23, and 22, observing a +3.7-volt reading each time. (9) If any of the above readings yields ground, one of the following logic elements is bad depending upon the Terminal at which ground was noted: *Terminal* .... *Logic element* (*a*) .... 25 .... 21, 22, or 23. (*b*) .... 24 .... 22, 17, or 24. (*c*) .... 23 .... 24, 18, or 20. (*d*) .... 22 .... 25, 19, or 20 (10) If all readings are ground, Logic Element 8 is bad. (11) If all readings are correct, disconnect the lead from terminal 12 and connect it to Terminal 9. (12) Connect the VTVM DC lead to terminal 26 and observe a +3.7-volt dc reading.

Table 2-3. Routing Indicator Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
			(13) If the correct reading is not obtained, connect the VTVM DC lead to Terminal 22 and observe a +3.7-volt reading. If this is obtained, Logic Element 23 or 16 is bad. If this is not obtained, Logic Element 2 is bad. (14) If the reading of step (12) is obtained, disconnect the lead from terminal 9 and connect it to terminal 18. (15) Connect the VTVM DC lead to Terminal 23, observing a +3.7-volt reading. If this is not obtained, Logic Element 4 or 20 is bad. (16) If the correct reading is obtained, disconnect the lead from Terminal 18 and connect it to Terminal 16. (17) Read +3.7 on WORD 1 JUMPER. If not element 9 is bad. (18) Connect the VTVM DC lead to one of terminals 26, 25, 24, 23, and 22 from which a "one" is expected, depending on the WORD 1 JUMPER. (19) If this particular terminal shows a reading of +3.7 volts, proceed to step (20). If it does not, Logic Element 23, 24, 25 is bad. (20) Disconnect the lead from Terminal 16 and connect it to Terminal 14. (21) Read +3.7v on WORD 2 JUMPER. If not logic element 3 is bad. (22) Repeat step (18) except bear in mind that this check is for the second character. (23) If this particular terminal shows a reading of +3.7 volts, proceed to step (24). If it does not, Logic Element 23, 24, 25 is bad. (24) Disconnect the lead from terminal 14 and connect it to Terminal 10. (25) Read +3.7v on Word–3 jumper. If not element 7 is bad. (26) Repeat step (18) except bear in mind that this check is for the third character. (27) If this particular terminal show a reading of +3.7 volts, proceed to step (29). (28) If it does not, Logic Element 16, 21, 17, 18 or 19 is bad. (29) Disconnect the lead from Terminal 10 and connect it to Terminal 11. (30) Read +3.7v on Word–4 jumper. If not, element 7 is bad. (31) Repeat step (18) except bear in mind that this check is for the fourth character. (32) If this particular terminal shows a reading of +3.7 volts, proceed to step (33). If not, Logic Element 16, 21, 17, 18 or 19 is bad. (33) At this point if the variable portion of the routing indicator (for the particular TCU) consist of four characters proceed to step (48). If it consists of 5, 6, or 7 characters, proceed to step (34). (34) Disconnect the lead from Terminal 11 and connect it to Terminal 15. (35) Measure +3.7v on Word 5 Jumper. If not element 3 is bad. (36) Repeat step (18) except bear in mind that this check is for the fifth character. (37) If this particular terminal shows a reading of +3.7 volts, proceed to step (38). If not, Logic Element 16, 23, 17, 18, or 19 is bad.

Table 2-3. Routing Indicator Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
			(38) At this point, if the variable portion of the routing indicator (for the particular TCU) consists of five characters proceed to step (48). If it consists of 6 or 7 characters proceed to step (39). (39) Disconnect the lead from Terminal 15 and connect it to Terminal 17. (40) Measure +3.7 on Word-6 Jumper. If not element 9 is bad. (41) Repeat step (18) except bear in mind that this check is for the sixth character. (42) If this particular terminal shows a reading of +3.7 volts, proceed to step (43). If not, Logic Element 16, 21, 17, 18, or 19 is bad. (43) At this point, if the variable portion of the routing indicator (for the particular TCU) consists of six characters, proceed to step (48). If it consists of 7 characters, proceed to step (44). (44) Disconnect the lead from Terminal 17 and connect it to Terminal 13. (45) Measure +3.7v on Word-7 Jumper. If not element 8 is bad. (46) Repeat step (18) except bear in mind that this check is for the 7th character. (47) If this particular terminal shows a reading of +3.7 volts, proceed to step (48). If not Logic Element 16, 21, 17, 18, or 19 is bad. (48) If the TCU messages for the particular TCU are according to the ACP-127 format and the card has checked out OK, the card should be checked for continuity. In this case, dismantle test setup. (49) If the TCU messages for the particular TCU are according to the JANAP 128 format, disconnect the lead from Terminal 13 and connect it to Terminal 20. (50) Connect the VTVM DC lead for terminal 23. If +3.7 volts is obtained, proceed to step (51). If not, Logic Element 4 or 20 is bad. (51) Disconnect the lead from Terminal 20 and connect it to Terminal 8. (52) Connect the VTVM DC lead to Terminal 25. If +3.7 volts is obtained, there may be a discontinuity problem with this card. If not, Logic Element 2 is bad. (53) Disconnect the test setup.
11	The TCU does not correctly generate its routing Indicator.	*c.* Card A2A2	Logic Element 4 may be defective.
	The TCU does not correctly generate its routing Indicator.	*d.* Card A2A3	Logic Element 22 or 23 may be defective.

Table 2-4. Control Sequence Trouble Chart

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
16a	CANCEL XMITED lamp does not light.	TRANSMIT CANCEL-STOP SEQUENCE logic card, A2A9.	(1) Remove Card A2A9 from the logic rack. (2) Connect the Card Extender to the A2A9 slot. (3) Connect Card A2A9 to the Card Extender. (4) Connect the VTVM common lead to terminal 3 and TURN ON POWER. (5) Connect the VTVM DC lead to terminal 5. A +0.0 volt reading shows a discontinuity between terminal 5 and the Control Indicator Panel. (6) If +11 is measured, connect the VTVM DC lead to terminal 9. A +3.7 volt reading should be obtained. If it is not, Logic Element 11 is bad. (7) If it is, the network consisting of R3, R1, C5 and Q1 is malfunctioned. This can be isolated by checking R3, R1, and C5. Disconnect VTVM setup.
16b	ACK-2T LAMP does not light.	TRANSMIT START ACKNOWLEDGE SEQUENCE, Card A2A11.	(1) Remove Card A2A11 from the Logic Rack. (2) Insert the Card Extender into A2A11 position. (3) Connect Card A2A11 to Card Extender. (4) Connect VTVM common lead to terminal 3 and turn ON POWER. (5) Connect VTVM DC lead to 36. A 0 volt reading indicates there is discontinuity between terminal 36 and the Simulator Test Panel. If +11V is measured go to Step 6. (6) Connect the VTVM DC lead to terminal 45. A +3.7 volt reading should be obtained. If it is not, there is discontinuity between terminal 45 and Card A2A4 or CNCL not sent or CNCL not RCVD. (7) If +3.7 is measured there is a malfunction in the network consisting of R12, R13, C8, and Q5. The trouble can be isolated by checking R12, R13, and C8. Disconnect VTVM setup.
16c	ACK-2R lamp does not light.	RECEIVE CONTROL SEQUENCES, Card A2A3.	(1) Remove Card A2A3 from the logic rack. (2) Insert Card Extender into A2A3 position. (3) Connect Card A2A3 to the Card Extender. (4) Connect VTVM common lead to terminal 3, and turn on Power. (5) Connect the VTVM DC lead to terminal 52. A +0.0 volt reading indicates there is discontinuity between terminal 52 and the Simulator Test Panel. If +11 v is measured go to step 6. (6) Connect the VTVM DC lead to the junction of pin 10, Logic Element 9 and R2. A +3.7 volt reading should be obtained. If it is, the network consisting of R2, R3, C5, and Q1 is malfunctioning. The trouble can be isolated by checking R2, R1, and C5. Disconnect VTVM setup. (7) If 0.6 v is read at junction of pin 10 and R2, logic element 9, 8, or 19 is bad.

Table 2-4. Control Sequence Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
17	MONITOR LAMP Does Not Light (START Control Sequence Only).	START Control Sequence Generating Logic Card A2A11.	(1) Put card A2A11 on extender and connect VTVM common lead to terminal 3. (2) Connect the VTVM DC lead to TP4. A +3.7 volt reading should be obtained. (3) If it is not, connect the VTVM DC lead to terminal 7 of logic element 24. A +3.7-volt reading should be obtained. If it is, logic element 24 is bad. (4) If it is not, connect the VTVM DC lead to terminal 3, 4, 5 of logic element 19. A +3.7 v reading should be obtained at each point. (5) If it is, Logic Element 19 is bad. (6) If pin 5 of 19 is not +3.7, connect the VTVM DC terminal to the junction of Q4 and R7. A ground should be obtained. If it is, Logic Element 15 or 21 is bad. (7) If it is not, connect the VTVM DC terminal to terminal 58. A −6.0 v should be obtained. If it is, the network consisting of Q3 and Q4 is bad. (8) If −6.0 v is not present on terminal 58, there may be a short condition between terminal 58 and +5 volts, requiring continuity check. (9) With TCU in test mode and Simulator Test Panel in CONT SEQ SIMULATOR in START position, connect the VTVM DC lead to terminal 20. A +3.7 volt reading should be obtained. (10) If it is not, there is discontinuity somewhere between terminal 20 and the Simulator Test Panel. If it is, either Logic Elements 9, 20, 19, 25, or 24 is bad. (11) Refer back to step (2). If the +3.7 volts is obtained, disconnect the VTVM DC lead from terminal 20. (12) Obtain an oscilloscope. Connect the channel A INPUT lead to Pin 41 of Card A2A11. *Note.* Whenever using the oscilloscope always ground the oscilloscope to the TCU chassis. Also, always keep the oscilloscope Channel A and B SENSITIVITY Switches on 5 V/CM. (13) Set the oscilloscope to −Internal SYNC. (14) Set the oscilloscope TIME/CM switch to 100 msec. The results obtained should be two negative pulses (167 millisec apart for 45.45 baud and 110 millisec apart for 75 or 74.2 baud), every 1-2 second in time. If the pulses are obtained, elements 24, 22, 17, or 8 are bad.
18a	ACK-1T lamp does not light.	TRANSIT START-ACKNOWLEDGE SEQUENCE, Card A2A11.	(1) Remove Card A2A11 from the Logic Rack. (2) Insert Card Extender into A2A11 position. (3) Connect Card A2A11 to Card Extender. (4) Connect VTVM common lead to terminal 3. (5) Connect VTVM DC lead to terminal 57. A 0.0 volt reading indicates there is discontinuity between terminal 57 and the Simulator Test Panel. (6) If +11 v is measured, connect the VTVM DC lead to terminal 46. A +3.7 volt reading should be obtained. If it is not, there is discontinuity between terminal 46 and Card A2A4.

Table 2-4. Control Sequence Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
			(7) If it is, there is trouble in the network consisting of R15, R16, C9, and Q6. The trouble can be isolated by checking R15, Q6, R16, and C9. Disconnect VTVM setup.
18b	ACK-1R lamp does not light.	RECEIVE CONTROL SEQUENCE, Card A2A3.	(1) Remove Card A2A3 from the logic rack. (2) Insert Card Extender into A2A3 position. (3) Connect Card A2A3 to Card Extender. (4) Connect VTVM common lead to terminal 3. (5) Connect VTVM DC lead to terminal 58. A 0.0 volt reading indicates there is discontinuity between terminal 58 and the Simulator Test Panel. (6) If +11.0 v is measured, connect the VTVM DC lead to the junction of Logic Element 9 pin 2 and R5. A +3.7 volt reading should be obtained. If it is not, Logic Element 9, 8, 13 or 9 are bad. (7) If it is +3.7 v, the network consisting of R5, R6, C6 and Q2 is malfunctioning. The trouble can be isolated by checking R5, R6, Q2 and C6. Disconnect VTVM setup.
18c	MONITOR LAMP does not light (ACK-1 Control Sequence only).	ACK-1 Control Sequence generating logic, CARD A2A11.	(1) Connect the common VTVM lead to terminal 3. Connect the DC VTVM lead to terminal 48. A +3.7 volt reading should be obtained. (2) If the +3.7 volts is not obtained, connect the VTVM DC lead to terminal 14. A +3.7 volt reading should be obtained. (3) If it is, obtain an oscilloscope, connect the channel A input lead to terminal 50 and set the oscilloscope to +INT SYNC. Then place the oscilloscope TIME/CM switch to 20 msec. When a trace is obtained, it should be 25 μsec positive pulses (167 millisec apart for 45.45 baud and 110 millisec apart for 74.2 or 75 baud) every one second in time. If this is obtained, Logic Element 4, 17 or 24 is bad. If these positive pulses are not obtained, there is an open condition, probably between terminal 50 and the TCU intra cabinet wiring. (4) In this case perform a continuity check after disconnecting the oscilloscope setup. (5) If the +3.7 volt reading at terminal 14 is not obtained, connect the DC terminal of the VTVM to terminal 55. If a reading of +5 volts is not obtained, there is an open condition, probably between terminal 55 and the TCU intra cabinet wiring; thus a continuity check should be performed. (6) If the +3.7 volts is obtained, Logic Element 24 or 22 is defective. (7) If the +3.7-volt reading of step (1) is obtained, obtain an oscilloscope and perform the same procedure as step (3) except connect the channel A input lead to TP2. Two positive 5 μsec pulses seen. If they are, the problem is discontinuity between terminal 39 and Card A2A19. A continuity check should then be made. Disconnect oscilloscope setup.

Table 2-4. Control Sequence Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
			(8) If these pulses are not obtained, connect the channel A INPUT Lead to terminal 41. Here, the results should be the same as step (7) except the pulses should be negative. If they are not present, discontinuity exists between terminal 41 and the TCU intra cabinet wiring. In this case a continuity check should be performed. Disconnect oscilloscope setup. (9) If the pulses described above are present, successively connect the DC terminal of the VTVM to terminals 43, 44, 15 and 16, observing a ground each time. (10) If this is obtained, connect the VTVM DC lead to terminal 46. A +3.7 volt reading should be obtained. If it is not there is discontinuity between terminal 46 and A2-A4 card. (11) If the +3.7 volts is obtained, either Logic Element 2 or 7 is bad. Disconnect VTVM setup. Perform a similar check here as for the ACK-1 Control Sequence Generating logic except for the following:
19a	ACK-2T Lamp does not light.	TRANSMIT START ACKNOWLEDGE SEQUENCE, Card A2A11.	Perform steps (1) through (7), item 16b. Suspect logic element 15, 23, 11, 12, 13, or 19.
19b	ACK-2R Lamp does not light.	RECEIVE CONTROL SEQUENCES, Card A2A3.	Perform steps (1) through (7), item 16c.
19c	MONITOR Lamp does not light (ACK-2 Control Sequence only).	ACK-2 Control Sequence Generating logic, Card A2A11.	Perform steps (1) through (11) of item 18c, and substitute TP1 wherever TP2 is referred to; substitute terminal 45 where terminal 46 is referred to; substitute terminal 54 where terminal 55 is referred to.
20	MONITOR lamp does not light (REPEAT Control Sequence only).	REPEAT Control Sequence Generating logic, Card A2A10.	(1) Remove Card A10 from the logic rack and insert a card extender in its place. Connect Card A2A10 to the card extender. Obtain an oscilloscope. (2) Set the oscilloscope up the same way as in item 17 step (1). The trace observed should be two positive pulses 167 milliseconds apart for 45.45 baud operation and 110 milliseconds apart for 75 or 74.2 baud operation, occurring every second. If these are obtained there may be discontinuity between pin 51 and the intra TCU wiring to card A2A19. (3) In this case disconnect the oscilloscope setup. (4) If these pulses are not obtained, connect the oscilloscope channel A INPUT lead to terminal 26. The results should be similar to those specified above, except the pulses are negative. If this is not obtained, there may be discontinuity between terminal 26 and the TCU intracabinet wiring. Disconnect oscilloscope setup. (5) If the specified pulses are present, successively connect the DC terminal of the VTVM to terminal 25, 46, 44, and 21. A ground should be obtained each time. If terminals 25 and 44 do not indicate a ground, there may be discontinuity between the terminal and its source. If 46 is not grounded operate SSSW and obtain gnd.

Table 2-4. Control Sequence Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
			(6) If 21 does not read ground connect the VTVM DC lead to TP1. A 0.6 volt reading should be obtained. If not, logic element 1 or 6 is bad. If it is obtained, element 18 is bad. (7) If all gnds are obtained, connect the oscilloscope channel A INPUT lead to terminal 33 and set the oscilloscope to + internal sync lead to terminal 42. The trace obtained should be a positive pulse, 100 to 170 msec wide occurring every (2 to 4) seconds in time. (8) If this is not obtained there may be discontinuity between terminal 33 and its source, requiring a continuity check. Disconnect oscilloscope setup. (9) If this pulse is obtained, connect the VTVM DC lead to terminal 11. A +5 volt reading should be obtained. If it is, logic element 2, 3 or 19 is bad, provided that a VTVM measurement at the junction of pin 10, logic element 21 and resistor R4 is ground. If it is, logic element 21 may be defective. If it is not logic element 24, 11, or 21 is defective. (10) If the test point TP1 reading (step (6)) is not obtained, connect the VTVM DC lead to terminal 11. A +3.7 volt reading should be obtained. If it is not, there is discontinuity between terminal 11 and its source, requiring a continuity check. (11) If it is, logic element 25, 21 or 16 is defective. (12) If ground is not observed at terminal 46 (step *g*), logic element 21, 22, 23, 2, or 3 is defective. Disconnect VTVM setup.
21a	ACK-1T Lamp does not light.	TRANSMIT START ACKNOWLEDGE SEQUENCE, Card A2A11.	Perform steps (1) through (7) of item 18a.
21b	ACK-1R Lamp does not light.	RECEIVE CONTROL SEQUENCES, Card A2A3.	Perform steps (1) through (7) of item 18b.
21c	CANCEL XMITTED Lamp does not light.	TRANSMIT CANCEL, STOP SEQUENCE, Card A2A9.	Perform steps (1) through (7) of item 16a.
21d	ACK-2T Lamp does not light.	TRANSMIT START ACKNOWLEDGE SEQUENCE, Card A2A11.	Perform steps (1) through (7) of item 16b.
21e	ACK-2R Lamp does not light.	RECEIVE CONTROL SEQUENCE Card A2A9.	Perform steps (1) through (7) of item 16c.
21f	MONITOR Lamp does not light (Test CANCEL Control Sequence only).	CANCEL Control Sequence Generating Logic Card A2A9.	(1) Remove Card A2A9 from logic rack and inser card extender in its place. (2) Connect Card A2A9 to the Card Extender. Obtain an oscilloscope. Set the oscilloscope up the same way as in item 17, step (12).

Table 2-4. Control Sequence Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
			(3) Connect the channel A INPUT lead to TP1 of card A2A9. The trace observed should be two positive pulses 167 milliseconds apart for 45.45 baud operation and 110 milliseconds apart for 75 or 74.2 baud operation, occurring every 2 to 4 seconds. (4) If these are obtained, discontinuity may exist between TP1 and the TCU intracabinet wiring to card A2A13. Disconnect oscilloscope setup. (5) If these pulses are not obtained, repeat this test, this time with the channel A INPUT Lead connected to terminal 8. The results should be similar to the above except the pulses should be negative. (6) If these are not obtained, there may be discontinuity between terminal 8 and the TCU intracabinet wiring from Card A2A8. Disconnect oscilloscope setup. (7) If these pulses are obtained, connect the oscilloscope channel A INPUT Lead to terminal 22. Place the TIME/CM Control to 1 sec. The trace obtained should be +3.7 volts, every (2 to 4) seconds with a duration of 245 milliseconds (for 74.2 or 75 baud operation) or 350 milliseconds (for 45.45 baud operation.) If these are obtained Logic Element 6 is defective. Disconnect oscilloscope setup. (8) Check for ground with the VTVM at terminals 14 and 43. If either of these is not present, there is, discontinuity between the terminal and its source requiring a continuity check. (9) If they are present, connect the oscilloscope channel A INPUT Lead to terminal 41 the TIME/CM control to 1 SEC and observe a pulse with a repetition rate of (2 to 4 seconds). If this is not obtained, there may be discontinuity between terminal 41 and its source. Disconnect oscilloscope setup. (10) If the correct trace is obtained, Logic Element 8, 17, 3 or 12 is defective. This may be further isolated by connecting the VTVM DC lead to terminal 19 and observing +3.7 volts. If this is obtained, logic element 8, 17, or 12 is defective. If this is not obtained, logic element 3 or 8 is defective.
22a	ACK-1T Lamp does not light.	Logic Card A2A11	Perform steps (1) through (7) of item 18a.
22b	ACK-1R Lamp does not light.	Logic Card A2A3	Perform steps (1) through (7) of item 18b.
22c	AUTO MES RT Lamp does not light.	Logic Card A2A10	(1) Remove Card A2A10 from the logic rack. (2) Insert a Card Extender into the A2A10 slot. (3) Connect Card A2A10 to the card extender. (4) Connect the VTVM common lead to Terminal 4. (5) Connect the VTVM DC lead to Terminal 54 and observe a ground. If this is observed, there may be discontinuity between terminal 54 and the Control Indicator Panel.

Table 2-4. Control Sequence Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
			(6) If ± 11 volts is measured, connect the VTVM DC lead to Terminal 24 and observe a +3.7-volt reading. If this is obtained, the network consisting of R1, R3, C5, and Q1 is bad. (7) If the +3.7-volt reading is not obtained, connect the channel A INPUT Lead of an oscilloscope to test point TP2. (8) Set the oscilloscope TIME/CM control to 1 SEC. (9) The trace observed should be two positive pulses, +3.7 volts in amplitude, occurring approximately every 2–4 seconds. (10) If the trace of step (9) is not observed, connect the oscilloscope channel A INPUT lead to terminal 26 and observe a similar waveform except the pulses are negative. If these are not observed, there may be discontinuity between terminal 26 and Card A2A8. (11) If the correct trace is observed, successively connect the VTVM DC lead to terminals 44 and 25 observing a ground each time and to test point TP1, observing +3.7 volts. If these are all observed, Logic element 18, 13, 20, or 14 is defective. (12) If 44 or 25 are not ground there may be a short circuit condition, or a discontinuity between those pins and A2A9. (13) If TP1 is not 3.7 volts, connect the VTVM DC lead to terminal 39 and observe a +3.7-volt reading. If this is observed, logic element 1 or 6 is defective. (14) If +3.7 volts is not obtained, there may be discontinuity between Terminal 39 and the Simulation Test Unit.
22d	ALARM lamp does not light.	(1) Card A2A19	(1) Remove Card A2A19 from the logic rack. Insert the Card Extender into the A2A19 slot. Connect Card A2A19 to the Card Extender. (2) Connect the VTVM common lead to terminal 3. (3) Connect the VTVM DC lead to Terminal 7. A 0.0 reading indicates there is discontinuity between Terminal 7 and the Control Indicator Panel. (4) If +11v is measured at Terminal 7, connect the DC VTVM lead to the junction of pin 10 of logic element 23 and R3. A +3.7-volt reading should be obtained. If it is, the network consisting of R3, C5, and Q1 is defective. The trouble can be isolated by checking R3, Q1 and C5. (5) If the +3.7 volts is not obtained, connect the VTVM DC lead to the junction of pin 4 logic element 25 and R5. A +3.7-volt reading should be obtained. If it is, Logic Element 23 or 25 is defective. (6) If it is not, there is discontinuity between Terminal 25 and Card A2A14. Disconnect VTVM setup.

Table 2-4. Control Sequence Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
22d	ALARM lamp does not light.	(2) Card A2A14	(1) Remove Card A2A14 from the logic rack. Insert the Card Extender into the A2A14 slot. Connect Card A2A14 to the Card Extender. (2) Connect the common VTVM lead to terminal 3. (3) Connect the DC VTVM lead to terminal 6. A +3.7-volt reading should be obtained. If it is, there is discontinuity between Terminal 6 and Card A2A19. (4) If it is not, connect the VTVM DC lead to the junction of Logic Element 17, pin 4 and R2. A reading of +3.7 volts should be obtained. If it is not, either Logic Element 16 is defective or there is discontinuity between terminal 33 and the Control Indicator Panel. (5) If the +3.7 volts is obtained, check the Simulator Test Panel to see that the ACK-1R lamp is illuminated. If it is, either Logic Element 17 is defective or there is discontinuity between Terminal 26 and Card A2A11. Disconnect VTVM setup.
22e	AUDIBLE ALARM does not sound.	(1) ALARM itself	Check the alarm by operating the Control Indicator Panel Test switch. If the alarm does not sound, the alarm itself is defective and has to be replaced.
22e		(2) Card A2A14	(1) If the alarm does sound, Remove Card A2A14 from the logic rack. Insert the card Extender into the A2A14 slot. Connect Card A2A14 to the Card Extender. (2) Obtain an oscilloscope. (3) Connect the oscilloscope channel A INPUT lead to terminal 51 and place the TIME/CM Control to .5 sec. A symmetrical square wave should be obtained with limits of −12 v and +12 volts (depending on potentiometer setting) with a duration and frequency of ½ second. If −12 v is not present there is discontinuity between Terminal 51 and the Control Indicator Panel. In this case disconnect oscilloscope setup. (4) If −12 v is present connect the oscilloscope channel A INPUT lead to the junction of R6 and R7. A +12 to 0 v square wave should be obtained. If it is, R6, R7, or Q3 is bad. This can be isolated by checking components. In this case, disconnect oscilloscope setup. (5) If the square wave is not obtained, connect the oscilloscope channel A INPUT lead to the junction of Logic Element 18, pin 2 and R4. A square wave varying between 1.0 v to 3.7 v should be seen. If it is, R4, R5, CR1, or Q2 is bad. This can be isolated by checking R4, R5, CR1 and Q2. Disconnect oscilloscope setup. (6) If the correct result is not obtained, connect the VTVM common lead to terminal 27. (7) Connect the VTVM DC lead to terminal 50. A 0.6 v reading should be obtained. If it is not, there is discontinuity between terminal 50 and Card A2A19.

Table 2-4. Control Sequence Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
			(8) If 0.6 v is measured connect the oscilloscope channel A INPUT Lead to Terminal 56. Similar results to step (5) should be obtained except the limits are ground and +3.7 volts. If the correct trace is observed, Logic Element 18 is defective. Disconnect oscilloscope setup. (9) If the correct trace is not observed, refer to trouble chart, Control sequence, items 2, 5, 8, 11, 15, 22 and 23 card A2A14. Disconnect VTVM setup.
22e		(3) Card A2A19	(1) Remove Card A2A19 from the logic rack. Insert the Card Extender into the A2A19 slot. Connect Card A2A19 to the Card Extender. (2) Connect the VTVM COMMON lead to terminal 3. (3) Connect the VTVM DC lead to terminal 11. A 0.6 v indication should be obtained. (4) If 3.7v is measured, connect the VTVM DC lead to Terminal 25. A +3.7 volt reading should be obtained. If it is, either R5, C8, C9, CR2, or Logic Element 23 or 18 is defective.
22f	CANCEL XMITED Lamp does not light.	TRANSMIT CANCEL STOP SEQUENCE, Card A2A9.	Perform steps (1) through (7) of item 16a.
22g	ACK-2T Lamp does not light.	TRANSMIT START ACKNOWLEDGE SEQUENCE, Card A2A11.	Perform steps (1) through (7) of item 16b.
22h	ACK-2R Lamp does not light.	RECEIVE CONTROL SEQUENCE, Card A2A3.	Perform steps (1) through (7) of item 16c.
22i	MONITOR lamp does not light (Test RT Control Sequence only).	RETRANSMIT CONTROL Sequence Generating logic. Card A2A10.	(1) Obtain the oscilloscope and connect the channel A INPUT lead to TP2. The setup is the same as ITEM 17, step 1. Also the results are similar, except the two pulses occur every second. (2) If they are present, there is discontinuity between pin 50 and the intra TCU cabinet wiring to Card A2A19. A continuity check is thus required. Disconnect oscilloscope setup. (3) If these pulses do not appear, successively connect the DC lead of the VTVM to terminals 25 and 44, observing a 0.6 v at each point. (4) If both readings are not 0.6 v there is discontinuity between terminals 25 to 44 and the TCU intra cabinet wiring. In this case, a continuity check should be made. (5) If both grounds are present, Connect the Channel A INPUT Lead of the oscilloscope to terminal 26. The trace observed should be similar to the above, except the pulses are negative and they occur approximately every 2-4 second. If these are not obtained, there is discontinuity between terminal 26 and the TCU Cabinet wiring from card A2A8 which requires a continuity check. Disconnect oscilloscope setup.

Table 2-4. Control Sequence Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
			(6) If these pulses are present, either Logic Element 18 or 14 is defective, provided that a VTVM check with the DC lead connected to TP1 results in a reading of +3.7 volts. (7) If this reading is not obtained connect the DC lead of the VTVM to Terminal 39 and observe a reading of +3.7 volts. If this is obtained either Logic Element 1 or 6 is bad. (8) If the +3.7 volts is not obtained, there is discontinuity between Terminal 39 and the intra TCU wiring from the Simulator Control panel. Perform a continuity check. Disconnect VTVM setup.
23a	STOP lamp does not flash.	(1) Card A2A10	(1) Remove Card A2A10 from the logic rack. Insert the Card Extender into the A2A10 slot. Connect Card A2A10 to the ard Extender. (2) Connect the oscilloscope Channel A INPUT Lead to Terminal 55 and place the TIME/CM control to .5 sec. (3) The trace obtained should be a symmetrical square wave with limits of ground and +11 volts and a duration of ¼ second. (4) If a 0.0 volt reading is obtained, there is discontinuity between terminal 55 and the Control Indicator Panel. In this case disconnect oscilloscope setup. (5) If 11 volts is measured at pin 55, connect the oscilloscope Channel A INPUT Lead to the junction of Logic Element 7, pin 10 and R7. 0.6 to 3.7 v square wave should be obtained as in step (3). (6) If the correct trace is obtained, the network consisting of R7, R8, C7, and Q2 is bad. The trouble can be isolated by checking R7, R8, and C7. In this case, disconnect oscilloscope setup. (7) If the correct trace is not obtained, connect the oscilloscope Channel A INPUT Lead to terminal 45. The results obtained should be the same as step (5). If it is not, there is discontinuity between terminal 45 and Card A2A14. In this case, disconnect oscilloscope setup. (8) If the correct trace is obtained, connect the VTVM DC lead to terminal 47. A +3.7-volt reading should be obtained. If it is, Logic Element 7 is bad. If it is not, Logic Element 10 or 4 or 9 is defective. Disconnect oscilloscope setup. *Note.* Logic Element 11 may also be defective in this case, but it would not cause the TRANSMIT STOP Lamp not to light.
		(2) Card A2A14	(1) Remove Card A2A14 from the logic rack. Insert the Card Extender into the A2A14 logic rack slot. Connect Card A2A14 to the card extender. (2) Connect the oscilloscope channel A INPUT Lead to Terminal 56. (3) Place the TIME/CM control to .5 sec. The results obtained should be a symmetrical square wave with limits of 0.6 v and +3.7 volts with a duration of ¼ second.

Table 2-4. Control Sequence Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
			(4) If the correct trace is not obtained, refer to item 17, 18c, 19c, 20, 21f, 24f, 22i, 25b, 23b, Card A2A14.
23b	MONITOR lamp does not light (STOP Control Sequence only).	STOP Control Sequence Generating logic. Card A2A9.	(1) Obtain the oscilloscope. Connect the channel A INPUT Lead to TP2. (2) With this exception set up the oscilloscope the same as in ITEM 17, step 1. The results should be similar, except that the pulses should be obtained about every 1 second. (3) If these pulses are obtained, there may be discontinuity between Pin 18 and the TCU intra cabinet wiring to card A2A19. In this case, perform a continuity check. Disconnect oscilloscope setup. (4) If these pulses are not obtained, connect the Channel A INPUT lead of the oscilloscope to terminal 8. The results here should be the same as above, except the pulses should be negative. (5) If these pulses are not obtained, there is discontinuity between terminal 8 and the TCU intra cabinet wiring from Card A2A8. (6) If these pulses are obtained, perform the following procedures after disconnecting oscilloscope setup. (7) Connect the DC lead of the VTVM to terminal 22, and observe a 0.6 volt reading. (8) If the ground is present, obtain the oscilloscope and connect the channel A INPUT lead to terminal 41. Set up the oscilloscope similarly to that in ITEM 18c step (3). The trace obtained should be the same. (9) If it is not, there may be discontinuity between terminal 41 and the TCU intra cabinet wiring from card A2A14. Disconnect oscilloscope setup. (10) Connect the DC lead of the VTVM to terminal 17 and observe a reading of +3.7 volts. (11) If this is not obtained, discontinuity exists between terminal 17 and the TCU intra cabinet wiring from the simulator Test Panel. If the +5 volts is obtained, Logic Element 7, 13, 14, 15, 6 or 9 is bad. Disconnect VTVM setup.
23c	CANCEL XMITED Lamp does not light (Test CANCEL Control Sequence only).	TRANSMIT CANCEL, STOP SEQUENCE Card, A2A9.	Perform steps (1) through (7) of item 16a.
24a	ACK-1T Lamp does not light.	TRANSMIT START ACKNOWLEDGE SEQUENCE, Card A2A11.	Perform steps (1) through (7) of item 18a.
24b	ACK-1R Lamp does not light.	RECEIVE CONTROL SEQUENCES, Card A2A3.	Perform steps (1) through (7) of item 18b.
24c	CANCEL XMITTED Lamp does not light.	TRANSMIT CANCEL, STOP SEQUENCE, Card A2A9.	Perform steps (1) through (7) of item 16a.

Table 2-4. Control Sequence Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
24d	ACK-2T Lamp does not light.	TRANSMIT START ACKNOWLEDGE SEQUENCE, Card A2A11.	Perform steps (1) through (7) of item 16b.
24e	ACK-2R Lamp does not light.	RECEIVE CONTROL SEQUENCE, Card A2A9.	Perform steps (1) through (7) of item 16c.
24f	MONITOR Lamp does not light (Manual CANCEL control sequence only).	CANCEL Control Sequence Generating Logic, Card A2A9.	Perform steps (1) through (10) of item 21f.
25a	MONITOR Lamp does not light (Manual RT Control Sequence only.)	RETRANSMIT CONTROL Sequence Generating Logic, Card A2A10.	Perform steps (1) through (8) of item 22i.
25b	AUDIBLE ALARM does not sound.	Card A2A14	Perform steps (a) through (i) of item 22e(2).
		Card A2A19	Perform steps (a) through (e) of item 22e(3).
18c	MONITOR lamp does not light (ACK-1 Control Sequence only).	ACK-1 Control Sequence Generating Logic. CARD A2A4.	(1) Remove Card A2A4 from its slot in the logic rack. (2) Insert a card extender into the slot normally occupied by Card A2A4. (3) Connect Card A2A4 to the Card Extender. (4) Connect the COMMON lead of the VTVM to terminal 3 and the DC lead of the VTVM to terminal 23. Observe a reading of +3.7 volts. If this is present, there may be discontinuity between terminal 23 and the TCU intra cabinet wiring to card A2A11. (5) If the +3.7 volts is not obtained, connect the DC lead of the VTVM to terminal 24 and observe a reading of +3.7 volts. If this is obtained, Logic Element 17 is defective. If the +3.7 volts is not obtained, there may be discontinuity between Terminal 24 and the Test Simulator Panel. Disconnect VTVM setup.
19c	MONITOR lamp does not light (ACK-2 Control Sequence only).	ACK-2 Control Sequence Generating Logic (CARD A2A4).	(1) Remove Card A2A4 from its slot in the logic rack. (2) Insert a card extender into the slot normally occupied by Card A2A4. (3) Connect Card A2A4 to the Card Extender. (4) Connect the COMMON lead of the VTVM to terminal 3 and the DC lead of the VTVM to terminal 22. (5) Observe a reading of +3.7 volts. If this is present, there exists discontinuity between terminal 22 and the TCU intracabinet wiring to Card A2A11. In this case a continuity check should be performed. (6) If the +3.7 volts is not present, connect the DC lead of the VTVM to terminal 7 and observe a reading of +3.7 volts. If this is present, either Logic Element 12 or 17 is defective. If the +3.7 volts is not present, there exists discontinuity between terminal 7 and the Simulator Control Panel wiring. In this case, perform a continuity check. Disconnect VTVM setup.

Table 2-4. Control Sequence Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
17	MONITOR lamp does not light (START control Sequence only).	START Decoding logic in the Receive Buffer, Card A2A2.	The malfunction occurred only during the start control sequence resulting in the fact that Card A2A2 is faulty. Therefore, because the only logic associated exclusively with START is Logic Element 14 and 2, either Logic Element 14 or 2 is defective or there is discontinuity between Terminal 21 and the TCU intra cabinet wiring to Card A2A3.
18c	MONITOR lamp does not light (ACK-1 Control Sequence only).	ACK-1 decoding logic in the Receive Buffer, Card A2A2.	Same as item 17 except that the trouble is either Logic Element 2 or 12 or discontinuity from Terminal 12 to Card A2A3.
19c	MONITOR lamp does not light (ACK-2 Control Sequence only).	ACK-2 decoding logic in the Receive Buffer, Card A2A2.	Same as item 17, except that the trouble is either Logic Element 2 or 12 or discontinuity from Terminal 13 to Card A2A3.
20	MONITOR lamp does not light (REPEAT Control Sequence only).	REPEAT decoding logic in the Receive Buffer, Card A2A2.	Same as item 17 except that the trouble is either Logic Element 7 or 17, or discontinuity from Terminal 10 to Card A2A3.
21f, 24f	MONITOR lamp does not light (Both Test and Manual CANCEL).	CANCEL decoding logic in the Receive Buffer, Card A2A2.	Same as item 17 except that the trouble is either Logic Element 7 or 17, or discontinuity from Terminal 11 to Card A2A3.
22i, 25a	MONITOR lamp does not light (Both Test and Manual RT).	RETRANSMIT decoding logic in the Receive Buffer, Card A2A2.	Same as item 17 except that the trouble is either Logic Element 7 or 9 or discontinuity from Terminal 16 to Card A2A3.
23b	MONITOR lamp does not light (STOP Control Sequence only).	STOP decoding logic in Receive Buffer, Card A2A2.	Same as item 17, except that the trouble is either Logic Element 14 or 2 or discontinuity from terminal 20 to Card A2A3.
17	MONITOR lamp does not light (START control Sequence only).	START pulse decoding logic, Card A2A3.	The malfunction occurred only during the START Control sequence resulting in the fact that Card A2A3 is faulty. The logic in Card A2A3 used exclusively for START is Logic Elements 24 and 23. Thus either Logic Element 24 or 23 is defective or there is discontinuity between terminal 14 and the TCU intracabinet wiring to the Test Simulator Panel.
18c	MONITOR lamp does not light (ACK-1 Control Sequence only).	ACK-1 pulse decoding logic, Card A2A3.	Same as item 17 except that the trouble is either Logic Element 13 or 8, or discontinuity from Terminal 16 to the Simulator Test Panel.
19c	MONITOR lamp does not light (ACK-2 Control Sequence only).	ACK-2 pulse decoding logic, Card A2A3.	Same as item 17, except that the trouble is either Logic Element 8 or 19, or discontinuity from Terminal 21 to the Simulator Test Panel.
20	MONITOR lamp does not light (REPEAT Control Sequence only).	REPEAT pulse decoding logic, Card A2A3.	Same as item 17, except that the trouble is either Logic Element 7 or 6, or discontinuity from terminal 11 to the Simulator Test Panel.
21f, 24f	MONITOR lamp does not light (Both Test and Manual CANCEL).	CANCEL pulse decoding logic, Card A2A3.	Same as item 17, except that the trouble is either Logic Element 7 or 11, or discontinuity from terminal 17 to the Simulator Test Panel.

Table 2-4. Control Sequence Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
22i, 25a	MONITOR lamp does not light (Both Test and Manual RT).	RETRANSMIT pulse decoding logic, Card A2A3.	Same as item 17, except that the trouble is either Logic Element 16 or 17, or discontinuity from terminal 8 to the Simulator Test Panel.
23b	MONITOR lamp does not light (STOP control sequence only).	STOP pulse decoding logic, Card A2A3.	Same as item 17, except that the trouble is either Logic Element 16 or 12 or discontinuity from Terminal 7 to the Simulator Test Panel.
17	MONITOR lamp does not light (START Control Sequence only).	START Control Sequence encoding logic, Card A2A19.	The malfunction occurred only during the START control sequence, resulting in the fact that Card A2A19 is faulty. The only logic on Card A2A19 used during START is Logic Elements 9, 13, and 14. Thus, either Logic Elements 13 or 9 or 14 is defective or there is discontinuity between terminal 40 or 41 to Card A2A18, or between terminals 48, 20, 46, 16, 17, 49, or 21 from cards A2A11, A10, A9. Perform the following procedure: (1) Obtain Oscilloscope. (2) Connect the oscilloscope channel A INPUT Lead to terminal 40 of Card A2A19. (3) Set the oscilloscope to +INT SYNC. (4) Set the oscilloscope TIME/CM switch to 20 μsec. The trace obtained should be two positive pulses (167 millisec apart for 45.45 baud and 110 millisec apart for 75 or 74.2 baud), every one second. (5) Place the oscilloscope channel A INPUT Lead to terminal 41 and observe the same results. If both are obtained, the trouble is discontinuity between terminal 41 or 40 (or both) and Card A2A18 and a continuity check is required. Disconnect oscilloscope setup. (6) If both the above (terminal 40 and 41) are missing, connect the oscilloscope Channel A INPUT Lead to terminal 48 and observe the same results. If it is not obtained, there is discontinuity between terminal 48 and Card A2A11. In this case a continuity check is required. Disconnect the oscilloscope setup. (7) If the procedure above yields a correct trace and both of the traces originally measured (terminals 40 and 41) are missing, either logic element 13 or 14 and 19 are bad.
18c	MONITOR LAMP does not light (ACK-1 Control Sequence only).	ACK-1 Control Sequence Encoding Logic, Card A2A19.	The procedure and results of the test for this trouble is similar to item 17 above, except for following differences: (1) The card A2A19 input terminal is 20. (2) The card A2A19 output terminals are 13 and 22. (3) The Logic Elements to be suspected are 9, 4, 8, 15, and 19.
19c	MONITOR LAMP does not light (ACK-2 control sequence only).	ACK-2 Control Sequence Encoding Logic, Card A2A19.	The Procedure and results of the test fgjthis trouble is similar to item 17, except for the following differences. (1) The card A2A59 input terminal is 46. (2) The card A2A19 output terminals are 13 and 40. (3) The logic elements to be suspected are 4, 8, 14, and 13.

Table 2-4. Control Sequence Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
20	MONITOR LAMP does not light (REPEAT Control Sequence only).	REPEAT Control Sequence Encoding Logic, Card A2A19.	The procedure and results of the test for this trouble is similar to item 17 except for the following differences. (1) The Card A2A19 input terminal is 16. (2) The Card A2A19 output terminals are 14 and 40. (3) The Logic Elements to be suspected are 9, 8, 14 and 13.
21f, 24f	MONITOR LAMP does not light (Both Test and Manual CANCEL).	CANCEL Control Sequence Encoding Logic, Card A2A19.	The procedure and results of the test for this trouble is similar to item 17 except for the following differences: (1) The Card A2A19 input terminal is 17. (2) The Card A2A19 output terminals are 14 and 22. (3) The Logic Elements to be suspected are 9, 8, 15 and 19.
22i, 25a	MONITOR LAMP does not light (Both Test and Manual RT).	RETRANSMIT Control Sequence Encoding logic, Card A2A19.	The procedure and results of the test for this trouble is similar to item 17 except for the following differences: (1) The Card A2A19 input terminal is 49. (2) The Card A2A19 output terminals are 41 and 22. (3) The Logic Elements to be suspected are 9, 13, 15, and 19.
23b	MONITOR LAMP does not light (STOP control sequence only).	STOP Control Sequence Encoding logic, Card A2A19.	The procedures and results of the test for this trouble is similar to item 17 except for the following differences: (1) The Card A2A19 input terminal is 21. (2) The Card A2A19 output terminals are 40 and 22. (3) The Logic Elements to be suspected are 14, 13, 15 and 19.
17, 22i, 25a	MONITOR LAMP does not light (Test START, Test RT, and Manual RT).	START and RT Control Sequence Transmit Buffer Decoder Logic, Card A2A18.	If only the START and RT Control sequences fail to function properly and Card A2A18 is malfunctioning, there is either discontinuity between terminal 10 of Card A2A18 and Card A2A19 or between terminal 10 of Card A2A18 and pin 3 of Logic Element 12. An oscilloscope check should then be made with the channel A INPUT Lead connected to Terminal 10. The trace should be the same as the previous item 17. If it is not the discontinuity is between terminal 10 and Card A2A19. Disconnect oscilloscope setup. If it is, discontinuity exists between terminal 10 and pin 3 of Logic Element 12.
17, 19c, 20, 23b	MONITOR LAMP does not light (Test START, Test ACK-2, Test REP, and Test STOP).	START, ACK-2, REP, and STOP Control Sequence Transmit Buffer Decoder Logic, Card A2A18.	START, ACK-2, REP, and STOP control sequences fail to function properly. Procedure and Results similar to items 17, 22i, 25a above except that terminal 12 and pin 3 of Logic Element 7 should be checked.
18c, 19c	MONITOR LAMP does not light (Test ACK-1 and Test ACK-2).	ACK-1 and ACK-2 Control Sequence Transmit Buffer Decoder Logic, Card A2A18.	ACK-1 and ACK-2 control sequences fail to function properly. Procedure and Results similar to items 17, 22i, 25a above except that terminal 9 and pin 3 of Logic Element 6 should be checked.
20, 21f, 24f	MONITOR LAMP does not light (Test REP, Test CANCEL, and Manual CANCEL).	REP and CAN Control Sequence Transmit Buffer Decoder Logic, Card A2A18.	REP and CAN control sequences fail to function properly. Procedure and Results similar to items 17, 22i, 25a above except that terminal 13 and pin 3 of Logic Element 11 should be checked.
18c, 19c, 22i, 25a	MONITOR LAMP does not light (Test ACK-1, Test ACK-2, Test RT, and Manual RT).	ACK-1, ACK-2 RT Control Sequences, Card A2A14.	Logic Element 4 may be defective.

Table 2-4. Control Sequence Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
18c, 21f, 24f, 22i, 25b, 23b	**MONITOR LAMP does not light (Test ACK-1, Test CANCEL, Manual CANCEL, Test RT, Manual RT, and Test STOP).**	**ACK-1, CAN, RT, and STOP Control Sequence Transmit Buffer Decoder Logic, Card A2A18.**	**ACK-1 CAN, RT, and STOP Control Sequences fail to function properly. Procedure and Results similar to items 17, 22i, 25a except that terminal 12 and pin 3 of Logic Element 7 should be checked.**
17, 18c, 19c, 20, 22i, 25b, 23b	**MONITOR LAMP does not light (All Control Sequences except CANCEL).**	**Cancel Reset Logic, Card A2A9.**	**Logic Element 18 may be defective.**
17, 18c, 19c, 20, 21f, 24f, 22i, 25a, 23b	MONITOR LAMP does not light (All Control Sequences).	FLGS level, Card A2A11 is disabled.	The FLGS level is generated during the transmission of all control sequences. If none of the control sequences checks out Logic Elements 24 and 4 may be defective.
17, 18c, 19c, 20, 21f, 24f, 22i, 25a, 23b	MONITOR LAMP does not light (All Control Sequences).	Transmit Buffer Logic, Card A2A18.	If no control sequences check out, and card A2A18 has been revealed to be malfunctioning, the Transmit Buffer is malfunctioning. Perform the following procedure: (1) Connect the oscilloscope channel A INPUT Lead to TP3. Set the oscilloscope to −INT SYNC and the TIME/CM Control to 20 msec. (2) Place the Simulator Test Panel RECEIVE and TRANSMIT switches to START position. The trace obtained on the oscilloscope should be two consecutive trains, each identical, with limits of +3.7 volts and ground. Each train should consist of a symmetrical square wave with a 13.4 millisecond duration (For 74.2 or 75 baud operation) or a 22 millisecond duration (For 45.45 baud operation). (3) If obtained, there is discontinuity between TP3 and card A2A7, necessitating a possible continuity check. Disconnect oscilloscope setup. (4) If this is not obtained, connect the oscilloscope Channel A INPUT Lead to terminal 35. (5) Position the oscilloscope TIME/CM switch to 20 msec for all baud rates. (6) Place the Simulator Test Panel TRANSMIT and RECEIVE Switches to one of the Control Sequence positions. The oscilloscope trace should be a group of 6 positive 5 μsec pulses spaced 22 milliseconds apart for 45.45 baud and 13.4 milliseconds apart for 75 or 76.2 baud. These should reoccur in 2 successive groups, repeated approximately every second. (7) If these are not obtained, there is discontinuity between Terminal 35 of Card A2A18 and card A2A8 necessitating a continuity check. Disconnect oscilloscope setup. (8) If these pulses are obtained the trouble may be either Logic Element 1, 4, 8, 10, or the Transmit Buffer which consists of Logic Elements 6, 11, 12, 7, 9, 14, and 15.

Table 2-4. Control Sequence Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
			(9) Another possibility is that the Transmit Baud Counter is not receiving the Buffer full. signal. This can be checked by connecting the VTVM DC lead to terminal 7. (10) A +3.7 volt reading should be obtained. If it is not, Logic element 2 may be defective.
17, 18c, 19c, 20, 21e, 24f, 22i, 25a, 23b	MONITOR LAMP does not light (All Control Sequences).	Receive Buffer Logic Card A2A2.	If no control sequences check out and Card A2A2 has been determined to be the malfunctioning card, perform the following: (1) Disconnect Card A2A2 from the logic rack. (2) Connect the Card Extender to the A2A2 slot. (3) Connect Card A2A2 to the Card Extender. (4) Place the Simulation Test Unit TRANSMIT and RECEIVE switches to START position. (5) Connect VTVM COMMON lead to terminal 27. (6) Connect VTVM DC lead to Terminal 7 and observe 0.6 volt. If this is obtained there may be discontinuity between terminal 7 and the Simulation Test Unit. (7) If +11.0 v is measured at terminal 7 connect the VTVM DC lead to the junction of pin 10 of Logic Element 15 and Resistor R2 observing +3.7 volts. If this is obtained the network consisting of R2, C5, and Q1 is bad. This can be isolated further by checking R2, and C5. (8) If this is not obtained, connect scope lead to Terminal 25, observing +3.7 volt pulse. If this is observed, Logic Element 15 is bad. (9) If this is not obtained, proceed to step (10). (10) Connect the input of the Channel A INPUT Lead of the oscilloscope to terminal 57 and place the TIME/CM Control to 20 msec. (11) Place the Test Simulator Panel TRANSMIT and RECEIVE switches to the START position. (12) The trace obtained should be the same as step (2). of the A2A18 items. If this is not obtained, there is discontinuity between Terminal 57 and the Control Indicator Panel. Disconnect Oscilloscope setup. (13) If this trace is obtained, proceed to step (14). (14) Connect its Channel A INPUT Lead to terminal 14. Set the oscilloscope to + INT SYNC. (15) Position the oscilloscope TIME/CM switch to 20 msec for all baud rates. (16) Place the Simulator Test Panel TRANSMIT and RECEIVE switches to one of the Control Sequence positions. The oscilloscope trace should be a group of 6 positive pulses, spaced 22 milliseconds apart for 45.45 baud operation and 13.3 milliseconds apart for 75 or 74.2 baud operation. These should reoccur, in two successive groups at frequent intervals. (17) If these are not obtained; there is discontinuity between terminal 14 and Card A2A6. Disconnect oscilloscope setup.

Table 2-4. Control Sequence Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
			(18) If the proper trace is obtained, connect the oscilloscope channel A INPUT Lead to TP2 and note the same results as step (16). If the proper trace is obtained, proceed to step (19). If the proper trace is not obtained, Logic element 10 is defective. (19) If the proper trace is obtained, connect the oscilloscope channel A INPUT Lead to TP1. The trace obtained should be the same as step (16). (20) If it is, either Logic Element 4, 5, 10, or the Receive Buffer consisting of Logic Element 3, 8, 13, 18, 23, 24, or 25 is bad. Disconnect oscilloscope setup. (21) If the trace of step (18) is not obtained, the conversion network, consisting of Q2 and Q3 is defective.
17, 18c, 19c, 20, 21f, 24f, 22i, 25b, 23b	MONITOR LAMP does not light (all control sequences).	TIMING GENERATOR logic card, A2A7.	If no control sequences test successfully and Card A2A7 has been determined to be faulty, check it as follows: Check the following A2A7 outputs at their terminals: BCRN-37. BCTN-34. CSTP-42. BCTP-33. HSCL-41. BCRP-38. Do this by checking these signals according to the following setups. *a.* BCRN, BCRP Procedure. (1) Remove Card A2A7 from the logic rack. (2) Insert the Card extender into the A2A7 slot. (3) Connect Card A2A7 to the card extender. (4) Connect the Channel A INPUT Lead of the oscilloscope to Terminal 37 (BCRN). (5) Connect the channel B INPUT Lead to terminal 38 (BCRP). Connect EXT SYNC Lead to terminal 37. (6) Position the oscilloscope FUNCTION switch to CHOPPED. Place the oscilloscope TIME/CM switch to 10 msec. A trace should be obtained of coincident positive and negative pulses, 11 milliseconds apart (for 45.45 baud operation) or 6.65 milliseconds apart (for 74.2 or 75 baud operation). (7) If the intervals are incorrect, correct the situation by adjustment of the RECEIVE BAUD GENERATOR according to TM 5815-335-12. (8) If the pulses are correct or can be corrected by adjustment, proceed to the BCTN, BCTP procedure. Disconnect oscilloscope setup. (9) If pulses cannot be obtained, there is internal trouble in the Receive Baud Generator. In this case, continue this procedure. (10) If the positive pulse is not obtained but the negative pulse is, Logic Element 7 is bad. (11) If neither pulse is obtained, place the channel A INPUT Lead of the oscilloscope to the junction of resistors R46 and R47.

Table 2-4. Control Sequence Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
			(12) The trace should be pulses, positive, about 1 volt in amplitude, from 10 to 20 microseconds in width, and occurring at 11 msec on 6.65 msec depending on baud rate setting. (13) If these are obtained, either R47 or Q17 is bad. This can be isolated further by checking R47. (14) If the pulses are not obtained, place the oscilloscope Channel A INPUT Lead to the junction of Q16 and C25. The trace obtained should be a sawtooth voltage, 3.7 to 5.0 volts in amplitude, reoccurring at a rate selected by the baud setting. (15) If these are obtained, Q16 or R45 is bad. This can be narrowed down by checking R45. (16) If the proper trace is not obtained, either the combination of R37/R44/C25 is defective (45.45 baud operation) or R38/R43/C25 is defective (74.2 or 75 baud) or Q15 is bad. (17) These can be isolated further by checking the resistors and the capacitor. Disconnect oscilloscope setup. *b.* BCTN, BCTP Procedure. (1) For the Transmit Baud Counter perform the entire procedure in *a* above, except note the following differences: (*a*) Substitute Terminal 34 for 37. (*b*) Substitute Terminal 33 for 38. (*c*) Substitute TRANSMIT BAUD GENERATOR adjustment for RECEIVE BAUD GENERATOR adjustment (TM 11-5815-335-12). (*d*) Substitute the junction of R58 and R59 for R46 and R47. (*e*) Substitute Q20 for Q17. (*f*) Substitute the junction of Q19 and C27 for Q16 and C25. (*g*) Substitute R57 for R45. (*h*) Substitute R49/R56 for R37/R44 or R50/R55 for R38/R43. (2) If the point is reached where it is found that procedure A is not necessary to procedure C. The difference in the components and terminals of the Transmit Baud Generator and Receive Baud Generator can be readily seen by referring to the logic diagram for Card A2A7, (fig. 1-10). *c.* HSCL Procedure. (1) The High Speed Clock should first be checked. (2) Connect the oscilloscope channel A INPUT Lead to terminal 41. Set to − INT SYNC. (3) Place the oscilloscope TIME/CM switch to 50 μsec. The trace obtained should be negative pulses, approximately 1 every three centimeters and +3.7 volts in amplitude. (4) If these are obtained, refer to the CSTP procedure. If these are not obtained, there is internal trouble in the HIGH SPEED CLOCK, necessitating the following procedure:

Table 2-4. Control Sequence Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
			(5) Connect the oscilloscope channel A INPUT Lead to the junction of R26 and C21. Observe a Sawtooth waveform, approximately 3.7 volts in amplitude, and with the same repetition rate as above. (6) If this is obtained the bad component is either R27, R28, R35, R36, L5, or Q14. This can be isolated by checking. (7) If this is not obtained, the trouble is either R25 R26, Q10 or C21. This can be isolated by checking R25, R26, and C21. Disconnect oscilloscope setup. *d.* CSTP Procedure. (1) Connect the oscilloscope Channel A INPUT Lead to terminal 42. Use −INT SYNC. (2) Adjust the oscilloscope TIME/CM control to .2 sec. The trace obtained should be negative pulses, 3.7 volts in amplitude and one per 1¼ CM (for ¼ sec. operation) or one every 2½ CM. (For ½ sec. operation). (3) If these are obtained, there is discontinuity between terminals 42, 38, 33, 34, 37, or 41 and the wiring to the respective destination. This thus required a continuity check. Disconnect oscilloscope setup. (4) If the proper trace is not obtained, perform the following procedure: (5) Connect the oscilloscope Channel A INPUT Lead to the junction of R32 and R33. The trace observed should be positive pulses, 1 volt in amplitude, approximately 15 usec in width and the same frequency as above. (Step 2.) (6) If these are obtained, either R33, R34, 5L6, or Q13 is defective. This can be isolated by checking R33, L6 and R34. Disconnect oscilloscope setup. (7) If these traces are not obtained, connect the oscilloscope channel A INPUT Lead to the junction of CR8 and C23. Observe exponential positive traces, 5 to 6 volts in amplitude and with a frequency equal to that described above step (2). (8) If +5 v is measured, the problem is R31, R32 or Q12. This can be isolated by checking R31 and R32. Disconnect oscilloscope setup. (9) If 0.0 v is measured at CR8 and C23 junction, connect the oscilloscope channel A INPUT Lead to the junction of Q11 and C22. The trace obtained should be negative pulses 12 volts in amplitude, with a repetition rate of approximately 8 kc. (10) If these are obtained, the problem is either C22, C23, CR7, or CR8. Disconnect oscilloscope setup. (11) If these pulses are not obtained, the problem is either Q11, R30 or R29. This can be isolated by checking R30 and R29.

Table 2-4. Control Sequence Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
17, 18c, 19c, 20, 21f, 24f, 22i, 25b, 23b	MONITOR LAMP does not light (All Control Sequences).	INPUT DEVICE CONTROL, CARD A2A14.	If none of the control sequences checks out and Card A2A14 has been revealed to be the defective card, the CSSP pulse may not be applied where required to the logic. (1) Remove Card A2A14 from the logic rack. (2) Insert the Card Extender into the A2A14 slot. (3) Connect Card A2A14 to the card extender. (4) Obtain the oscilloscope. (5) Connect the oscilloscope Channel A INPUT Lead to terminal 47. (6) Place the oscilloscope TIME/CM Control to 1 sec. The trace obtained should be a train of positive pulses 100 to 170 msec wide, 3.7 volts in amplitude with one every 2 to 4 seconds. If these are obtained, there is discontinuity between terminal 47 and its destination, requiring a continuity check. Disconnect oscilloscope setup. (7) If the proper trace is not obtained, connect the oscilloscope Channel A INPUT Lead to terminal 16. (8) The trace obtained should be a positive pulse 3.7 volts in amplitude. (9) If the trace does not appear, there is discontinuity between terminal 16 and Card A2A8, requiring a continuity check. Disconnect oscilloscope setup. (10) If the proper trace is obtained, connect the oscilloscope Channel A INPUT Lead to terminal 58 and the TIME/CM switch .2 sec. (11) The trace obtained should be negative pulses, +3.7 volts in amplitude, occurring every ¼ second or ⅕ second (depending upon TCU setup). (12) If this is not obtained, there is discontinuity between terminal 58 and card A2A7, requiring a continuity check. Disconnect oscilloscope setup. (13) If the correct trace is obtained, and terminal 10 is 0.6 v and terminal 46 is 3.7 v there is trouble in the control sequence synchronizer. In this case either Logic Element 18, 20, 21, 22, 24, or 23 is defective.
17, 18c, 19c, 20, 21f, 24f, 22i, 25a, 23b	MONITOR lamp does not light (All Control Sequences).	RECEIVE BAUD COUNTER Card A2A6.	If none of the control sequences checks out properly and card A2A6 is revealed to be malfunctioning, it may be desirable to first check the receive shift pulses. (1) Remove Card A2A6 from the logic rack. (2) Connect the card extender to the space occupied normally by Card A2A6. (3) Connect Card A2A6 to the card extender. (5) Connect the oscilloscope Channel A INPUT Lead to terminal 8. (6) Connect the oscilloscope EXT INPUT Lead to terminal 8. (7) Position the oscilloscope TIME/CM to 20 msec (for all baud rates).

Table 2-4. Control Sequence Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
			(8) Place the Simulator Test Panel TRANSMIT and RECEIVE switch to the START position. The oscilloscope trace should be a group of 6 positive pulses, spaced 22 milliseconds apart for 45.45 baud operation and 13.3 milliseconds apart for 74.2 or 75 baud operation. These should reoccur in successive groups at frequent intervals. (9) If these are obtained, there may exist discontinuity between terminal 8 and its destination. In this case, disconnect oscilloscope setup. (10) If these pulses are not obtained, connect the oscilloscope channel A INPUT Lead to terminal 33 and place the TIME/CM control to 10 msec. The trace obtained should be negative pulses, falling to ground from +3.7 volts, with a time between pulses of 11 msec for 45.45 baud, and 6.67 msec for 74.2 baud or 75 baud. (11) If these are not obtained, there may be discontinuity between terminal 33 and the TCU wiring from Card A2A7. In this case disconnect oscilloscope setup. (12) If the proper trace is obtained, at terminal 33 connect the oscilloscope Channel A INPUT Lead to terminal 22. The trace obtained should be a symmetrical square wave of +5 volts and ground amplitude limits, with a duration (of each) of 44 milliseconds (for 45.45 baud operation) or 26.6 milliseconds (for 74.2 or 75 baud operation). This trace should reappear frequently in pairs. (13) If this trace is not obtained, there may be discontinuity between terminal 22 and the Control and Indicator Panel. In this case, disconnect the oscilloscope setup. (14) If these are obtained, connect the oscilloscope and channel A INPUT Lead to terminal 17 and the TIME/CM control to 20 msec. (15) The trace observed should be a square wave, with limits of +3.7 volts and ground. (16) If this trace is obtained, connect the oscilloscope Channel A INPUT Lead to TP2. (17) Set the oscilloscope to + INT SYNC and place the TIME/COM Control to 50 msec. (18) The trace obtained should be a positive pulse x 80 μsec wide, +3.7 volts in amplitude, followed by another, 176 milliseconds later (for 45.45 baud operation) or 106 milliseconds later (for 74.2 or 75 baud operation). Each pair should reoccur frequently. (19) If the proper trace is not obtained, connect the oscilloscope channel A INPUT Lead to terminal 24. If the proper trace is obtained, disconnect oscilloscope setup and proceed to step (21). The trace on terminal 24 obtained should be positive pulses, +3.7 volts in amplitude with an interval between pulses of ≈125 microseconds.

Table 2-4. Control Sequence Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
			(20) If this trace is not obtained, there may be discontinuity between terminal 24 and Card A2A7. In this case, disconnect oscilloscope setup.
			(21) If this trace is obtained, connect the DC VTVM lead to terminal 26. A ground should be obtained. If it is not, there may be discontinuity between terminal 26 and Card A2A4. In this case, disconnect oscilloscope setup.
			(22) If the proper reading is obtained, Logic Element 5 or 3 is bad.
			(23) If the trace at TP2 (step 18) is obtained, Logic Element 14, 13, or 4 bad. In this case, disconnect oscilloscope setup.
			(24) If the proper trace is obtained at terminal 17 (step 15) connect the oscilloscope Channel A INPUT Lead to terminal 58 and the TIME/CM control to 5 msec. Trace obtained should be positive pulses, +3.7 volts in amplitude, occurring every 11 milliseconds (for 45.45 baud operation) or 6.65 milliseconds (for 74.2 or 75 baud operation).
			(25) If this is not obtained, there may be discontinuity between terminal 58 and Card A2A7. In this case, disconnect oscilloscope setup.
			(26) If the proper trace is obtained, Logic Element 6, 20, 19, 18, or 17 is defective.
			(27) If, to this point, all signals are proper, proceed further.
			(28) Connect the oscilloscope Channel A INPUT Lead to terminal 14. Use +INT SYNC.
			(29) Connect the TIME/CM control to 50 msec. The trace obtained from the signal should be a negative pulse, +3.7 volts in amplitude, occurring every 176 milliseconds (for 45.45 baud operation) or 106 milliseconds (for 75 or 74.2 baud operation). This pulse should be time coincident with one of the pulses of the other trace.
			(30) If the correct trace is not received, Logic Element 11 or 12 is defective. In this case, disconnect oscilloscope setup.
			(31) If the correct trace is obtained, proceed further.
			(32) Connect the channel A INPUT lead of the oscilloscope to terminal 50. Place the TIME/CM control to 20 msec. The trace obtained should be similar to that in step (16) except with opposite amplitudes.
			(33) If this trace is not obtained, Logic Element 5 is bad. In this case, disconnect oscilloscope setup.
			(34) If this trace is obtained, proceed further.
			(35) Connect the channel A INPUT Lead of the oscilloscope to terminal 7.
			(36) Connect the oscilloscope EXT INPUT Lead to terminal 22.
			(37) Connect the oscilloscope Channel B INPUT Lead to terminal 14.

Table 2-4. Control Sequence Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
			(38) Adjust the TIME/CM to 0.1 sec. The trace observed (from the first connection made) should be a square wave with limits of ground and +3.7 volts. The duration of the ground should be .35 seconds (for 45.45 baud operation) or .21 seconds (for 75 or 74.2 baud operation). The transition to ground should occur in coincidence with one of the negative pulses viewed on the trace of the second connection made. The traces should reoccur frequently.
			(39) If this is not obtained repeat the previous oscilloscope measurement, except remove the oscilloscope connection from Terminal 7 and connect it to terminal 38.
			(40) The trace at 38 should be similar to that at 7 except inverted. If the trace is correct, Logic Element 1 is defective.
			(41) If the second trace is not obtained, remove the oscilloscope connection from Terminal 38 and connect it to terminal 35. Place the TIME/CM Control to 50 msec. The trace obtained should be a square wave with +3.7 volt and ground limits with a +3.7 volt duration of 176 milliseconds (for 45.45 baud operation) or 106 milliseconds (for 74.2 or 75 baud operation). The transition of +5 volts should occur in time coincidence with a negative pulse observed on the other trace.
			(42) If this trace is not obtained, either Logic Element 21, 9, 8, 16, or one of the Mark Interval Counter Logic Elements (25, 24, or 23) or 4 are bad. This can be further isolated by connecting the oscilloscope Channel A INPUT Lead to TP3. If a similar trace with opposite polarity to step (42) is obtained Logic Element 25, 24, 23 or 4 is defective. If this is not obtained, Logic element 21, 9, 8, or 16 is bad. In this case, disconnect oscilloscope setup.
			(43) If this trace is obtained, disconnect the oscilloscope from terminal 35 and connect it to Terminal 6.
			(44) The trace obtained should be similar to that in step (41).
			(45) If the trace is obtained, Logic Element 10 or 1 is defective.
			(46) If this trace is not obtained, Logic Element 1 is bad. Disconnect oscilloscope setup.
			(47) If the trace required in step (41) is correct, proceed further.
			(48) Connect the oscilloscope Channel A INPUT Lead to TP1.

Table 2-4. Control Sequence Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
			(49) Connect the Channel B INPUT Lead to TP2. The trace obtained from the first pre-amp should be a square wave with ground and +3.7 volt limits. The +3.7 volts should persist for a duration of 176 milliseconds (for 45.45 baud operation) or 106 milliseconds (for 74.2 of 75 baud operation). The trace should reoccur frequently and the transition +3.7 volts should be time coincident with a positive pulse from the other preamp.
			(50) If this trace is not observed, connect the oscilloscope Channel A INPUT Lead to terminal 37. Place the TIME/CM control to 5 msec. The trace observed should be a positive square wave +3.7 volts in amplitude, with a duration of 11 milliseconds (for 45.45 baud operation) or 6.65 milliseconds (for 74.2 or 75 baud operation). These should occur every 165 milliseconds (for 45.45 baud operation) or every 86.35 milliseconds (for 74.2 or 75 baud operation).
			(51) If the proper trace is obtained, Logic Element 22 is defective.
			(52) If the proper trace is not obtained connect the Channel A INPUT Lead of the oscilloscope to terminal 46. The trace obtained should be the same as above except with opposite polarity.
			(53) If this trace is obtained, Logic Element 3 in Card A2A4 is bad or there may be discontinuity between Cards A2A6 and A2A4. If this trace is not obtained Logic Element 11 or 12 is defective.
			(54) If the trace on TP1 (step 48) is correct, connect the oscilloscope Channel A INPUT Lead to terminal 11 and the TIME/CM control to 50 msec. The results should be the same at TP1 (step 45). If this is not obtained, Logic Element 2 or 9 is bad.
			(55) If the proper trace is obtained, proceed to the next step.
			(56) Connect the oscilloscope Channel A INPUT Lead to terminal 42.
			(57) Connect the oscilloscope EXT INPUT Lead to Terminal 33.
			(58) Set the TIME/CM control of the oscilloscope to 1 sec.
			(59) The trace observed should be a positive square wave, +3.7 volts in amplitude, with a width of 175 msec (for 45.44 baud operation) or 105 msec (for 74.2 or 75 baud operation)..
			(60) If this is not obtained, Logic element 2 or 9 is defective.

Table 2-4. Control Sequence Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
17, 18c, 19c, 20, 21f, 24f, 22i, 25a, 23b	MONITOR LAMP does not light (All control sequences).	TRANSMIT BAUD COUNTER Card A2A8.	If none of the control sequences checks out and Card A2A8 is found to be at fault, proceed as follows. (1) Remove Card A2A8 from the logic rack. (2) Connect a card extender to the logic rack to the A2A8 position. (3) Connect Card A2A8 to the card extender. (4) Obtain the oscilloscope. (5) Connect the Channel A INPUT Lead to terminal 33 (CC2P). (6) Connect the Channel B INPUT Lead to terminal 35 (CCLP). (7) Connect the oscilloscope EXT INPUT Lead to terminal 34 (+SYNC). (8) Place the TIME/CM Control to 20 msec position. (9) Place the Simulator Test Panel TRANSMIT and RECEIVE Switches to START position. (10) The trace obtained should be 1 positive pulse (from A) and 2 negative pulses (from B). The should be 106 milliseconds apart (for 74.2 and 75 baud operation) or 176 milliseconds apart (for 45.45 baud operation). Also, these pulses should reoccur every 800 milliseconds. (11) If the positive pulse is obtained or a trace is obtained but the negative pulses are not, element 16 is bad. (12) If the trace is not obtained at all, connect Channel A INPUT Lead of the oscilloscope to terminal 36. Use INT+SYNC. (13) The trace obtained should be a positive pulse, 3.7 volts in amplitude, occurring every 176 milliseconds (for 45.45 baud operation) or every 106 milliseconds (for 74.2 or 75 baud operation). (14) If the trace of step (13) is not obtained, successively check Terminals 51 and TP4 for the same trace. (15) If none of these are obtained, connect the Channel A INPUT Lead to terminal 47 and the Channel B INPUT and + EXT SYNC Lead to terminal 46. Place the TIME/CM Control to 5 msec. The results should be positive pulses at terminal 46 and negative pulses for terminal 47. These should be time coincident, with a time between pulses of 11 milliseconds (for 45.45 baud operation) or 6.67 milliseconds (for 74.2 or 75 baud operation). (16) If either of these is not obtained, there is discontinuity between the respective terminal and Card A2A7. Disconnect oscilloscope setup. (17) If both traces are obtained, Logic Element 8, 13, 18, or 17, 10, 19, 3, 20 is defective. (18) If only TSIX is not obtained Logic Element 10 or 12 is bad; and if only TSIL is not obtained, Logic Element 6 is bad.

Table 2-4. Control Sequence Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
			(19) If the trace of step (12) (TATE) is obtained and also if TSIX and TSIL are obtained, connect the oscilloscope Channel A INPUT Lead to terminal 58 and place the TIME/CM Control to 50 msec. (20) The trace should be the same as that in step (14) TATE. (21) If it is not, Logic Element 20, 25 is defective. In this case, disconnect oscilliscope setup. (22) If it is, connect the oscilloscope Channel A INPUT Lead to terminal 39. The trace obtained should be similar to that in step (13), except it should be a negative pulse. (23) If the correct trace is not observed, Logic Element 16 is defective. In this case, disconnect oscilloscope setup. (24) If the proper trace is observed, connect the oscilloscope Channel A INPUT Lead to Terminal 56 and place the TIME/CM control to 1 sec. (25) The trace obtained should be a positive square wave 3.7 volts in amplitude with a duration of approximately 150 milliseconds. This trace should reoccur frequently. (26) If the proper trace is observed, Logic Element 21 is defective. Disconnect oscilloscope setup. (27) If the proper trace is not observed, Logic Element 23, 22, 25, 24, 14, 9, 15, or the Send Generate Timer is defective, providing a VTVM reading at TP5 does not yield ground for one second intervals. If it does there may be discontinuity between TP5 and Card A2A18. (28) If the proper pulses, CCLP and CC2P (see step 5) are obtained, connect the oscilloscope Channel A INPUT Lead to terminal 11. (29) Connect the EXT INPUT Lead to terminal 36 and connect the channel B INPUT Lead to terminal 47. Place the TIME/CM Control to 20 µsec. (30) The trace observed on A should be 6 positive pulses 3.7 volts in amplitude, with a duration between pulses of 44 milliseconds (for 45.45 baud operation) or 26.6 milliseconds (for 74.2 or 75 baud operation). This group should reoccur frequently and each pulse should be in time coincidence with a pulse of the other trace (input 47). (31) If these are correct, this card (A2A8) should be checked for continuity. Disconnect oscilloscope setup. (32) If the proper trace is not obtained, connect the DC VTVM lead to terminal 19. A +3.7 volt reading should be obtained. If it is not, there is discontinuity between terminal 19 and Card A2A14. Disconnect VTVM Setup. (33) If the correct VTVM reading is obtained, connect the oscilloscope channel A INPUT Lead to terminal 30 and place the TIME/CM control to 50 µsec.

Table 2-4. Control Sequence Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
			(34) The trace obtained should be a pair of square waves, positive, 3.7 volts in amplitude, with a duration between square waves of 44 milliseconds (for 45.45 baud operation) or 26.6 milliseconds (for 74.2 or 75 baud operation). (35) If the proper trace is not obtained, there is is discontinuity between terminal 20 and card A2A18. (36) If the proper trace is obtained, either Logic element 14, 2, 1, 7, 3, 4 or 5 is defective. Disconnect oscilloscope setup. (37) This can be further isolated by an oscilloscope measurement of TP2. If a +3.7 volt measurement is obtained for a period of 133 milliseconds (for 45.45 baud operation) or 78 milliseconds (for 74.2 or 75 baud operation), Logic element 7 is defective. If the reading is not obtained, Logic element 1, 2, 3, 4, 5 or 14 may be defective.
17, 18c, 19c, 20, 21f, 24f, 22i, 25b, 23b	MONITOR Lamp does not light (All Control Sequences).	Logic Card A2A3	Logic Element 1, 2 or 18 may be defective.

Table 2-5. Message Checking Trouble Chart

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
26a	ACK-IT lamp does not light.	PRELIMINARY PROCEDURE ACKNOWLEDGE SEQUENCE, Card A2A11.	(1) Remove Card A2A11 from the Logic Rack. (2) Insert Card Extender into A2A11 position. (3) Connect Card A2A11 to Card Extender. (4) Connect VTVM common lead to terminal 3. (5) Connect VTVM DC lead to terminal 57. A 0.0-volt reading should be obtained. If 0.0v is measured, there is discontinuity between terminal 57 and the Simulator Test Panel. (6) If +11.0v is measured, connect the VTVM DC lead to Terminal 46. A +3.7 volt reading should be obtained. If it is not, there is discontinuity between terminal 46 and Card A2A4. (7) If +3.7 is measured on Terminal 46, there is trouble in the network consisting of R15, C9, and Q6. The trouble can be isolated by checking R15, C9. Disconnect VTVM setup.
26b	ACK-1R lamp does not light.	RECEIVE CONTROL SEQUENCES, Card A2A3.	(1) Remove Card A2A3 from the logic rack. (2) Insert Card Extender into A2A3 position. (3) Connect Card A2A3 to Card Extender. (4) Connect VTVM common lead to terminal 3. (5) Connect VTVM DC lead to terminal 58. A 0.0v reading should be obtained. If 0.0v is measured, there is discontinuity between terminal 58 and the Simulator Test Panel.

Table 2-5. Message Checking Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
			(6) If +11.0v is measured, connect the VTVM DC lead to the junction of Logic Element 9, pin 2 and R5. A +3.7 volt reading should be obtained. If it is not, Logic Element 9, 8, 13, 19 is defective. (7) If it is, the network consisting of R5, C6 and Q2 is malfunctioning. The trouble can be isolated by checking R5, and C6. Disconnect VTVM setup.
26c	AUTO NO. off lamp does not light.	Switch S14, Simulation Test Panel, defective.	Replace Switch S14.
A. SENDING OF TWO CONSECUTIVE MESSAGES			
27a	CANCEL XMITED lamp does not light.	TRANSMIT CANCEL-STOP SEQUENCE logic card A2A9.	(1) Remove Card A2A9 from the logic rack. (2) Connect the Card Extender to the A2A9 slot. (3) Connect Card A2A9 to the Card Extender. (4) Connect the VTVM common lead to terminal 3. (5) Connect the VTVM DC lead to terminal 5. A 0.0 volt reading should be obtained. If 0.0v is measured, there is discontinuity between Terminal 5 and the Control Indicator Panel. (6) If +11.0v is measured, connect the VTVM DC lead to terminal 9. A +3.7 volt reading should be obtained. If it is not, Logic Element 11 is defective. (7) If it is, the network consisting of R3, C5 and Q1 is malfunctioned. This can be isolated by checking R3 and C5. Disconnect VTVM setup.
27b	ACK-2T LAMP does not light.	TRANSMIT START ACKNOWLEDGE SEQUENCE, Card A2A11.	(1) Remove Card A2A11 from the Logic Rack. (2) Insert the Card Extender into A2A11 position. (3) Connect Card A2A11 to Card Extender. (4) Connect VTVM common lead to terminal 3. (5) Connect VTVM DC lead to 36. A 0.0-volt reading should be obtained. If 0.0v is measured, there is discontinuity between terminal 36 and the Simulator Test Panel. (6) If +11.0v is measured, connect the VTVM DC lead to terminal 45. A +3.7 volt reading should be obtained. If it is not, there is discontinuity between terminal 45 and Card A2A4. (7) If it is, there is a malfunction in the network consisting of R12, C8, and Q5. The trouble can be isolated by checking R12, and C8. Disconnect VTVM setup.
27c	ACK-2R lamp does not light.	RECEIVE CONTROL SEQUENCES, Card A2A3.	(1) Remove Card A2A3 from the logic rack. (2) Insert Card Extender into A2A3 position. (3) Connect Card A2A3 to the Card Extender. (4) Connect VTVM common lead to terminal 3. (5) Connect the VTVM DC lead to terminal 52. A 0.0 volt reading should be obtained. If 0.0v is read, there is discontinuity between terminal 52 and the Simulator Test Panel. (6) If +11.0v is measured, connect the VTVM DC lead to the junction of pin 10, Logic Element 9 and R2. A +3.7 volt reading should be obtained. If it is not, Logic Element 9 is defective. (7) If it is +3.7v, the network consisting of R2, C5, and Q1 is malfunctioning. The trouble can be isolated by checking R2, and C5. Disconnect VTVM setup.

Table 2-5. Message Checking Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
27d	TTY input device does not begin to operate.	(1) Card A2A14	(1) Remove Card A2A14 from the logic rack. (2) Insert the Card Extender into the A2A14 slot. (3) Connect Card A2A14 to the Card Extender. (4) Connect the VTVM common lead to Terminal 3. Connect the VTVM DC lead to TP1. A +3.7 volt reading should be obtained. (5) If it is, there may be discontinuity between TP1 and Card A2A7. (6) If it is not, connect the oscilloscope channel A INPUT Lead to terminal 45 and place the TIME/CM Control to 20 μsec. The trace observed should be a positive pulse, 3.7 volts amplitude, occurring every 176 milliseconds (for 45.45 baud operation) or every 106 milliseconds (for 74.2 or 75 baud operation). If these are not observed, there is discontinuity between terminal 45 and Card A2A8. Disconnect oscilloscope setup. (7) If the correct pulse is obtained, connect the VTVM common lead to terminal 3. (8) Successively connect the VTVM DC lead to Terminals 8, 49, 12, 11, 10, 13, and 14 noting a ground reading at each point. If all are not ground, recheck source of the nonground signal. (9) If all are correct either Logic Element 13, 12, 2, 8, or 3 is defective. Disconnect VTVM setup.
27d	TTY input device does not begin to operate.	(2) Card A2A8	(1) Remove Card A2A8 from the logic rack. (2) Insert the Card Extender into the A2A8 slot. (3) Connect Card A2A8 to the Card Extender. (4) Connect the oscilloscope Channel A INPUT Lead to terminal 58 and place the TIME/CM control to 50 μsec. The trace obtained should be positive pulses 3.7 volts amplitude, with 176 milliseconds between each pulse (for 45.45 baud operation) or 106 milliseconds between each pulse (for 74.2 or 75 baud operation). If these are obtained, there is discontinuity between terminal 58 and Card A2A14. In this case, disconnect oscilloscope setup. (5) If these are not obtained, connect the oscilloscope Channel A INPUT Lead to terminal 36, noting the same trace as (4) above. If the trace is correct, Logic Element 20 or 25 is bad. Disconnect oscilloscope setup. (6) If the trace is not correct, perform steps (14) through (18) of Control Sequence trouble charts, Card A2A8 (table 2-4).
27d	TTY input device does not begin to operate.	(3) Card A2A1	(1) Remove Card A2A1 from the logic rack. (2) Insert card extender into A2A1 slot. (3) Connect Card A2A1 to the card extender. (4) Connect the VTVM common lead to terminal 30. (5) Connect the VTVM DC lead to the C4 positive terminal, noting a reading of 12 vdc. If this is not present, the network consisting of L1, L2, C1, C2, C3 and C4 may be defective. (6) If the voltage is present, connect the VTVM COMMON lead to the C8 minus terminal. (7) Connect the VTVM DC lead to terminal 30, noting a reading of 12 vdc. If this is not present, the network consisting of L3, L4, C5, C6, C7, and C8 may be defective.

Table 2-5. Message Checking Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
			(8) If the voltage is present, the network between terminals 44 and 9 is defective. Use standard procedures to isolate defect.
27c	XMIT IN PROCESS lamp does not light.	(1) Card A2A11	(1) Disconnect Card A2A11 from the logic rack. (2) Connect the Card Extender to the A2A11 slot. (3) Connect Card A2A11 to the Card Extender. (4) Connect the VTVM common lead to terminal 4. (5) Connect the VTVM DC lead to terminal 35. +0.0v should be observed. If 0.0v is measured there is discontinuity between terminal 35 and the Control Indicator Panel. (6) If +11.0v is measured, connect the VTVM DC lead to the junction of pin 2, element 10 and R1. A +3.7 volt reading should be obtained. If it is, the network consisting of R1, C6, and Q1 is malfunctioning. This can be isolated further by checking R1, C6. (7) If it is not, either Logic Element 10 is bad, or the precedence character is not entering this card due to discontinuity between Terminal 24 and Card A2A18. The determination of a defective logic element 10 is also contingent on the fact that VTVM readings at terminals 16 and 52 are ground. Disconnect VTVM setup.
27c	XMIT IN PROCESS lamp does not light.	(2) Card A2A18	(1) Remove Card A2A18 from the logic rack. (2) Insert the Card Extender into the A2A18 slot. (3) Connect Card A2A18 to the Card Extender. (4) Connect the VTVM common lead to Terminal 3. (5) Connect the VTVM DC lead to terminal TP1. A +3.7 volt reading should be obtained. If it is, there is discontinuity between TP2 and Card A2A11. (6) If it is not, either Logic Element 1, 21, or the element associated with the precedence character being used (22, 23, 24, 20, 19, 18, or 17) is defective. Disconnect VTVM setup.
27f	REC IN PROCESS does not light.	(1) Card A2A5	(1) Disconnect Card A2A5 from the logic rack. (2) Insert the Card Extender into the A2A5 slot. (3) Connect Card A2A5 to the Card Extender. (4) Connect the VTVM common lead to Terminal 3. (5) Connect the VTVM DC lead to Terminal 33. A 0.0v reading should be obtained. If 0.0v is measured, there is discontinuity between terminal 33 and the Control Indicator Panel. (6) If +11.0 volts is measured, connect the VTVM DC lead to Terminal 15. A +3.7 volt reading should be obtained. If it is, the network consisting of R2, C5, and Q1 is malfunctioning. The trouble can be isolated by checking R2 and C5. (7) If it is not, connect the VTVM DC lead to Terminal 20. A ground should be obtained. If it is, Logic Element 14 or 22 is defective or there is discontinuity between Terminal 22 or 16 and Card A2A6. (8) If it is not, Logic Element 12, 7 or 1 is defective, or there is discontinuity between terminal 37 and Card A2A3.
		(2) Card A2A6	(1) Remove Card A2A6 from the logic rack. (2) Insert the Card Extender into the logic rack slot. (3) Connect Card A2A6 to the Card Extender. (4) Perform steps (28) through (30) of Control Sequence Trouble Charts Card A2A6, then proceed to step (5).

Table 2-5. Message Checking Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
			(5) Perform steps (31) through (33) of Control Sequence Trouble Charts Card A2A6. If trouble is not uncovered there is continuity trouble. Disconnect VTVM setup.
27g	ACK-1T lamp does not light.	Card A2A11	Perform steps (1) through (7) of item 26a.
27h	ACK-1R lamp does not light.	Card A2A3	Perform steps (1) through (7) of item 26b.
27i	MESSAGE NUMBER digital readout is not correct.	(1) Card A2A16	(1) Remove Card A2A16 from the logic rack. Insert the Card Extender into the A2A16 slot. Connect Card A2A16 to the Card Extender. (2) Connect the VTVM COMMON lead to terminal 3. (3) Successively connect the VTVM DC lead to the following terminals and observe the following readings: (*a*) 41—ground. (*b*) 38—+3.7 volts. (*c*) 39—+3.7 volts. (*d*) 37—ground. (*e*) 10—ground. (*f*) 20—ground. (*g*) 51—ground. (*h*) 52—+3.7 volts. (*i*) 23—+3.7 volts. (*j*) 49—ground. (*k*) 18—+3.7 volts. (*l*) 57—ground. If these readings are obtained, there is discontinuity between one or more of the terminals and the Control Indicator Panel. (4) If one or more incorrect readings are obtained, the associated Logic Element is defective. This may be Logic Element 2, 6, 11, 16, 21, 22, 4, 5, 9, 10, 15, 20, or 3. Logic Element 13 or 25 may also be defective. (5) If the count is one less than it should be, the Card A2A16 did not receive the EMVP pulse. In this case there may be discontinuity between Terminal 40 and Card A2A5. (6) If the number is wrong and the VTVM measurements described in step (c) are correct, it is possible that this card is not receiving the DEMN 9, 10 and/or 11 pulses. If the 5 is not displayed on the panel, the DEMN 9 was not received, indicating that there may be discontinuity between terminal 19 and Card A2A15. Another possibility in this case is that Logic Element 14 or 24 is defective. (7) If the 8 is not displayed on the panel, the DEMN-10 may not have been received, indicating that there may be discontinuity between Terminal 13 and Card A2A15. Another possibility is that Logic Element 18 or 17 is defective. (8) If the 7 is not displayed, the DEMN 11 may not have been received, indicating that there may be discontinuity between Terminal 12 and Card A2A15. Another possibility in this case is that Logic Element 12 or 7 is defective. (9) If nothing is displayed on the panel, it is possible that Logic Element 19 or 8 is defective. Disconnect VTVM setup.

Table 2-5. Message Checking Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
			(10) If the message number originally displayed at the time testing was begun is still displayed and fails to clear, Logic Element 1 or 23 may be defective.
	Message Number Digital Readout is not 587.	(2) Card A2A15	If 587 is not displayed, it is the result of the preset logic on this Logic Card. This could be one of Logic Elements 1, 2, 3, 6, 7, or 8.
		(3) Card A2A5	Logic Element 25 may be defective.
		(4) Card A2A11	Logic Element 8 may be defective.
		(5) Card A2A17	Logic Element 1, 2, 3, 4, 6, 8, 11, 7, 12, 17, 16, 21, 22, 18, or 23 may be defective.
		(6) Control Indicator Panel, A1.	An incorrect display indicates that there is either trouble in the Message Numbering Switches (UNITS, TENS or HUNDREDS) or that the Nixie display tubes or decoders are defective.
27j	ACK-2T lamp does not light.	Card A2A11	Perform steps (1) through (7), of item 27b.
27k	ACK-2R lamp does not light.	Card A2A3	Perform steps (1) through (7), of item 27c.
27l	The message printout is not correct.	Any card	See para 2-8 Message Printout, Trouble Analysis at the end of this Table.
B. USE OF STOP-AT-EOM TRANSMIT CAPABILITY			
28a	STOP AT EOM lamp does not light.	Card A2A14	(1) Remove Card A2A14 from the logic rack. Insert the Card Extender into the A2A14 slot. Connect Card A2A14 to the Card Extender. (2) Connect the VTVM COMMON lead to Terminal 3. (3) Connect the VTVM DC lead to Terminal 54. A +0.0v dc reading should be obtained. If 0.0v is measured, there is discontinuity between Terminal 54 and the Control Indicator Panel. (4) If +11.0v is measured, connect the VTVM DC terminal to the junction of pin 2, Logic Element 16 and R2. A +3.7 volt reading should be obtained. If it is, the network consisting of R2, C5, and Q1 is defective. The trouble can be isolated by checking R2, and C5. (5) If it is not, Logic Element 16 is defective or there is discontinuity between terminal 33 and the Control Indicator Panel. Disconnect VTVM setup.
28b	ALARM lamp does not light.	(1) Card A2A19	(1) Remove Card A2A19 from the logic rack. Insert the Card Extender into the A2A19 slot. Connect Card A2A19 to the Card Extender. (2) Connect the VTVM COMMON lead to Terminal 3. (3) Connect the VTVM DC lead to Terminal 7. A 0.0 reading should be obtained. If 0.0v is measured, there is discontinuity between Terminal 7 and the Control Indicator Panel. (4) If +11v is measured, connect the DC VTVM lead to the junction of pin 10 of Logic Element 23 and R3. A +3.7 volt reading should be obtained. If it is, the network consisting of R3, C5 and Q1 is defective. The trouble can be isolated by checking R3, and C5.

Table 2-5. Message Checking Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
			(5) If the +3.7 volts is not obtained, connect the VTVM DC lead to the junction of Pin 4, Logic Element 25 and R5. A +3.7 volt reading should be obtained. If it is, Logic Element 23 or 25 is bad. (6) If it is not, there is discontinuity between Terminal 25 and Card A2A14. Disconnect VTVM setup.
	ALARM lamp does not light.	(2) Card A2A14	(1) Remove Card A2A14 from the logic rack. Insert the Card Extender into the A2A14 slot. Connect Card A2A14 to the Card Extender. (2) Connect the COMMON VTVM lead to terminal 3. (3) Connect the DC VTVM lead to terminal 6. A +3.7 volt reading should be obtained. If it is, there is discontinuity between Terminal 6 and Card A2A19. (4) If it is not, connect the VTVM DC lead to the junction of Logic Element 17, pin 4 and R2. A reading of +3.7 volts should be obtained. If it is not, either Logic Element 16 is defective or there is discontinuity between terminal 33 and the Control Indicator Panel. (5) If the +3.7 volts is obtained, check the Simulator Test Panel to see that the ACK-1R lamp is illuminated. If it is, either Logic Element 17 is defective or there is discontinuity between Terminal 26 and Card A2A11. Disconnect VTVM setup.
	ALARM LAMP does not light.	(3) Card A2A5	Logic Element 23 or 18 may be defective.
28c	AUDIBLE ALARM does not sound.	(1) ALARM itself	Check the alarm by operating the Control Indicator Panel Test Switch. If the alarm does not sound, the Alarm itself is defective and has to be replaced.
		(2) CARD A2A14	(1) If the alarm does sound, remove Card A2A14 from the logic rack. Insert the Card Extender into the A2A14 slot. Connect Card A2A14 to the Card Extender. (2) Obtain the oscilloscope. (3) Connect the oscilloscope channel A INPUT lead to terminal 51 and place the TIME/CM Control to .5 sec. A symmetrical square wave should be obtained with limits of −12 and +12 volts with a duration and frequency of ½ second. If no negative voltage is present, there is discontinuity between Terminal 51 and the Control Indicator Panel. In this case, disconnect oscilloscope setup. (4) If −12 is present, connect the oscilloscope Channel A INPUT Lead to the junction of R6 and R7. The same results as with (3) above should be obtained except for +12 and ground voltage level. If it is, R6, R7, or Q3 is defective. This can be isolated by checking R6 and R7. In this case, disconnect oscilloscope setup. (5) If the ground is not obtained, connect the oscilloscope Channel A INPUT Lead to the junction of Logic Element 18, pin 2 and R4. A +3.7v to ground square wave should be obtained. If it is, R4, R5, CR1, or Q2 is defective. This can be isolated by checking R4, R5, CR1 and Q2. Disconnect oscilloscope setup. (6) If the square wave is not obtained, connect the VTVM COMMON lead to terminal 27. (7) Connect the VTVM DC lead to terminal 50. A ground should be obtained. If it is not there is discontinuity between terminal 50 and CARD A2A19.

Table 2-6. Message Checking Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
			(8) If ground is measured on term 50, connect the oscilloscope channel A INPUT lead to Terminal 56. Similar results to step (5) should be obtained. If the correct trace is observed Logic Element 18 is defective. Disconnect oscilloscope setup. (9) If the correct trace is not observed, refer to Trouble Chart, Control sequences items 17, 18c, 19c, 20, 21f, 24f, 22i, 25b, 23b. Card A2A14. Disconnect VTVM setup.
		(3) Card A2A19	(1) Remove Card A2A19 from the logic rack. Insert the Card Extender into the A2A19 slot. Connect Card A2A19 to the Card Extender. (2) Connect the VTVM COMMON lead to terminal 27. (3) Connect the VTVM DC lead to terminal 11. A ground should be obtained. If it is, there is discontinuity between Terminal 11 and Card A2A14. (4) If it is not, connect the VTVM DC lead to Terminal 25. A +3.7 volt reading should be obtained. If it is, either R5, C8, C9, CR2, or Logic Element 23 or 25 is defective. (5) If the correct reading is obtained, there is discontinuity between Terminal 25 and Card A2A14. Disconnect VTVM setup.
28d	TTY input device does not begin to operate.	(1) Card A2A14	Perform steps (1) through (9) of item 27d(1).
		(2) Card A2A8	Perform steps (1) through (6) of item 27d(2).
		(3) Card A2A1	Perform steps (1) through (8) of item 27d(3).
28e	XMIT IN PROCESS lamp does not light.	(1) Card A2A11	Perform steps (1) through (7) of item 27e(1).
		(2) Card A2A18	Perform steps (1) through (6) of item 27e(2).
28f	RECEIVE IN PROCESS lamp does not light.	(1) Card A2A5	Perform steps (1) through (8) item 27f(1). Perform steps (1) through (5) of item 27f(2).
28g	ACK-1T Lamp does not light.	Card A2A11	Perform steps (1) through (7) of item 26a.
28h	ACK-1R Lamp does not light.	Card A2A3	Perform steps (1) through (7) of item 26b.
28i	MESSAGE NUMBER does not advance to 588.	(1) Card A2A16	Perform steps (1) through (10) item 27i(1). *Note.* Keep in mind that the number in this case is 589 (not 580).
		(2) Card A2A15	Perform step 27i(2).
		(3) Card A2A5	Perform step 27i(3).
		(4) Card A2A11	Perform step 27i(4).
		(5) Card A2A17	Perform step 27i(5).
		(6) Control Indicator Panel	Perform step 27i(6).
28j	The printout is not correct.	Any Card	See para 2-8 Message Printout, Trouble Analysis at the end of this table.
28k	ITTY Input device does not begin to operate.	Card A2A14	Perform steps (1) through (9) of item 27d(1).
		Card A2A8	Perform steps (1) through (6) of item 27d(2).
28l	XMIT IN PROCESS lamp does not light.	(1) Card A2A11	Performs steps (1) through (7) of item 27e(1).
		(2) Card A2A18	Performs steps (1) through (6) of item 27e(2).
		(3) Card A2A15	Perform step 27i(2).
		(4) Card A2A5	Perform step 27i(3).
		(5) Card A2A11	Perform step 27i(4).
		(6) Card A2A17	Perform step 27i(5).
		(7) Control Indicator Panel.	Perform step 27i(6).

Table 2-5. Message Checking Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
28m	RECEIVE IN PROCESS lamp does not light.	Card A2A5 Card A2A6	Perform steps (1) through (8) item 27f(1). Perform steps (1) through (5) item 27f(2).
28n	ACK-2T lamp does not light.	Card A2A11	Perform steps (1) through (7) of item 27b.
28o	ACK-2R lamp does not light.	Card A2A3	Perform steps (1) through (7) of item 27c.
28p	Message Number does not read 589.	(1) Card A2A16	Perform steps (1) through (10) item 27i(1). *Note.* Message Number in this case should be 589.
28q	Message Printout is not correct.	Any Card	See para 2-8 Message Printout, Trouble Analysis at the end of this table.
C. USE OF STOP AT EOM RECEIVE CAPABILITY			
29a	CANCEL XMITED lamp does not light.	Card A2A9	Perform steps (1) through (7) of item 27a.
29b	ACK-2T lamp does not light.	Card A2A11	Perform steps (1) through (9) of item 27b.
29c	ACK-2R lamp does not light.	Card A2A3	Perform steps (1) through (7) of item 27d.
29d	TTY input device does not begin to operate.	(1) Card A2A14 (2) Card A2A8 (3) Card A2A1	Perform steps (1) through (9) item 27d(1). Perform steps (1) through (6) item 27d(2). Perform steps (1) through (7) of item 27d(3).
29e	XMIT IN PROCESS lamp does not light.	(1) Card A2A11 (2) Card A2A18	Perform steps (1) through (7) of item 27e(1). Perform steps (1) through (6) of item 27e(2).
29f	REC IN PROCESS lamp does not light.	(1) Card A2A5 (2) Card A2A6	Perform steps (1) through (8) of item 27f(1). Perform steps (1) through (5) of item 27f(2).
29g	RECEIVE STOP AT EOM lamp does not light.	Control Indicator Panel.	Check Switch S1, replace it if it is faulty. If it is not, there is a continuity problem.
29h	ALARM Lamp does not light.	(1) Card A2A19 (2) Card A2A14 (3) Card A2A5	Perform steps (1) through (6) of item 28b(1). Perform steps (1) through (5) of item 28b(2). Logic element 23 or 18 may be bad.
29i	AUDIBLE ALARM does not sound.	(1) ALARM itself (2) Card A2A14 (3) Card A2A19	Perform step of item 28c(1). Perform steps (1) through (9) of item 28c(2). Perform steps (1) through (5) item 28c(3), except in this case, the affected network consists of R4, C7, C6, CR1.
29j	ACK-1T Lamp does not light.	Card A2A11	Perform steps (1) through (7) of item 26a.
29k	ACK-1R Lamp does not light.	Card A2A3	Perform steps (1) through (7) of item 26b.
29l	MESSAGE NUMBER readout is not 590.	(1) Card A2A16 (2) Card A2A15 (3) Card A2A5 (4) Card A2A11 (5) Card A2A17 (6) Control Indicator Panel.	Perform steps (1) through (10) item 27i(1). *Note.* Keep in mind that the number in this case is 590 (not 586). Perform step 27i(2). Perform step 27i(3). Perform step 27i(4). Perform step 27i(5). Perform step 27i(6)
29m	The printout is not correct.	Any Card	See para 2-8 Message Printout, Trouble Analysis at the end of this table.
29n	TTY input device does not start to operate.	(1) Card A2A14 (2) Card A2A8	Perform steps (1) through (9) of item 27d(1). Perform steps (1) through (5) of item 27d(2).

Table 2-5. Message Checking Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
29o	XMIT IN PROCESS lamp does not light.	(1) Card A2A11 (2) Card A2A18	Perform steps (1) through (7) of item 27e(1). Perform steps (1) through (5) of item 27e(2).
29p	REC IN PROCESS lamp does not light.	(1) Card A2A5 (2) Card A2A6	Perform steps (1) through (7) of item 27f(1). Perform steps (1) through (5) of item 27f(2).
29q	ACK-2T lamp does not light.	Card A2A11	Perform steps (1) through (7) of item 27b.
29r	ACK-2R Lamp does not light.	Card A2A3	Perform steps (1) through (7) of item 27c.
29s	MESSAGE NUMBER readout is not 591.	(1) Card A2A16	Perform steps (1) through (10) of item 27i(1). *Note.* Keep in mind that the number in this case is 591 (not 586).
		(2) Card A2A15 (3) Card A2A5 (4) Card A2A11 (5) Card A2A17 (6) Control Indicator Panel.	Perform item 27i(2). Perform item 27i(3). Perform item 27i(4). Perform item 27i(5). Perform item 27i(6).
29t	The printout is not correct.	Any Card	See para 2-8, Message Printout, Trouble Analysis at the end of this table.
D. TESTING MESSAGE WITH ABNORMAL INPUT DEVICE			
30a	CANCEL XMITED Lamp does not light.	Card A2A9	Perform steps (1) through (7) of item 27a.
30b	ACK-2T lamp does not light.	Card A2A11	Perform steps (1) through (7) of item 27b.
30c	ACK-2R lamp does not light.	Card A2A3	Perform steps (1) through (7) of item 27c.
30d	ABNORMAL INPUT lamp does not light.	Card A2A11	(1) Remove Card A2A11 from the logic rack. Connect the Card Extender to the A2A11 slot. Connect Card A2A11 to the Card Extender. (2) Connect the VTVM COMMON lead to terminal 4. Connect the VTVM DC lead to terminal 33. A 0.0v reading should be obtained. If 0.0v is measured there is discontinuity between Terminal 33 and the Control Indicator Panel. (3) If +11.0v reading is obtained, connect the VTVM DC lead to terminal 21. A +3.7 volt reading should be obtained. If it is, the network consisting of R4, C7, and Q2 is bad. The trouble can be isolated by checking R4 and C7. (4) If the +3.7 volt reading is not obtained, connect the VTVM DC lead to Terminal 58. A +6.0 volt reading should be obtained. If it is, the network consisting of R7, R8, R9, R11, CR1, CR2, Q3 and Q4 is bad. This can be isolated to one of the resistors, diodes or the transistors by checking the diodes and resistors. (5) If the +6.0 volts is not obtained, there is discontinuity between Terminal 58 and the Control Indicator Panel. Disconnect VTVM setup.
30e	ALARM Lamp does not light.	(1) Card A2A19	Perform steps (1) through (6) of item 28b(1), except, in this case, the affected network consists of C17, C16, R9, CR6, and Logic Element 24.
		(2) Card A2A14	Perform steps (1) through (5) of item 28b(2).

Table 2-5. Message Checking Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
30f	AUDIBLE ALARM does not sound.	(1) ALARM itself	*Note.* Also, for this section, Logic Element 4 of Card A2A14 may be bad. Perform step 28c(1).
		(2) Card A2A14	Perform steps (1) through (9) of item 28c(2).
		(3) Card A2A11	Perform steps (1) through (5) of item 28c(3).
30g	XMIT IN PROCESS lamp does not light.	(1) Card A2A11	Perform steps (1) through (7) of item 27e(1).
		(2) Card A2A18	Perform steps (1) through (6) of item 27e(2).
30h	REC IN PROCESS lamp does not light.	(1) Card A2A5	Perform steps (1) through (8) of item 27f(1).
		(2) Card A2A6	Perform steps (1) through (5) of item 27f(2).
30i	ACK-1T Lamp does not light.	Card A2A11	Perform steps (1) through (7) of item 26a.
30j	ACK-1R Lamp does not light.	Card A2A3	Perform steps (1) through (7) of item 26b.
30k	MESSAGE NUMBER readout is not 593.	(1) Card A2A16	Perform steps (1) through (10) of item 27i(1). *Note.* Keep in mind that the number in this case is 593 (not 586).
		(2) Card A2A15	Perform item 27i(2).
		(3) Card A2A5	Perform item 27i(3).
		(4) Card A2A11	Perform item 27i(4).
		(5) Card A2A17	Perform item 27i(5).
		(6) Control Indicator Panel.	Perform item 27i(6).
30l	ACK-2T lamp does not light.	Card A2A11	Perform steps (1) through (7) of item 27b.
30m	ACK-2R lamp does not light.	Card A2A3	Perform steps (1) through (7) of item 27c.
30n	Printout is not correct.	Any Card	See para 2-8, Message Printout, Trouble Analysis, at the end of this table.
E. TESTING MESSAGES WITH ABNORMAL OUTPUT DEVICE			
31a	CANCEL XMITED lamp does not light.	Card A2A9	Perform steps (1) through (7) of item 27a.
31b	ACK-2T lamp does not light.	Card A2A11	Perform steps (1) through (7) of item 27b.
31c	ACK-2R lamp does not light.	Card A2A3	Perform steps (1) through (7) of item 27c.
31d	ABNORMAL OUTPUT lamp does not light.	Card A2A4	(1) Remove Card A2A4 from the logic rack. Insert the Card Extender into the A2A4 slot. Connect Card A2A4 to the Card Extender. (2) Connect the VTVM COMMON lead to terminal 3. (3) Connect the VTVM DC lead to terminal 26. A 0.0v reading should be observed. If 0.0v is measured, there is discontinuity between Terminal 26 and the Control Indicator Panel. (4) If +11.0v is measured, connect the VTVM DC lead to the junction of Q2 and R2. A +3.7 volt reading should be obtained. If it is, the network consisting of R2, C5, and Q1 is defective. This can be isolated by checking R2 and C5. (5) If the +3.7 volts is not obtained, connect the VTVM DC lead to terminal 58. A +6 volt reading should be obtained. If it is, the network consisting of R7, R6, R5, R4, CR1, CR3, Q3 and Q2 is defective. The trouble can be isolated by checking the resistors and diodes.

Table 2-5. Message Checking Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
			(6) If the +6 volts is not obtained, there is discontinuity between terminal 58 and the Control Indicator Panel. Disconnect VTVM setup.
31e	ALARM Lamp does not light.	(1) Card A2A19	Perform steps (1) through (6) of item 28b(1).
		(2) Card A2A14	Perform steps (1) through (6) of item 28b(2). *Note.* Also, for this section, Logic Element 4 of Card A2A14 may be bad.
31f	AUDIBLE ALARM does not sound.	(1) ALARM itself	Perform the step of item 28c(1).
		(2) Card A2A14	Perform steps (1) through (9) of item 28c(2).
		(3) Card A2A19	Perform steps (1) through (5) of item 28c(3) except, in this case, the affected network consists of C17, C16, CR6, R9, and Logic Element 24.
31g	STOP lamp does not light.	(1) Card A2A10	(1) Remove Card A2A10 from the logic rack. Insert the Card Extender into the A2A10 slot. Connect Card A2A10 to the Card Extender. (2) Connect the oscilloscope Channel A INPUT Lead to Terminal 55 and place the TIME/CM control to .5 sec. (3) The trace obtained should be a symmetrical square wave with limits of ground and 11 volts and a duration of ¼ second. (4) If 0.0v is obtained, there is discontinuity between Terminal 55 and the Control Indicator Panel. In this case disconnect oscilloscope setup. (5) If +11v is measured, connect the oscilloscope Channel A INPUT lead to the junction of Logic Element 7, pin 10 and R7. A square wave should be obtained as in step (3), except that the limits are ground and +3.7 volts. (6) If the correct trace is obtained, the network consisting of R7, C7, and Q2 is defective. The trouble can be isolated by checking R7 and C7. In this case, disconnect oscilloscope setup. (7) If the correct trace is not obtained connect the oscilloscope Channel A INPUT Lead to terminal 45. The results obtained should be the same as step (5). If it is not, there is discontinuity between terminal 45 and card A2A14. In this case, disconnect oscilloscope setup. (8) If the correct trace is obtained connect the VTVM DC lead to terminal 47. A +3.7 volt reading should be obtained. If it is, Logic Element 7 is defective. Disconnect oscilloscope setup. *Note.* Logic Element 11 may also be defective in this case, but it would not cause the TRANSMIT STOP Lamp not to light.
		(2) Card A2A14	(*a*) Remove Card A2A14 from the logic rack. Insert the Card Extender into the A2A14 logic rack slot. Connect Card A2A14 to the card extender. (*b*) Perform steps (8) and (9), item 28c(2).
31h	XMIT N PROCESS Lamp does not light.	(1) Card A2A11	Perform steps (1) through (7) of item 27e(1).
		(2) Card A2A18	Perform steps (1) through (6) item 27e(2).
31i	REC IN PROCESS lamp does not light.	(1) Card A2A5	Perform steps (1) through (8) of item 27f(1).
		(2) Card A2A6	Perform steps (1) through (5) item 27f(2).
31j	ACK-1T lamp does not light.	Card A2A11	Perform steps (1) through (7) of item 26a.

Table 2-5. Message Checking Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
31k	ACK-1R lamp does not light.	Card A2A3	Perform steps (1) through (7) of item 26b.
31l	MESSAGE NUMBER readout is not 595.	(1) Card A2A16	Perform steps (1) through (8), item 27i(1). *Note.* Keep in mind that the number in this case is 595 (not 586).
		(2) Card A2A15	Perform item 27i(2).
		(3) Card A2A5	Perform item 27i(3).
		(4) Card A2A11	Perform item 27i(4).
		(5) Card A2A17	Perform item 27i(5).
		(6) Control Indicator Panel.	Perform item 27i(6).
31m	ACK-2T lamp does not light.	Card A2A11	Perform steps (1) through (7) of item 27b.
31n	ACK-2R lamp does not light.	Card A2A3	Perform steps (1) through (7) of item 27c.
31o	The message printout is not correct.	Any Card	See para 2-8 Message Printout, Trouble Analysis, at the end of this table.
F. MANUAL CANCELING AND RETRANSMITTING OF MESSAGE IN PROCESS			
32a	CANCEL XMITED lamp does not light.	Card A2A9	Perform steps (1) through (7) of item 27a.
32b	ACK-2T Lamp does not light.	Card A2A11	Perform steps (1) through (7) of item 27b.
32c	ACK-2R Lamp does not light.	Card A2A3	Perform steps (1) through (7) of item 27c.
32d	CANCEL XMITED Lamp does not light.	Card A2A9	Perform steps (1) through (7) of item 27a.
32e	Message Processing does not resume.	Card A2A11	Perform steps (1) through (5) of item 30d, except note opposite results in each case. Also, ascertain that Terminal 21 reads ground.
32f	ACK-1T Lamp does not light.	Card A2A11	Perform steps (1) through (7) of item 26a.
32g	ACK-1R Lamp does not light.	Card A2A3	Perform steps (1) through (7) of item 26b.
32h	STOP Lamp does not flash.	(1) Card A2A10 (2) Card A2A14	Perform steps (1) through (8) of item 31g(1). Perform steps (1) and (2) of item 31g(2).
32i	CANCEL XMITED Lamp does not light.	Card A2A9	Perform steps (1) through (7) of item 27a.
32j	ACK-2T Lamp does not light.	Card A2A11	Perform steps (1) through (7) of item 27b.
32k	ACK-2R Lamp does not light.	Card A2A3	Perform steps (1) through (7) of item 27c.
32l	The Printout is incorrect.	Any Card	See para 2-8, Message Printout, Trouble Analysis, at the end of this table.

2-8. Message Printout, Troubleshooting

a. General. If, during message checking, the message printout on the TTY output device is found to be incorrect, the trouble analysis procedure should be undertaken by noting two factors: the logic card found (by replacement at Echelon 2) to be defective; and the section of the message which did not print out properly. The message printout may be considered to consist of four (4) separate sections which are—

(1) Message Header—VZCZC XXX* 999**

*Channel Designator
**Message Number

(2) Precedence Character
(3) Message Intelligence (text)
(4) End-of-Message—NNNN

b. If the message header only does not printout properly, failure of one of the following logic cards (as shown at organizational maintenance) will yield the following possibilities as to the malfunctioning logic:

(1) *Logic Card A2A15.*

(*a*) The type of erroneous printout will provide a clue to the trouble. For instance, if one or two letters are erroneous but generally the message header is correct and in order. the trouble is in that portion of the logic associated with the erroneous letters. The trouble could also be in the 4-stage counter which produces pulses for the generation of each of the message header characters. This counter consists of Logic Elements 16, 21, 22, 23 and an input gate Logic Element 11. These counter pulses and the associated header characters which they generate are as follows. (Also shown are the suspected Logic Elements for each LOND pulse):

Pulse	*Printout*	*Logic Element*
1. LOND-0	V	11
2. LOND-1	Z	10
3. LOND-2	C	19
4. LOND-1	Z	10
5. LOND-4	C	19
6. LOND-5	X Channel Designator	10
7. LOND-6	X	9
8. LOND-7	X	9
9. LOND-8	Switch to Figures (Not Printed)	14
10. DEMN-9	1 Message Number	20
11. DEMN 10	1	15
12. DEMN-11	1	15
13. LOND-12	Switch to Letters (Not Printed)	4
14. LOND-13	Carriage Return Not Printed*	4
15. LOND-14	Carriage Return	5
16. LOND-15	Line Feed	5

*Used only with JANAP-128; if ACP 127 is used, counuer advances directly from LOND-12 to LOND-0

(*b*) Therefore, if a letter is missing, the counter may not be producing the correct count. The particular missing character will indicate the erroneous count. The erroneous count (LOND) may also occur as a result of one of the decoding Logic elements having malfunctioned.

(*c*) In addition if the message header is not printed out at all, Logic element 17 may be bad. If the first four characters (VZCZ) are missing, logic element 25 may be bad. If the second four characters (CXXX) are missing, logic element 24 may be defective. If the message number is printed as letters, logic element 13 may be bad. If the message number is not printed out, logic element 13 may be bad. If, for JANAP 128 operation, the line feeds and carriage return are not accomplished, logic element 24 may be bad. If none of the message header is printed out, logic element 18, 17, 11, or 12 may be bad.

(*d*) If the message number is not printed out logic element 20 or 25 may be bad.

(2) *Logic Card A2A16.* If the message number is not correct, refer to the isolation procedure presented for steps (1) through (9), card A2A16, item 5(b) in the trouble shooting tables.

(3) *Logic Card A2A17.*

(*a*) If the message header does not printout properly, the problem is the decoding logic on this logic card. Thus one of logic elements 10, 15, 19, 9. 14, 24, 20, or 8 can be defective. Also logic element 4 can be bad.

(*b*) If specifically the message number does not print out properly, one of logic elements 1, 2, 3, 4, 6, 8, 11. 7, 12, 17, 16, 21, 22, or 18 is bad.

(4) Logic card A2A5; logic element 4 may be defective.

(5) Logic card A2A3; logic element 25 may be defective.

(6) Logic card A2A6; logic element 15 may be defective.

c. If the precedence character only does not print properly, the failure of one of the following cards will provide a clue to the particular trouble.

- (1) Card A2A19—Logic Element 1, 6, 11, 16, 21, 2, 7, 12, 17, or 22 may be defective. This can be checked by ascertaining that, during the course of message transmission, an oscilloscope measurement first at TP1, then at TP2, yields positive (3.7 volt) pulses. If the former is not present, then discontinuity may exist and Logic elements 1, 6, 11, 16, and 21 are probably good. If the latter is not present, discontinuity may exist in which case Logic elements 2, 7, 12, 17 and 22 are probably good.
- (2) Card A2A14—Logic element 2 may be defective.
- (3) Card A2A11—Logic element 18 may be defective.
- (4) Card A2A9—Logic element 18, 17, or 4, may be defective.

d. If the message text only prints out incorrectly, the trouble is likely one of the TTY devices. In this case the INPUT or OUTPUT ABNORMAL Lamp on the Control and Indicator Panel is not illuminated since these lamps indicate only a tight tape or out of paper or tape condition.

e. If the end-of-message does not print out correctly, the particular trouble depends upon the defective card.

- (1) Card A2A2—Logic element 7 or 9 may be defective.
- (2) Card A2A4—Logic element 8, 13, 14, 6, or the N Counter (logic element 19, 20, or 18) may be defective.
- (3) Card A2A14—Logic element 11, 12, 7, 8, 19, 6, 10 or the N Counter (logic element 9, 14, or 15) may be defective.
- (4) Card A2A11—Logic element 6 may be defective.
- (5) Card A2A18—Logic element 16 may be defective.
- (6) Card A2A5—Logic element 13, 17, 18 or 10 may be defective. This can be checked by an oscilloscope measurement at TP1 during the course of message reception. If a +3.7 volt pulse is obtained, the logic elements are probably good.
- (7) Card A2A3—Logic element 25 may be defective.

f. If none of the message prints out correctly, the particular trouble depends on the following defective cards.

- (1) Card A2A4—It is possible that the enable signal for the receive start pulse is not being generated or that the termination signal for the control sequences has not been generated. In this case, Logic element 7, 9, 16, or 11 may be defective. It is also possible that the Transmit Buffer is not being cleared when required, in which case logic element 5 may be defective. Another possibility of trouble, if the stop or retransmit capability is being used either during testing or operation (as a receiver), is a defective Logic element 1, 2, 3, 4, 5, 6, 7, or 10.
- (2) Card A2A3—It is possible that due to malfunctioning logic, the incorrect printout is due to unintelligible characters. In this case Logic Element 20, 3, 15, 21, or 25 may be defective. Another possibility which may occur during a retransmission or stop condition is that Logic Element 1, 15, or 21 may be defective.
- (3) Card A2A8
  - (*a*) If the TCU is operating in CRYPTO position, Logic Element 20, 19, or 10 may be bad.
  - (*b*) If the TCU is operating in either mode (TCU or CRYPTO), the trouble may be the SEND DETECT portion which consists of Logic Elements 11, 1 and the time delay network. This can be checked as follows:
    - *1*. Remove Logic cards A2A9, A2A27, and A2A8 from the logic rack.
    - *2*. Insert a card extender into the A2A8 slot.
    - *3*. Connect card A2A8 to the Card Extender.
    - *4*. Connect the oscilloscope SYNC INPUT Lead to TP1.
    - *5*. Connect the oscilloscope Channel A INPUT Lead to Terminal 38.
    - *6*. Adjust the oscilloscope TIME/CM Control to 10 Msec.
    - *7*. The trace from Channel A should be a positive pulse; the delay from the trigger point should be 40 milliseconds.

8. If this cannot be obtained by adjustment of R4, connect the oscilloscope Channel B INPUT Lead to TP3.

Note. Each time an attempt is made to obtain the trace, +5 volts must be applied to input 7 of Logic element 11. This can be done by touching terminal 50 with a lead from the junction of C3 and L3.

9. The trace should be similar to step 7, except the Channel A trade should negative.

10. If this is obtained, Logic Element 1 is bad.

11. If this is not obtained, connect the VTVM COMMON lead to Terminal 28, and the VTVM DC Lead to TP1. A ground reading should be obtained. If it is not, Logic Element 11 is defective.

12. If this is obtained the network consisting of Q1, Q2, Q3, R1, R2, R3, R4, R5, R6, R7, C5 and C14 is defective.

(4) Card A2A11—Logic Element 6 or 7 may be defective.

(5) Card A2A10—Logic Element 9, 8, or 15 may be defective.

Note. This logic would most likely be defective during message checks involving the use of the manual retransmit or manual cancel capability.

Note. If the 3 RPT lamp on the Control and Indicator Panel fails to light (during actual operation only) in spite of a 3 REPEAT or 3 CANCEL condition the network consisting of R4, C6, and Q3, or Logic element 21, 22, or 23 may be defective. Also, if Logic card A2A19 is faulty under this symptom, the network consisting of C11, C10, R6, CR3, and Logic element 24 may be defective.

(6) Card A2A5—Logic element 10, 7, 4, 14, 19, 2, or 9 may be defective. Also if there is trouble on this card during testing or operation in which a stop facility is used, Logic element 16, 5, 15, 11, or 20 may be defective.

(7) Card A2A5—Logic element 15, 14, 2, or 4 may be defective.

Note. This would be applicable only if the retransmit capability were being used during testing, or if the TCU is requesting retransmission of a received message during operation.

(8) Card A2A6—Logic Element 7, 6, or 16 may be defective.

(9) Card A2A9—If the TCU is operating in the CRYPTO mode, the network consisting of R7, R8, R9, R10, C7, CR1, Q4 and Q3 may be defective.

(10) Card A2A18—The network consisting of R1, R2, R3, R4, CR1, CR2, Q1, and Q2 may be defective.

(11) Card A2A1—The network consisting of R1, R2, R13, R14, R15, R16, R17, L9, L10, L11, L12, C15, C16, C17, Q5 and Q6 is defective provided + and −6.2 volts is present on this card where required.

(12) Card A2A13 (If present)—Perform the troubleshooting procedure in table 2-6.

(13) Card A2A7—This card, if defective, should be checked out according to the procedures in table 2-3, item 17, 18c, 19c, 20, 21f, 24f, 22i, 25b, 23b, MONITOR LAMP DOES NOT LIGHT, TIMING GENERATOR LOGIC CARD, A2A7.

g. If the output TTY device is not blinded (which can be determined if the control characters are being printed out or printout occurs in spite of a stop condition), the trouble depends on the card failure. Card A2A5—Logic element 7, 2, 12, 11, 20, 15, 5, 18, or 6 may be bad.

h. If the blind is not performed on the TCU transmit end, which can be seen by the fact that the precedence character is printed out before the message header, the trouble may be as shown below.

(1) Card A2A9—Logic element 10 may be defective.

(2) Card A2A14—Logic element 19 may be defective.

i. If the message prints out erratically, and and Card A2A1 is faulty, the network consisting of R3, R4, R5, R6, R7, R20, R21, L5, L6, L15, L16, C9, C10, C11, Q1, and Q2 is defective provided + and −12 volts is present on this card where required.

Table 2-6. Disconnect Line Trouble Chart

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
Incorrect Printout.	Message transmission cannot be performed.	Card A2A13	(1) Perform the A2A13 adjustment procedure described in TM 11-5815-355-12. (2) If the procedure checks out correctly, perform the procedure given in table 2-7 for isolator assembly. (3) If the procedure does not check out correctly, repeat the procedure, this time with step (11) changed so that the VTVM DC lead is connected to the junction of R14 and pin 2 of Logic Element 21. Also in this case, in step (22) watch for a rise on the VTVM meter from zero volts. (4) If this procedure checks out correctly, the network consisting of R14, R15, R16, and Q7 is bad. The trouble can be further isolated by checking the resistors. (5) If this procedure does not check out correctly, connect the VTVM common lead to terminal 3. (6) Obtain a lead, terminated on one end by an alligator clip and on the other end by a tip jack. (7) Connect the alligator clip to the junction of C1 and L2. ***Caution:* This is connected to +5 volts dc; do not allow the tip end to come in contact with the equipment.** (8) Touch the tip end of the lead to terminal 26, then disconnect the alligator clip. (9) Connect the VTVM DC lead to the junction of R1 and pin 10 of Logic Element 16 and observe a ground reading. (10) If this reading is not observed, Logic Element 16 is defective. If the ground is observed, proceed to step (11). (11) Repeat step (7). (12) Touch the tip end of the lead to terminal 23. Disconnect the alligator clip, and observe that the VTVM reads +3.7 volts dc. (13) If this reading is not observed, Logic Element 16 is defective. If the reading is observed, proceed to step (14). (14) Repeat step (7). (15) Touch the tip end of the lead to terminal 26, then disconnect the alligator clip. (16) Connect the VTVM DC lead to the junction of R14 and pin 2 of Logic Element 21 and observe ground reading. (17) If this is not obtained Logic Element 21 is defective. If it is, proceed to step (18). (18) Repeat step (7). (19) Touch the tip end of the lead to terminal 25, disconnect the alligator clip, and observe a VTVM reading of +3.7 volts. (20) If this is not obtained, Logic Element 21 is defective. If it is, proceed to step (21). (21) Repeat step (7). (22) Touch the tip end of the lead to terminal 26, then disconnect the alligator clip. (23) Connect the VTVM DC lead to the junction of R1 and pin 10 of Logic Element 16. (24) Repeat step (7). (25) Hold the tip end of the lead to terminal 24 and observe a VTVM reading of +3.7 volts dc. Disconnect the alligator clip. (26) If the correct reading is not obtained, Logic Element 11 is defective. If it is, proceed to step 37.

Table 2-6. Disconnect Line Trouble Chart—Continued

Item No.	Trouble symptom	Probable trouble	Checks and corrective maintenance
			(37) Return to step 1 and perform the A2A13 adjustment procedure, except alter step (11) as follows: (a) Obtain the oscilloscope. (b) Connect its Channel A INPUT Lead to the junction of R5 and Q4. (c) Place the oscilloscope TIME/CM switch to 0.2 sec/cm. (d) Place the oscilloscope Channel A SENSITIVITY switch to 1. Also, in step (22) stop the stop watch when a positive pulse of +3.7 volts is noted. (38) If the correct results are obtained, there is discontinuity on this card. If not, return to step 1 and perform the A2A13 adjustment procedure except alter step (11) to connect the oscilloscope Channel A INPUT Lead to the junction of R6 and R7. Also, in step (22) stop the stop watch when a negative 3.7 volt pulse is noted. (39) If the correct results are obtained, R5, R7, or Q4 is defective. The trouble can be isolated by checking R5 and R7. (40) If the correct results are not obtained, return to step 1 and alter step (11) to connect the oscilloscope Channel A INPUT Lead to the junction of R8 and R9. Also in step (22) stop the stop watch when a positive pulse of 3 volts is noted. (41) If the correct results are obtained, R6, R8, or Q5 is defective. The trouble can be isolated by checking R6 and R8. (42) If the correct results are not obtained, perform step (7). (43) Touch the tip end of the lead to terminal 23. (44) Connect the VTVM DC lead to the junction of Q2 and R3, and observe a ground reading. (45) If this is obtained, Q2, Q3, or Q6, of the associated circuitry is defective. If the correct reading is not obtained, Q1, R1, or R2 is defective.

Table 2-7. Disconnect Line Trouble Chart for Isolator Assembly

Item number	Trouble symptom	Probable trouble	Checks and corrective maintenance
Incorrect Print-out.	Message transmission cannot be performed.	Isolator Assembly, RF-216/G.	(1) Check output of J2 with a VTVM. Set VTVM to read a + d.c. voltage, and connect + probe to pin A of J2 and the − probe to pin B of J2. If +6 volts is obtained continue the following steps. If 0 volt to +0.5 volt is obtained, there is a discontinuity problem between the Isolator Assembly and its output wiring within the TCU. (2) If +6 volts is obtained, connect the + probe of the VTVM to A2P4 pin A and the − probe of the VTVM to A2P4 pin B. The VTVM should read +6 volts, if it does not, there is a discontinuity problem between A2A13 and A2P4. (3) If +6 volts is obtained, perform the following steps. (4) Disconnect A2P5 and connect the + probe of the VTVM to A2P5 pin A and the − probe of the VTVM to A2P5 pin B and read +5.5V. If this voltage does not exist, there is a discontinuity problem between A2P5 and Power Supply PP-4571/G. (5) If this voltage is measured reconnect A2P5 and check that DS1 and DS2 are lit. (6) If DS1 and DS2 are lit, then F3, F4, or FL3 is defective. (7) If either DS1 or DS2 is not lit, then PS1 is defective. (8) If both DS1 and DS2 are not lit, then F1, F2 may be defective. (9) If F1 and F2 are good, then S1 may be defective. (10) If S1 is good, then FL1, FL2 may be defective. (11) If FL1 and FL2 are good then PS1 is defective.

2-9. Troubleshooting During Operation

Once a malfunction has occurred during operation and trouble analysis has isolated the trouble to a logic card, the trouble must then be isolated further. This is done by testing out the defective card in an "off-line" operating TCU. The procedures for accomplishing this is similar to those for checking logic cards which have malfunctioned during message testing (monthly maintenance). Before checking is actually performed, it is advisable to set up the TCU to test the transmission and reception of two consecutive messages. Then the trouble charts can be referred to and tests made based upon the card which has malfunctioned. These tests are provided in Part A, SENDING OF TWO CONSECUTIVE MESSAGES.

CHAPTER 3

DIRECT SUPPORT, GENERAL SUPPORT, AND DEPOT REPAIR

Note. Direct support, general support, and depot maintenance of the TCU includes trouble location and corrective procedures described in TM 11-5815-335-12 and in Chapter 2 of this manual. For information concerning the authorization of tools and test equipment and the extent of maintenance authorized for each maintenance category, refer to the maintenance allocation chart (app C, TM 11-5815-335-12).

Section I. REPAIRS AND ALIGNMENT

3-1. General Parts Replacement Techniques

Most of the parts in Teletypewriter Control Unit C-7050/G (TCU) can be reached and replaced without special procedures. Figures 3-1 through 3-18 illustrate the parts of the TCU. Procedures for removing and replacing those parts which are not obvious are given in paragraphs 3-3 through 3-16. The following precautions apply:

a. If the settings of variable resistors are disturbed, or if any variable resistors are replaced, perform the adjustment procedures given in TM 11-5815-335-12.

b. The TCU equipment is transistorized. Use a pencil-type soldering iron with a 25-watt maximum capacity. If the iron must be used with ac, use an isolating transformer between the iron and the ac line. Do not use a soldering gun; damaging voltages can be induced in the components.

c. When soldering the transistor leads, solder them quickly; wherever wiring permits, use a heat sink (such as a long-nosed pliers) between the soldered joint and the transistor. Use approximately the same length and dress of transistor leads as used originally.

d. Before making repairs to the printed circuit boards, refer to TB SIG 222.

e. During disassembly procedures, be careful not to damage gaskets.

f. During assembly procedures, insure that all gaskets are in place and all screws are used and properly tightened.

3-2. Tools Required for Removal and Replacement of Parts

The tools required for removal and replacement of parts in the TCU are contained in Tool Kit, Electronic Equipment TK-100/G and Tool Kit, Electronic TK-105/G.

3-3. Replacement of Toggle Switches
(fig. 3-3 and 3-16)

a. Removal. Remove toggle switches as follows:

(1) Tag and unsolder the leads from the switch terminals.

(2) Remove the locknut from the switch shaft.

(3) Remove the switch.

b. Replacement. Replace toggle switches as follows:

(1) Insert a replacement switch into the panel.

(2) Replace and tighten the locknut.

(3) Connect and solder all leads to the replacement switch terminals.

3-4. Replacement of Rotary or Pushbutton Switches
(fig. 3-16 and 3-1)

a. Removal. Remove rotary or pushbutton switches as follows:

(1) Tag and remove the leads from the switch terminals.

(2) On rotary switches, loosen the two Allenhead retaining screws that secure the knob to the shaft.

(3) Remove the knob.

(4) Remove the locknut located on the opposite side of the panel from the switch body.

(5) Remove the switch from the unit.

b. Replacement. Replace rotary or pushbutton switches as follows:

(1) Insert a replacement switch into the unit and tighten the locknut.

(2) Connect and solder all leads to the proper terminals on the replacement switch.

(3) Replace the switch's knob. (On rotary switches, tighten the Allen-head retaining screws.)

3-5. Replacement of Lampholder

a. Removal. Remove the lampholder as follows:

(1) Tag and remove the leads from the lampholder terminals.

(2) Unscrew and remove the lamp lens.

(3) Remove the locknut located on the front of the panel.

(4) Remove the lampholder.

b. Replacement. Replace the lampholder as follows:

(1) Insert the replacement lampholder into the panel.

(2) Replace and tighten the locknut on the lampholder.

(3) Connect and solder all leads to the replacement lampholder terminals.

(4) Replace the lamp lens.

3-6. Replacement of Audible Alarm

a. Removal. Remove the audible alarm assembly as follows:

(1) Tag and remove the leads from the audible alarm terminals.

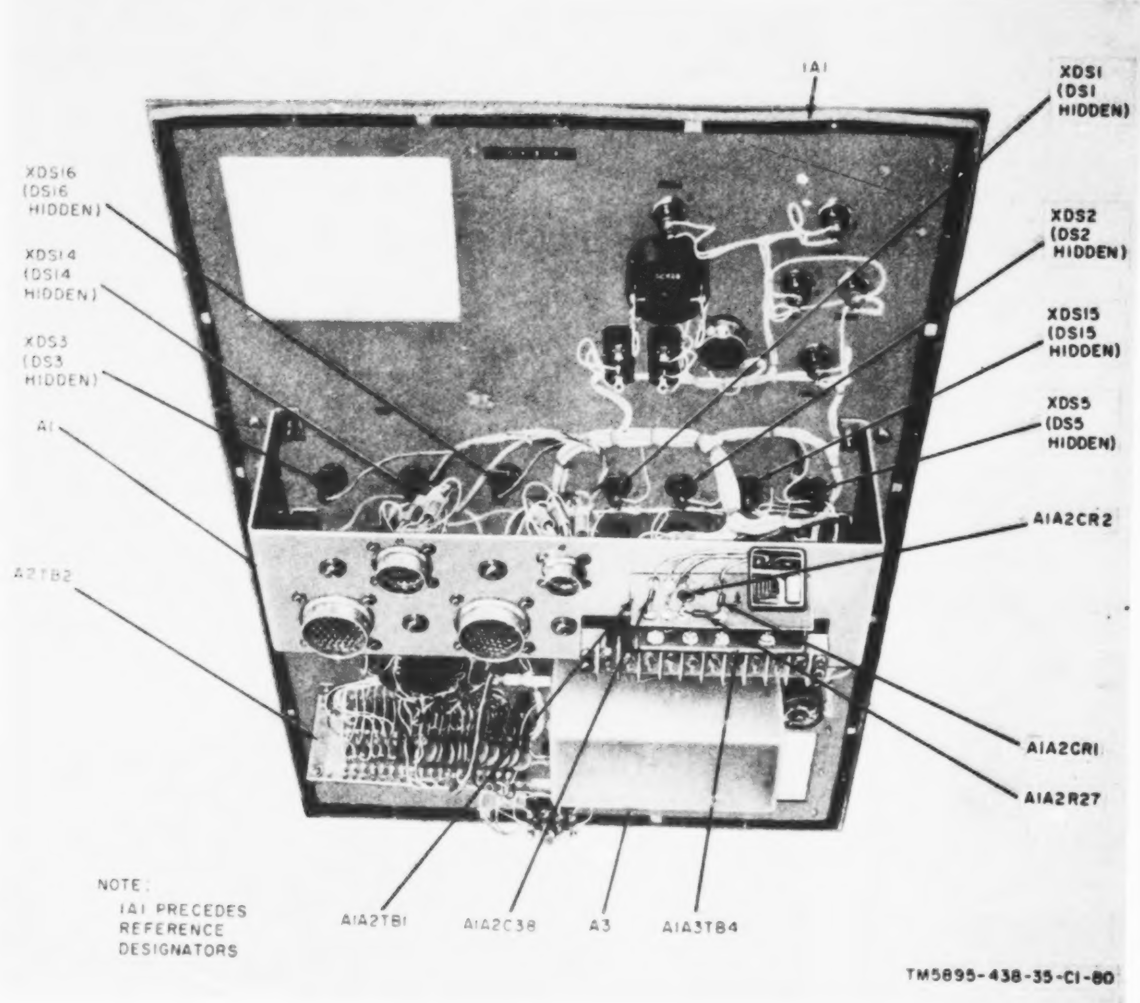

1A1
XDS16
(DS16
HIDDEN)
XDS14
(DS14
HIDDEN)
XDS3
(DS3
HIDDEN)
A1
A2TB2
XDS1
(DS1
HIDDEN)
XDS2
(DS2
HIDDEN)
XDS15
(DS15
HIDDEN)
XDS5
(DS5
HIDDEN)
A1A2CR2
A1A2CR1
A1A2R27
NOTE:
1A1 PRECEDES
REFERENCE
DESIGNATORS
A1A2TB1
A1A2C38
A3
A1A3TB4
TM5895-438-35-C1-80

Figure 3-1. Control-Indicator Panel A1, rear oblique view, parts location.

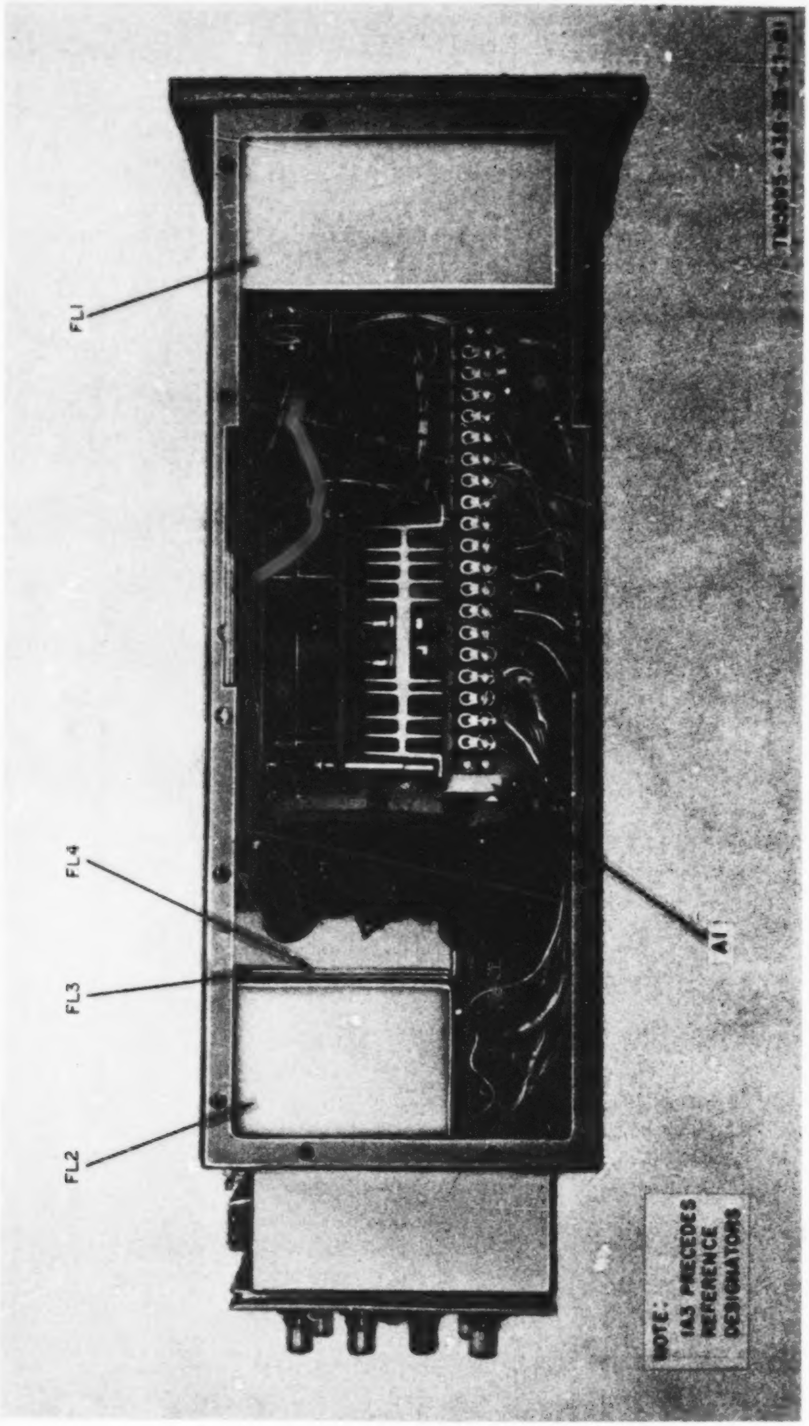

FL1
FL4
FL3
FL2
A1
NOTE:
1A3 PRECEDES
REFERENCE
DESIGNATORS

Figure 3-2. Power supply and filter Assembly 1A3, top view, parts location.

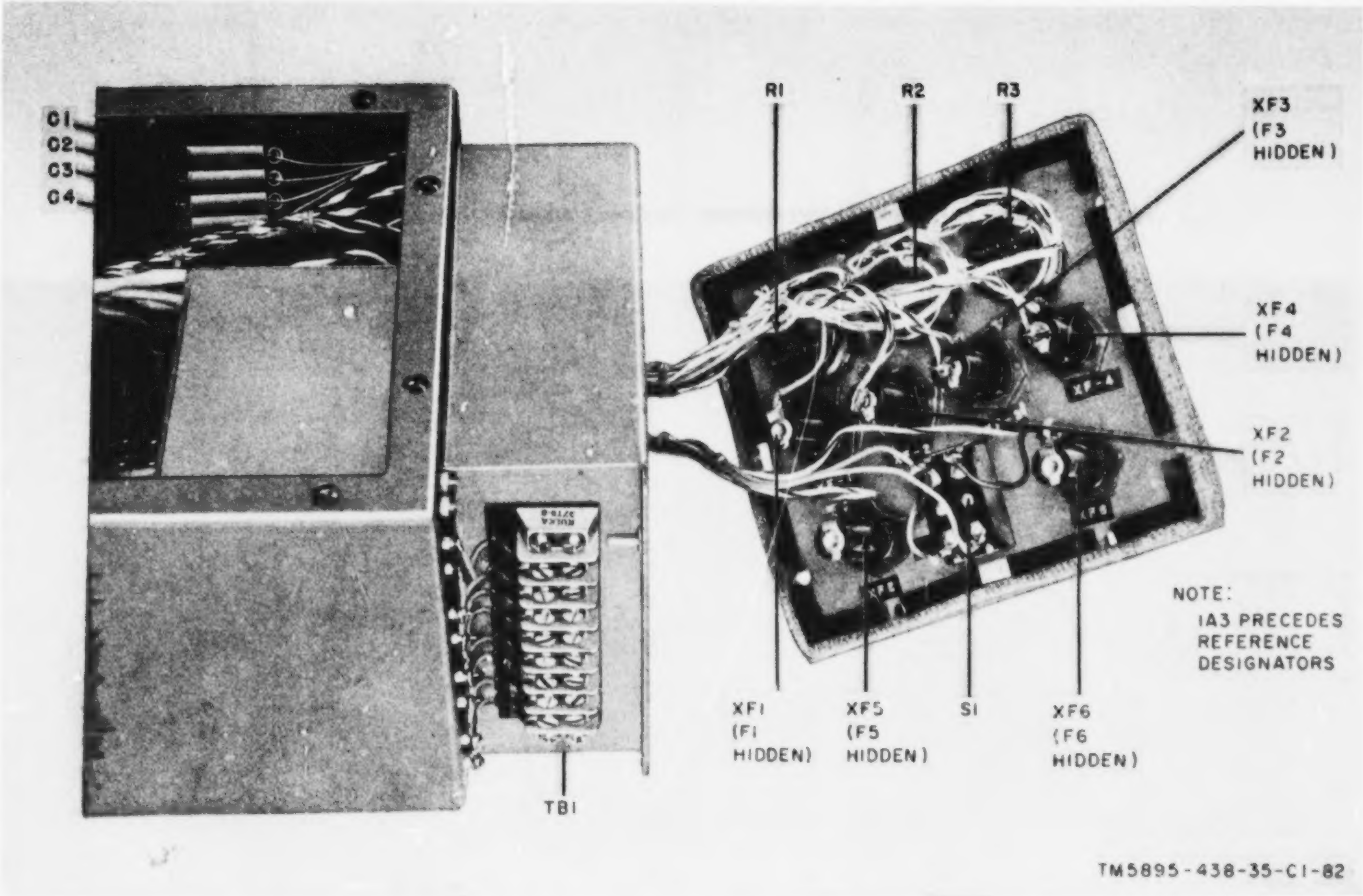

C1
C2
C3
C4
R1
R2
R3
XF3
(F3
HIDDEN)
XF4
(F4
HIDDEN)
XF2
(F2
HIDDEN)
NOTE:
1A3 PRECEDES
REFERENCE
DESIGNATORS
XF1
(F1
HIDDEN)
XF5
(F5
HIDDEN)
S1
XF6
(F6
HIDDEN)
TB1
TM5895-438-35-C1-82

Figure 3-3. Power supply and filter assembly 1A3, front cover removed, parts location.

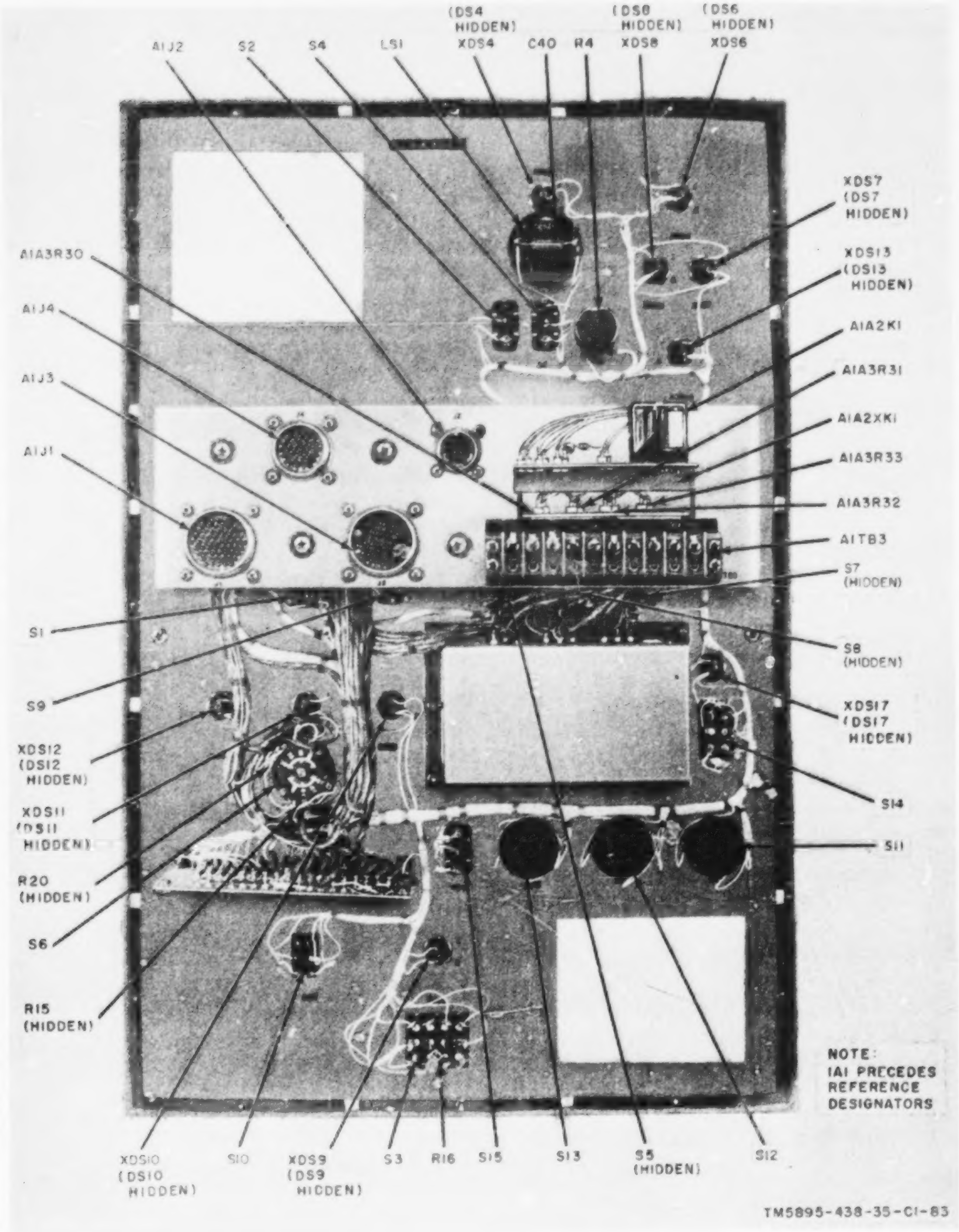

A1J2
S2
S4
LS1
(DS4 HIDDEN) XDS4
C40
R4
(DS8 HIDDEN) XDS8
(DS6 HIDDEN) XDS6
XDS7 (DS7 HIDDEN)
XDS13 (DS13 HIDDEN)
A1A2K1
A1A3R31
A1A2XK1
A1A3R33
A1A3R32
A1TB3
S7 (HIDDEN)
S8 (HIDDEN)
XDS17 (DS17 HIDDEN)
S14
S11
A1A3R30
A1J4
A1J3
A1J1
S1
S9
XDS12 (DS12 HIDDEN)
XDS11 (DS11 HIDDEN)
R20 (HIDDEN)
S6
R15 (HIDDEN)
XDS10 (DS10 HIDDEN)
S10
XDS9 (DS9 HIDDEN)
S3
R16
S15
S13
S5 (HIDDEN)
S12
NOTE: 1A1 PRECEDES REFERENCE DESIGNATORS
TM5895-438-35-C1-83

Figure 3-4. Control-indicator panel 1A1, rear view, parts location.

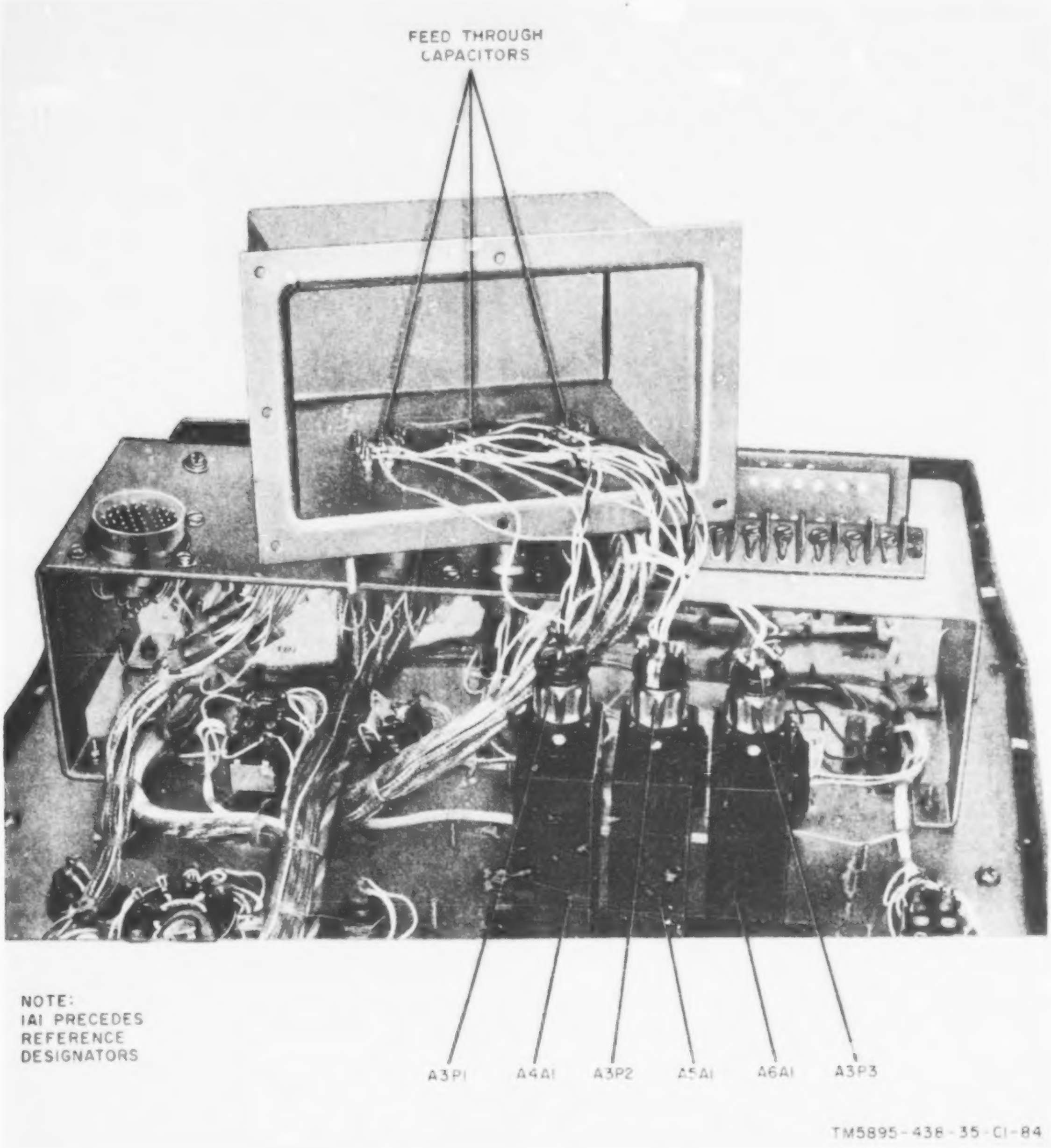

FEED THROUGH CAPACITORS
NOTE:
1A1 PRECEDES
REFERENCE
DESIGNATORS
A3P1
A4A1
A3P2
A5A1
A6A1
A3P3
TM5895-438-35-C1-84

Figure 3-5. Control-indicator panel 1A1, rear view, cover A1A3 removed, parts location.

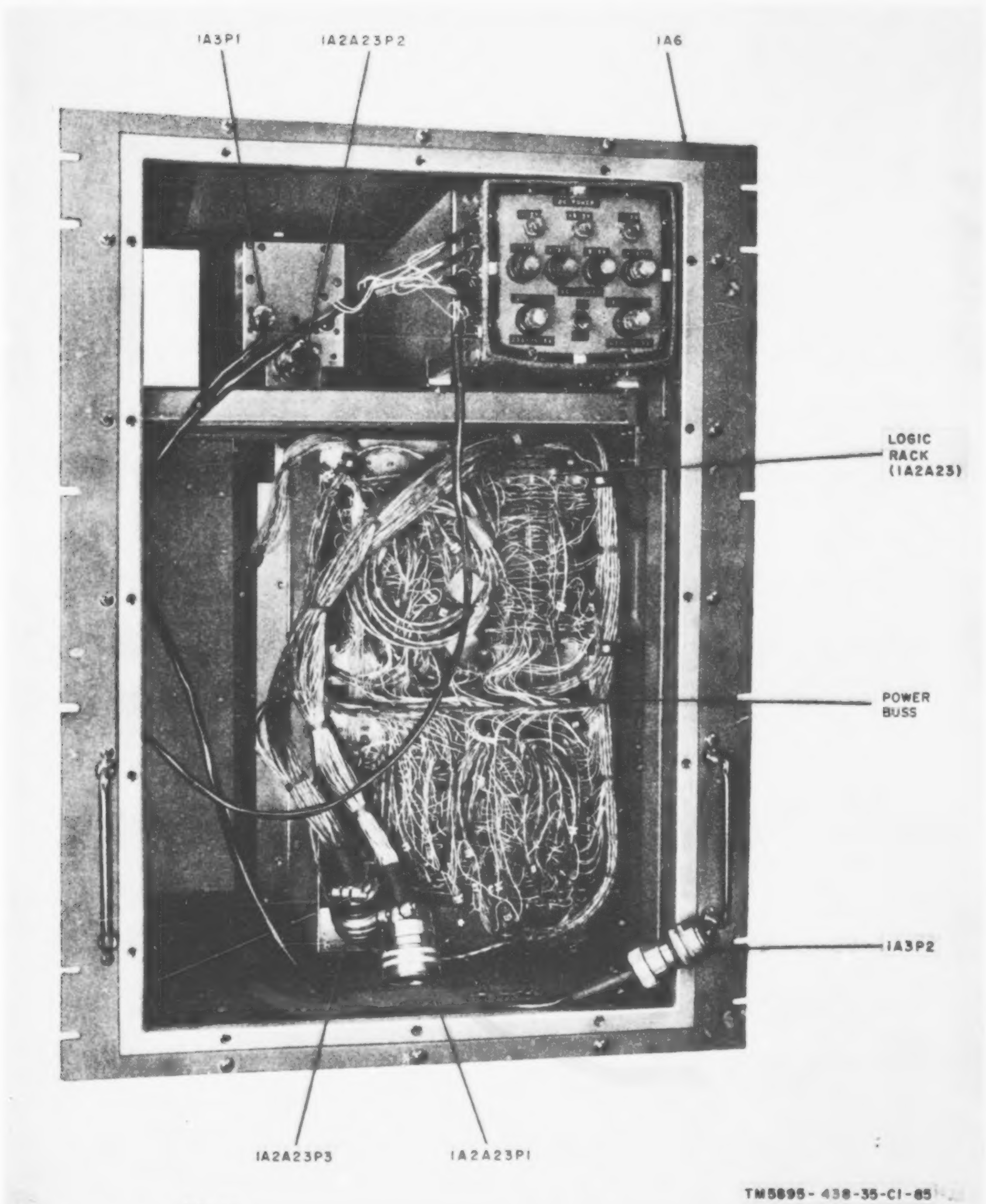

1A3P1
1A2A23P2
1A6
LOGIC RACK (1A2A23)
POWER BUSS
1A3P2
1A2A23P3
1A2A23P1
TM5895-438-35-C1-85

Figure 3-6. TCU front view control-indicator panel removed, parts location.

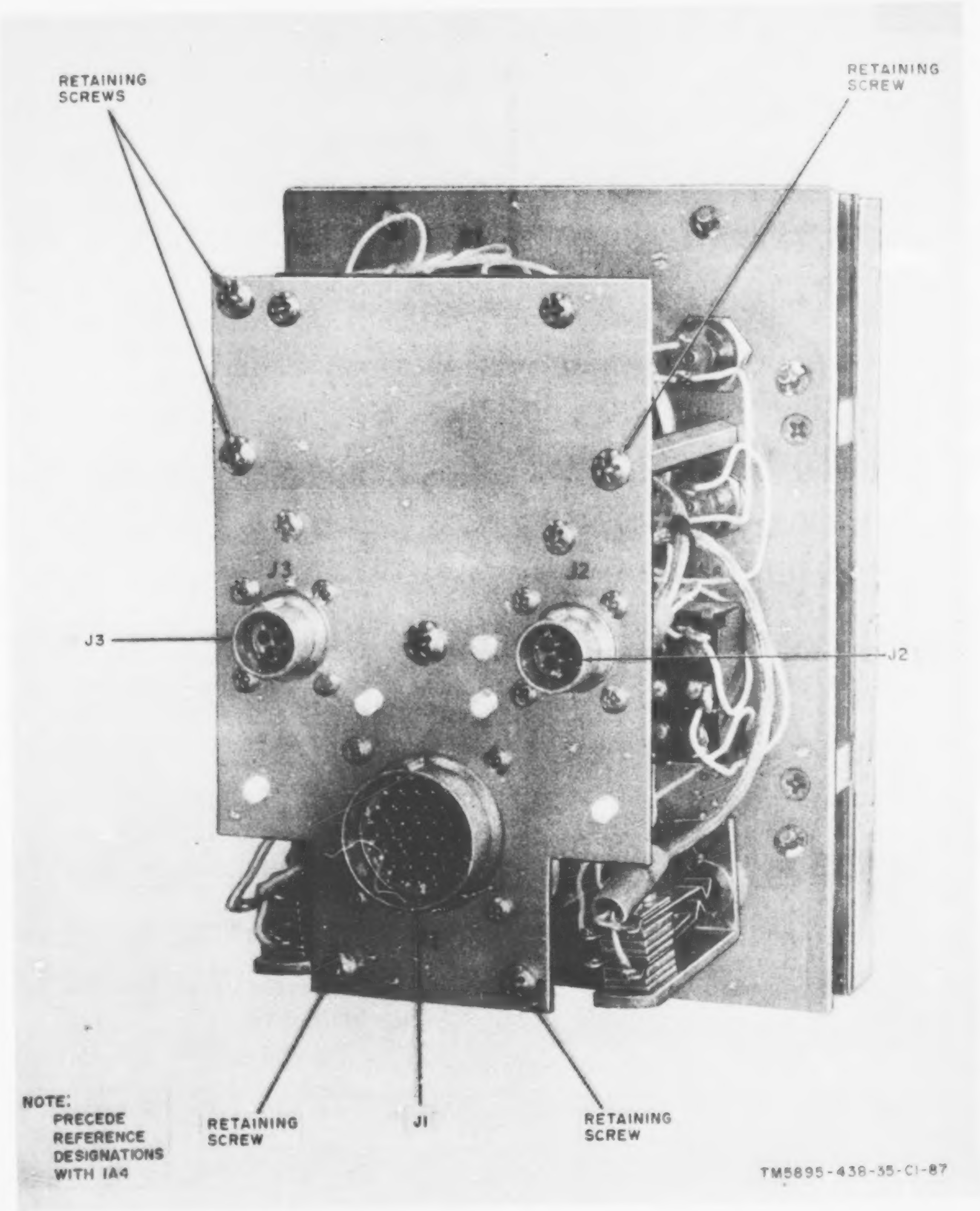
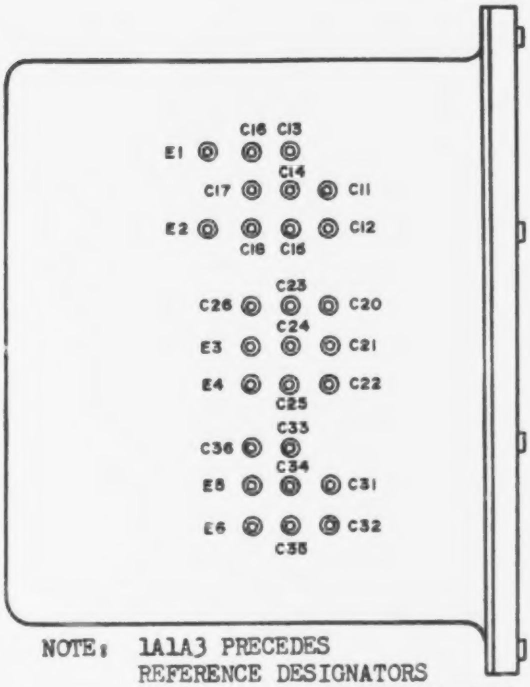

RETAINING SCREWS
RETAINING SCREW
J3
J2
J3
J2
NOTE:
PRECEDE REFERENCE DESIGNATIONS WITH 1A4
RETAINING SCREW
J1
RETAINING SCREW
TM5895-438-35-C1-87

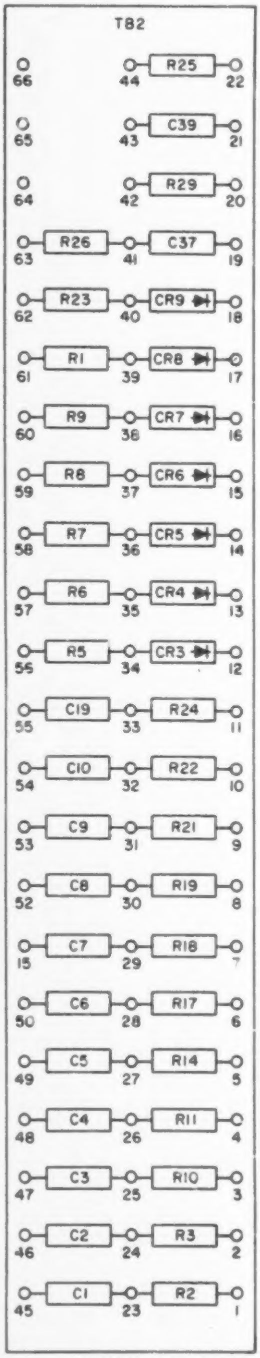
Figure 3-7. Simulation test unit 1A4, rear view, parts location


C16 C13
E1
C14
C17 C11
E2 C12
C18 C15
C23
C26 C20
C24
E3 C21
E4 C22
C25
C33
C36
C34
E5 C31
E6 C32
C35

NOTE: 1A1A3 PRECEDES REFERENCE DESIGNATORS

TM 5895-438-35-88

Figure 3-8. Nixie Housing 1A1A3, internal view, parts location.


TB2
66 44 R25 22
65 43 C39 21
64 42 R29 20
63 R26 41 C37 19
62 R23 40 CR9 18
61 R1 39 CR8 17
60 R9 38 CR7 16
59 R8 37 CR6 15
58 R7 36 CR5 14
57 R6 35 CR4 13
56 R5 34 CR3 12
55 C19 33 R24 11
54 C10 32 R22 10
53 C9 31 R21 9
52 C8 30 R19 8
15 C7 29 R18 7
50 C6 28 R17 6
49 C5 27 R14 5
48 C4 26 R11 4
47 C3 25 R10 3
46 C2 24 R3 2
45 C1 23 R2 1

NOTE: 1A1A2 PRECEDES REFERENCE DESIGNATOR:

TM5895-438-35-89

Figure 3-9. Terminal Board 1A1TB2, top view, parts location.

(2) Remove the audible alarm locknut.
(3) Remove the audible alarm unit.

b. Replacement. Replace the audible alarm unit as follows:

(1) Insert the audible alarm into the unit.
(2) Replace and tighten the locknut on the unit.
(3) Connect and solder all leads to the audible alarm terminals.

3-7. Replacement of Nixie Tubes

Replace a nixie tube as follows:

a. Removal.

(1) Remove the six retaining screws that secure the protective plexiglass window to the control-indicator panel.
(2) Remove the window.
(3) Grasp the defective nixie tube and carefully pull the tube out, gently rocking it from side to side.

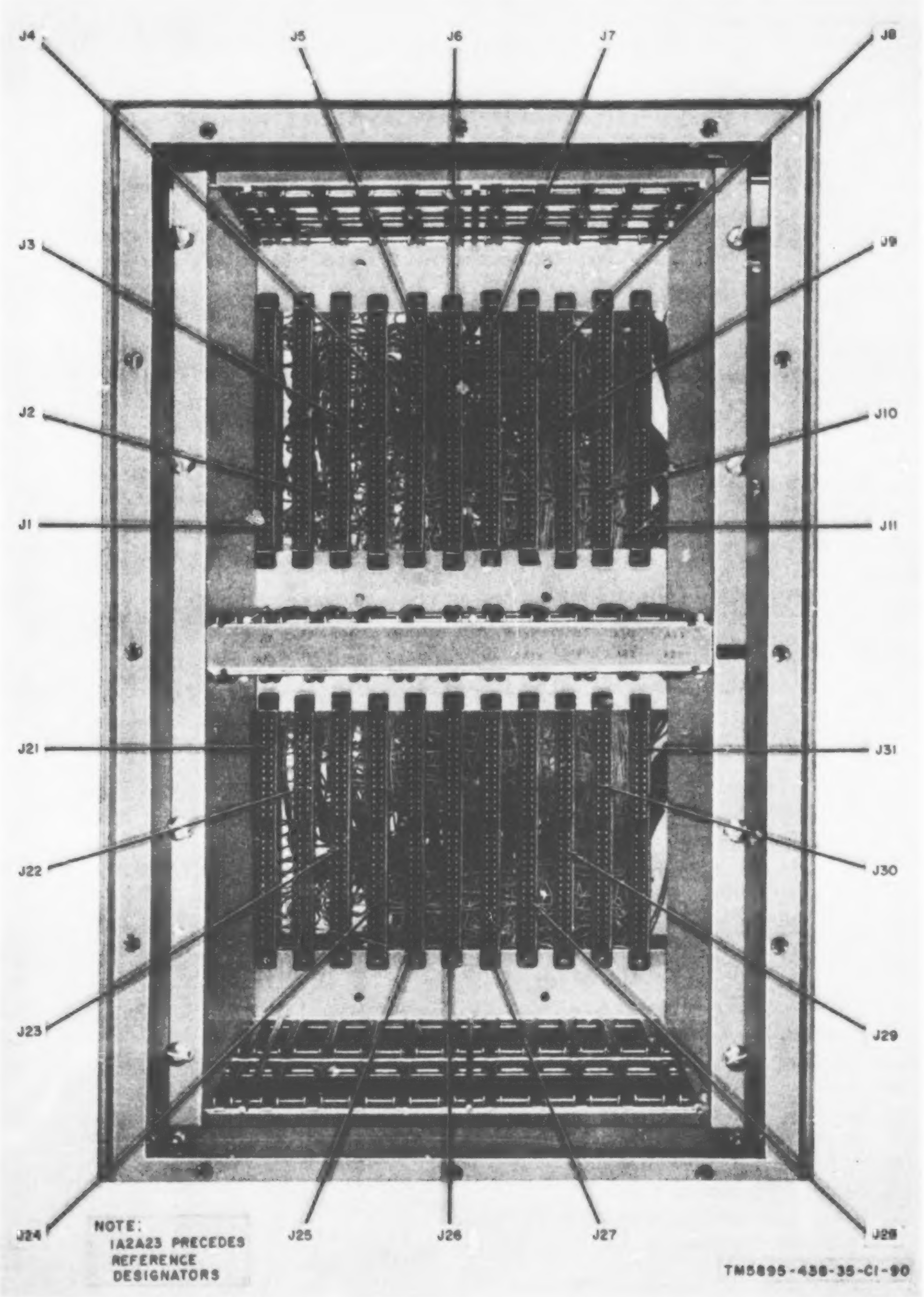

J4
J5
J6
J7
J8
J3
J9
J2
J10
J1
J11
J21
J31
J22
J30
J23
J29
J24
J25
J26
J27
J28
NOTE:
1A2A23 PRECEDES
REFERENCE
DESIGNATORS
TM5895-438-35-C1-90

Figure 3-10. Logic rack 1A2, front view, parts location.

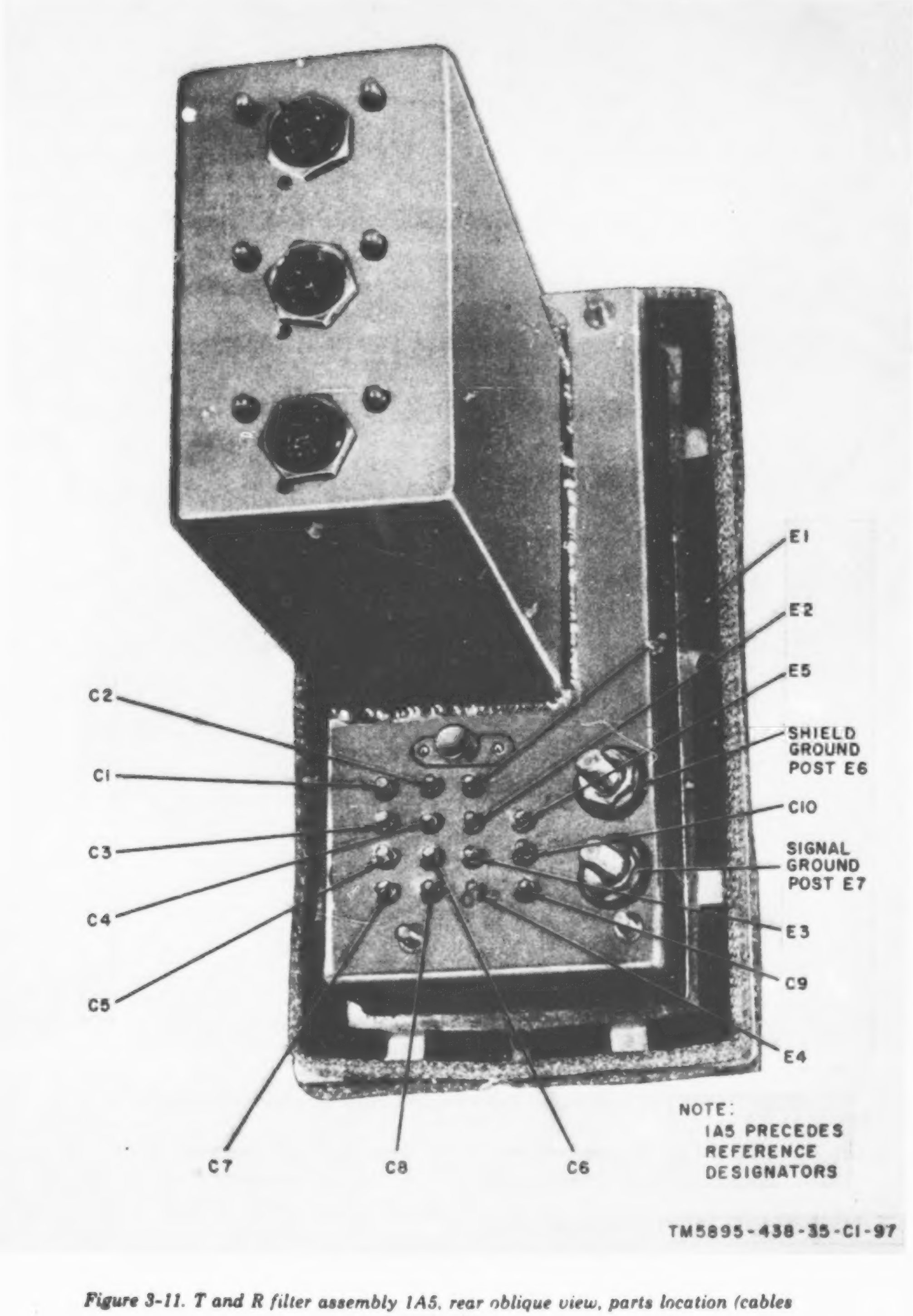
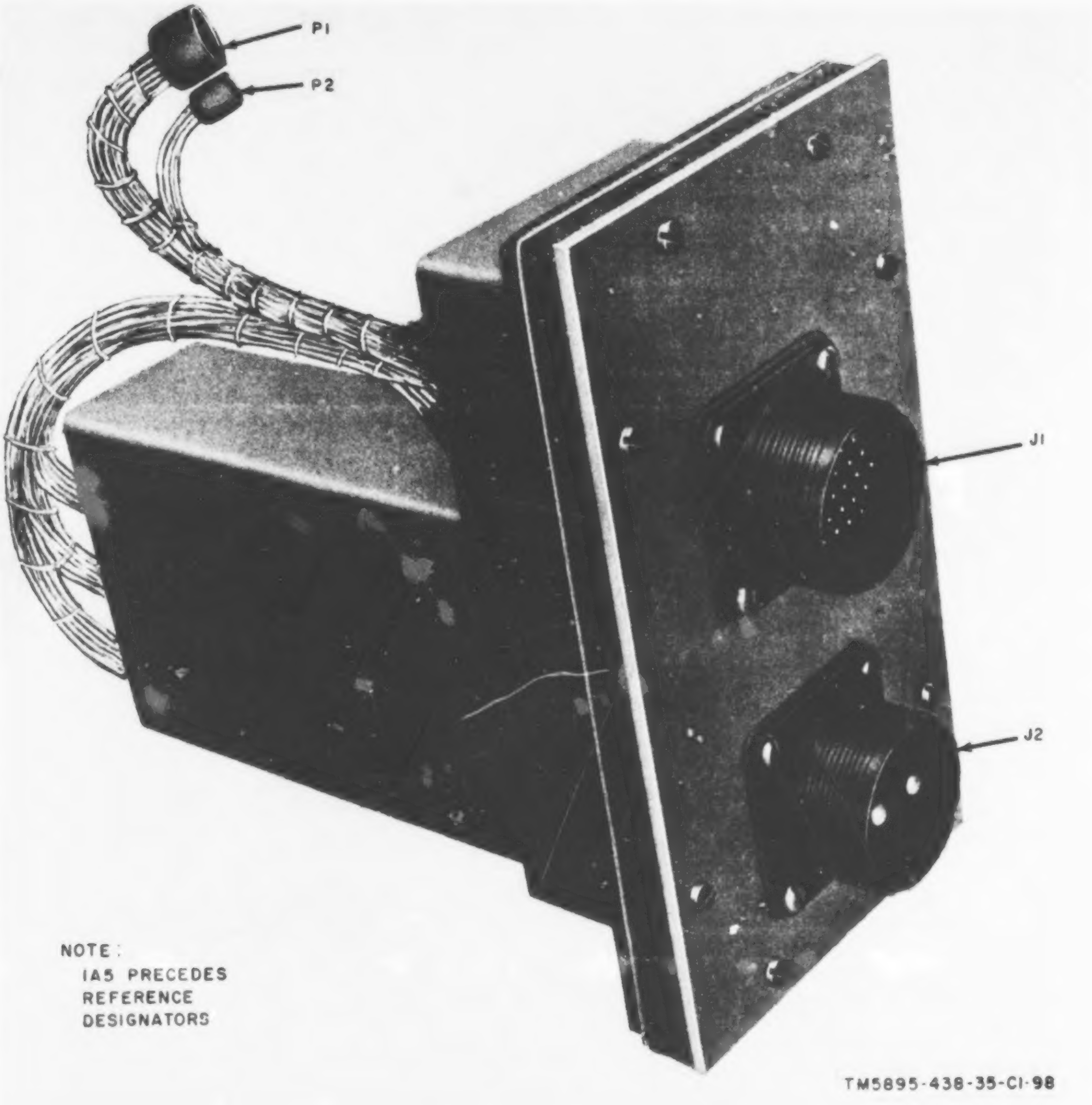

E1
E2
E5
SHIELD GROUND POST E6
C10
SIGNAL GROUND POST E7
E3
C9
E4
C2
C1
C3
C4
C5
C7
C8
C6
NOTE:
1A5 PRECEDES REFERENCE DESIGNATORS
TM5895-438-35-C1-97

Figure 3-11. T and R filter assembly 1A5, rear oblique view, parts location (cables removed).



NOTE:
1A5 PRECEDES
REFERENCE
DESIGNATORS

TM5895-438-35-C1-98

Figure 3-12. T and R filter assembly 1A5, left oblique view, parts location.

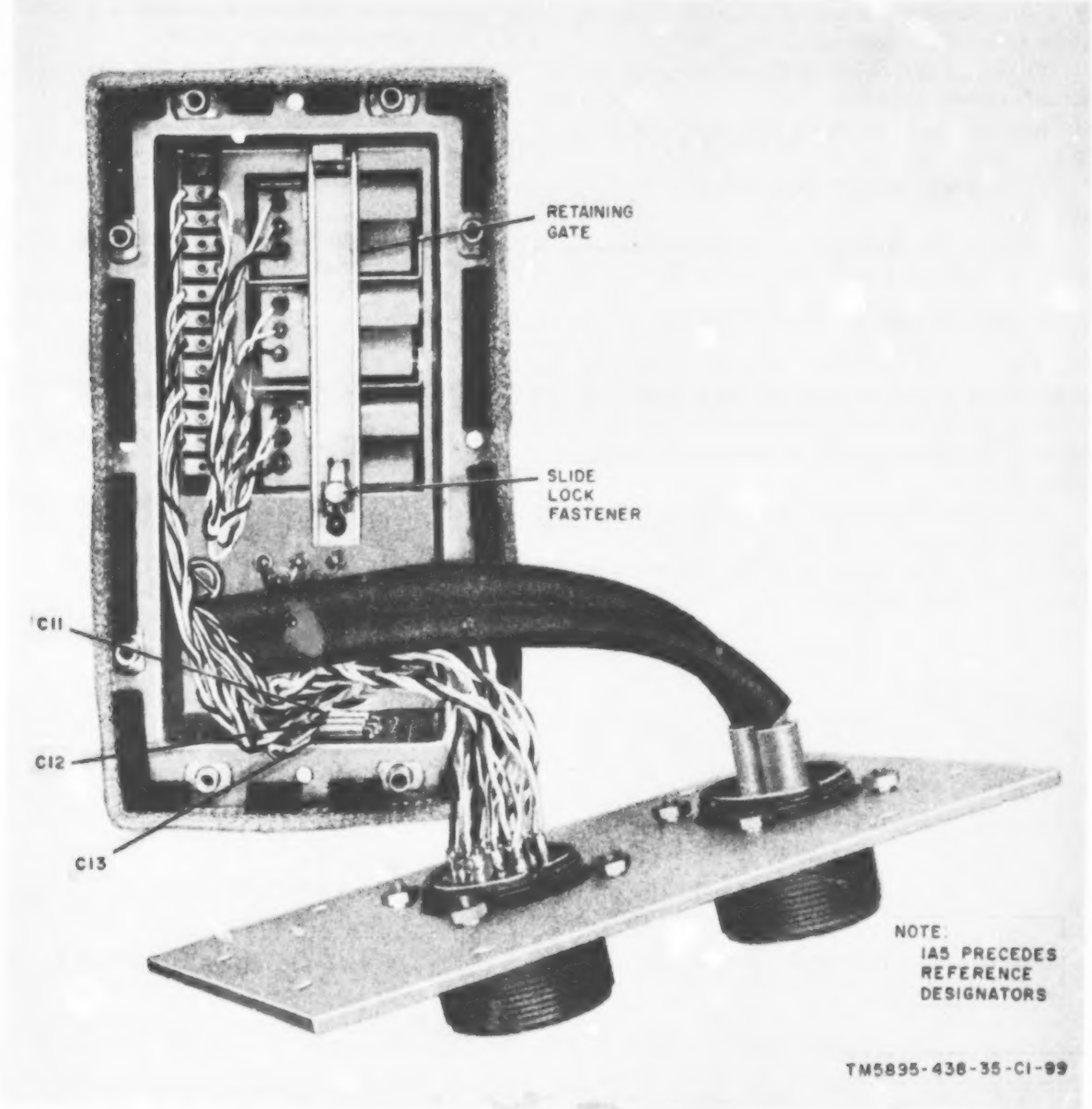

RETAINING GATE
SLIDE LOCK FASTENER
C11
C12
C13
NOTE:
1A5 PRECEDES REFERENCE DESIGNATORS
TM5835-436-35-CI-99

Figure 3-13. T and R filter assembly 1A5, front view with cover removed, parts location.

retaining nut located behind the dust cover.

(3) Remove the jack from the panel.

b. Replacement. Replace phone jacks as follows:

(1) Insert a replacement jack into the panel.

(2) Replace and tighten the locknut.

(3) Connect and solder all leads to the replacement jack terminals.

3-9. Replacement of Plug-in Relay

a. Removal. Remove the plug-in relay as follows:

(1) The relay is secured to its mating jack by a wire-retaining strap. Pivot this strap to either side of the relay case (fig. 3-1).

(2) Grasp the relay case and pull the relay out of the mating jack.

b. Replacement. Replace the relay as follows:

(1) Insert a replacement relay into the jack.

(2) Pivot the wire-retaining strap until it is locked in place on top of the relay cover.

3-10. Replacement of Nixie Decoders

a. Removal. To reach the nixie decoders, cover A1A3 (fig. 3-5) and the nixie tube protective window located on the front of the Control-Indicator panel must be removed. Proceed as follows:

(1) Remove the eight retaining nuts and washers that secure cover A1A3 to the Control-Indicator panel and carefully lift the cover to expose the nixie decoders.

(2) Grasp the metal collar of the plug, on the decoder to be replaced, and twist it a quarter turn counterclockwise (CCW).

(3) Separate the plug from the nixie decoder by pulling straight up and out.

(4) Remove the six screws that secure the protective plexiglass nixie tube window to the front of the Control-Indicator Panel and remove the window.

(5) Remove the nixie tube from the decoder to be replaced. (fig. 3-15).

(6) Remove the two decoder retaining screws.

(7) Remove the nixie decoder assembly.

b. Replacement. Replace a nixie decoder as follows:

(1) Insert a replacement nixie decoder and secure it with the two retaining screws.

(2) Insert the plug into the decoder jack and lock it in place by twisting the metal collar one-quarter of a turn clockwise.

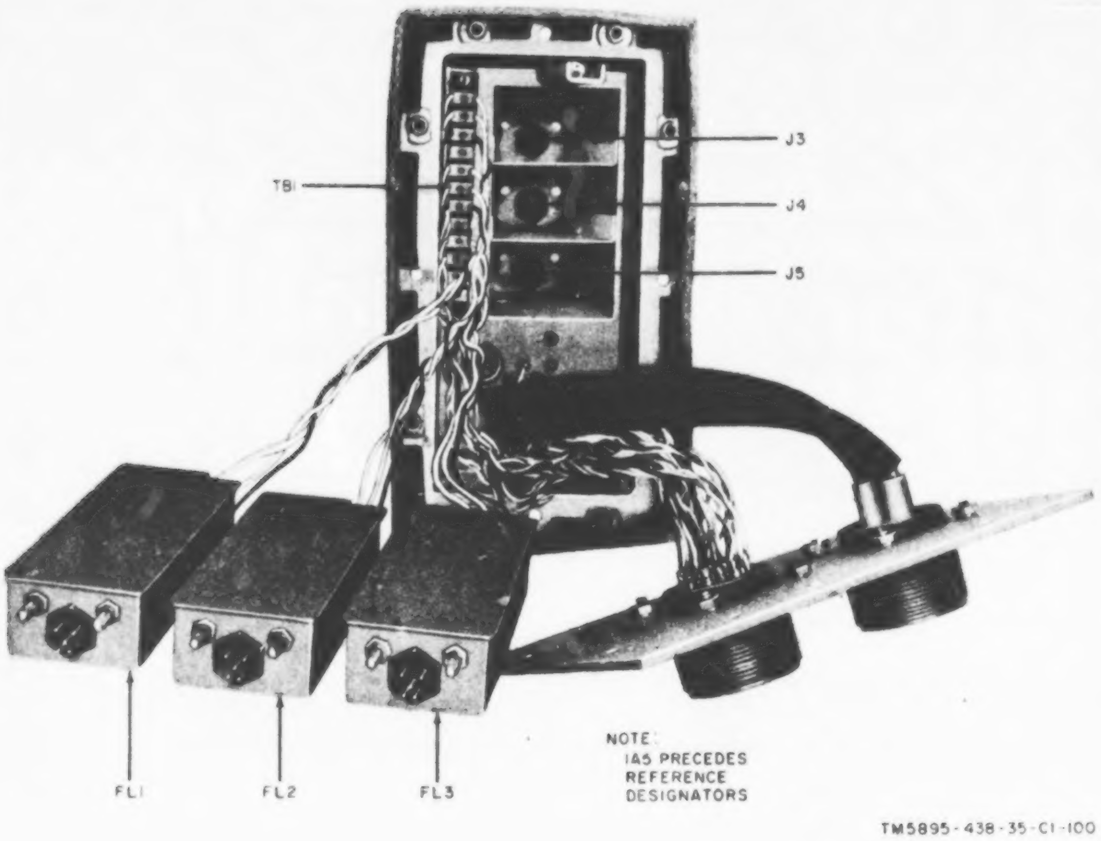

J3
TB1
J4
J5
FL1
FL2
FL3
NOTE:
1A5 PRECEDES
REFERENCE
DESIGNATORS
TM5895-438-35-C1-100

Figure 3-14. T and R filter assembly 1A5, front cover removed and parts removed, parts location.

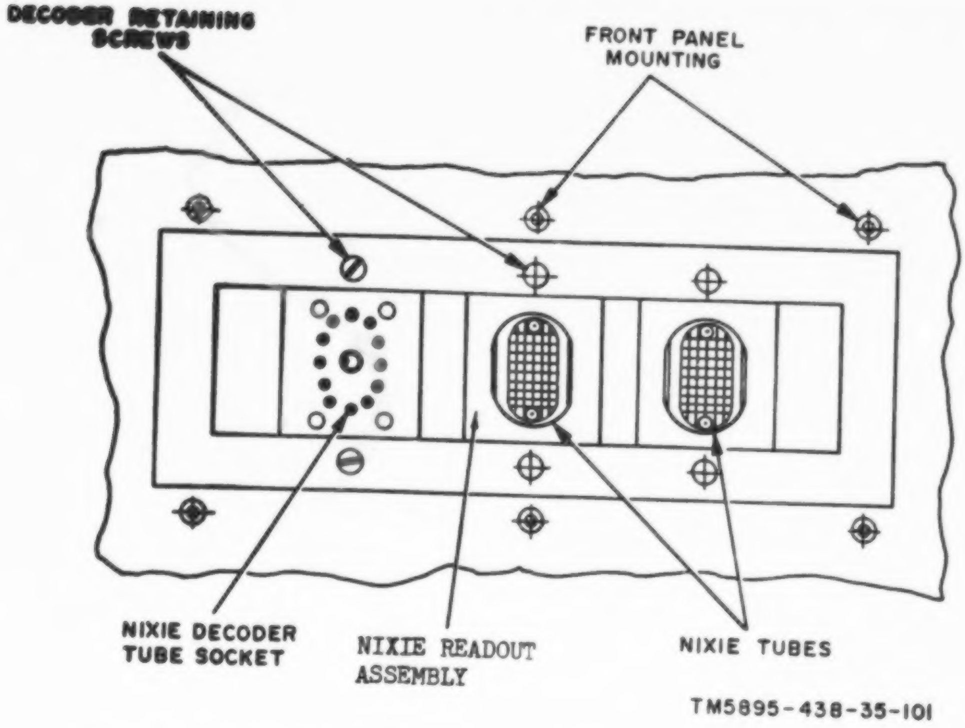

DECODER RETAINING SCREWS
FRONT PANEL MOUNTING
NIXIE DECODER TUBE SOCKET
NIXIE READOUT ASSEMBLY
NIXIE TUBES
TM5895-438-35-101

Figure 3-15. Control Indicator Panel, partial front view, showing nixie tubes and decoder socket.

(3) Carefully replace cover assembly A1A3 and secure it using the eight retaining nuts and washers.
(4) Replace the nixie tube in the decoder socket.
(5) Replace the protective plexiglass window on the Control-Indicator front panel and secure it with the six retaining screws and washers.

3-11. Replacement of Fuseholder

Replace fuseholders as follows:

a. Removal.
(1) Unsolder the leads from the fuseholder terminals.
(2) Remove the locknut from the face of the panel.
(3) Remove the fuseholder.

b. Replacement.
(1) Insert a replacement fuseholder into the panel.
(2) Replace and tighten the fuseholder locknut.
(3) Connect and solder all leads to the fuseholder terminals.

3-12. Replacement of Potentiometers

a. Removal. Remove potentiometers as follows:
(1) Tag and remove the leads from the potentiometer terminals.
(2) Remove the potentiometer's knob (if applicable) by loosening the two Allen-head retaining screws.
(3) Remove the locknut from the potentiometer's shaft.

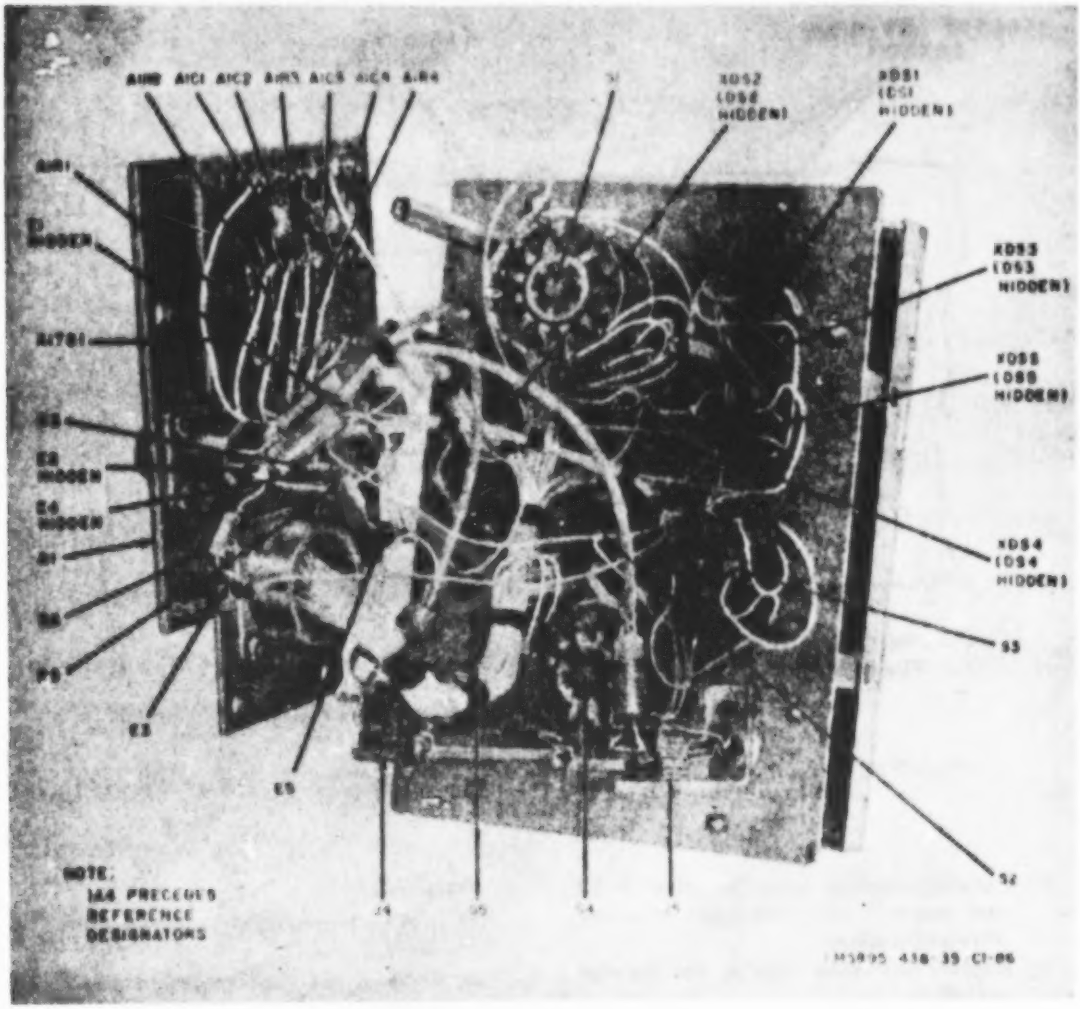

A1R2
A1C1
A1C2
A1R3
A1C3
A1C4
A1R4
J1
XDS2
(DS2
HIDDEN)
XDS1
(DS1
HIDDEN)
A1R1
E1
HIDDEN
A1TB1
E5
E2
HIDDEN
E4
HIDDEN
A1
E6
P1
E3
E5
XDS3
(DS3
HIDDEN)
XDS5
(DS5
HIDDEN)
XDS4
(DS4
HIDDEN)
S3
S2
J4
S5
S4
J5
NOTE:
1A4 PRECEDES
REFERENCE
DESIGNATORS
MS895 436 35 C1-06

Figure 3-16. Simulation test unit A4, rear view, partially disassembled, parts list.

b. Replacement. Replace potentiometers as follows:

(1) Insert the replacement potentiometer into the panel.

(2) Replace and tighten the locknut.

(3) Connect and solder all leads to the replacement potentiometer terminals.

(4) Replace the potentiometer's knob (if applicable) and tighten the Allen-head retaining screws.

3-13. Replacement of Feedthrough Capacitors

(fig. 3-8)

a. Removal. Remove feedthrough capacitors as follows:

(1) Unsolder the leads from both ends of the capacitor.

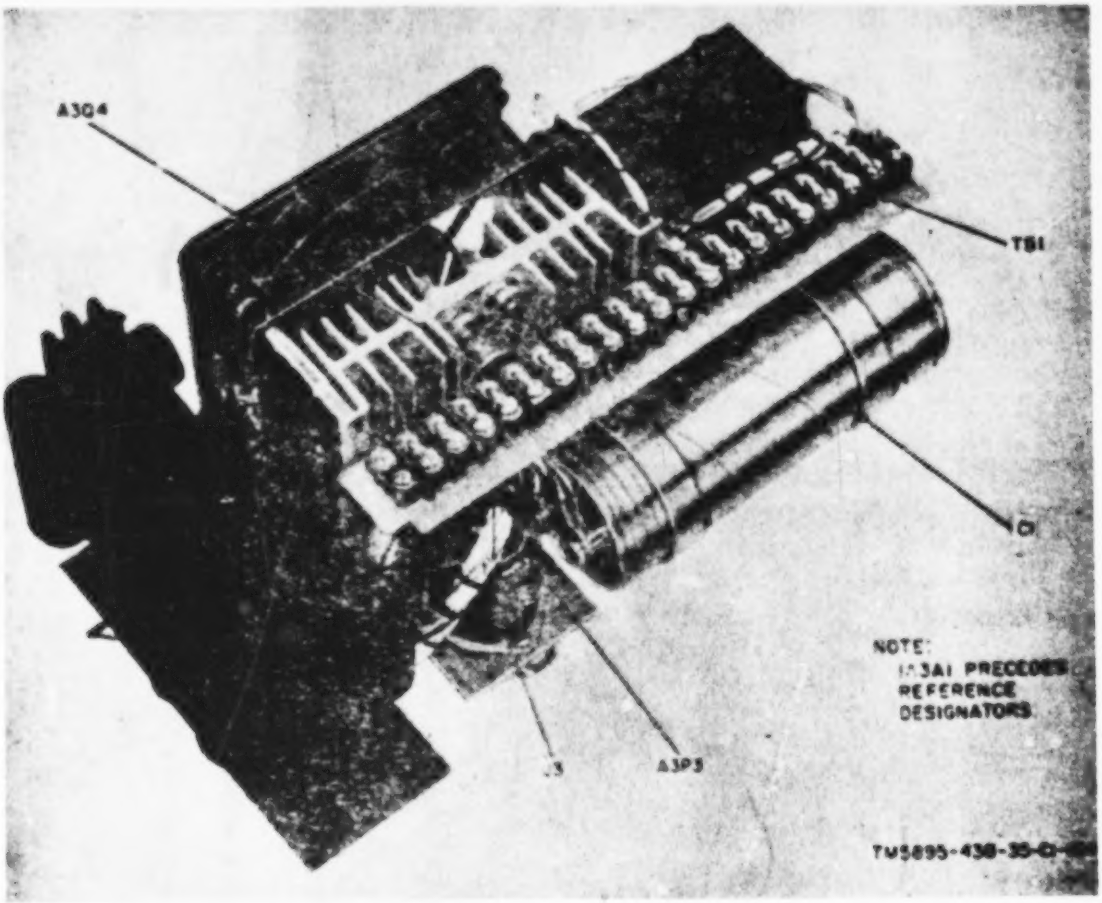


Figure 3-17. Power supply subassembly A1, parts location.

(2) Use the special ring-shaped soldering iron tip (locally fabricated) to unsolder and remove the defective capacitor.

b. Replacement. Replace feedthrough capacitors as follows:

(1) Insert a replacement feedthrough capacitor into the assembly.

(2) Insert the solder ring, supplied with the new capacitor, over the body of the capacitor.

(3) Using the special ring-shaped tip and soldering iron, heat the solder ring until the solder flows freely. Remove the soldering iron and support the body of the capacitor until the solder hardens.

(4) Replace the leads on each end of the capacitor.

3-14. Replacement of Logic Rack Jacks (fig. 3-10)

a. To replace a logic rack jack (logic rack removed from the TCU) proceed as follows:

(1) Tag and remove the leads from the, jack to be replaced using the Termi-point extraction tool (AMP Inc. Part No. 465195-2).

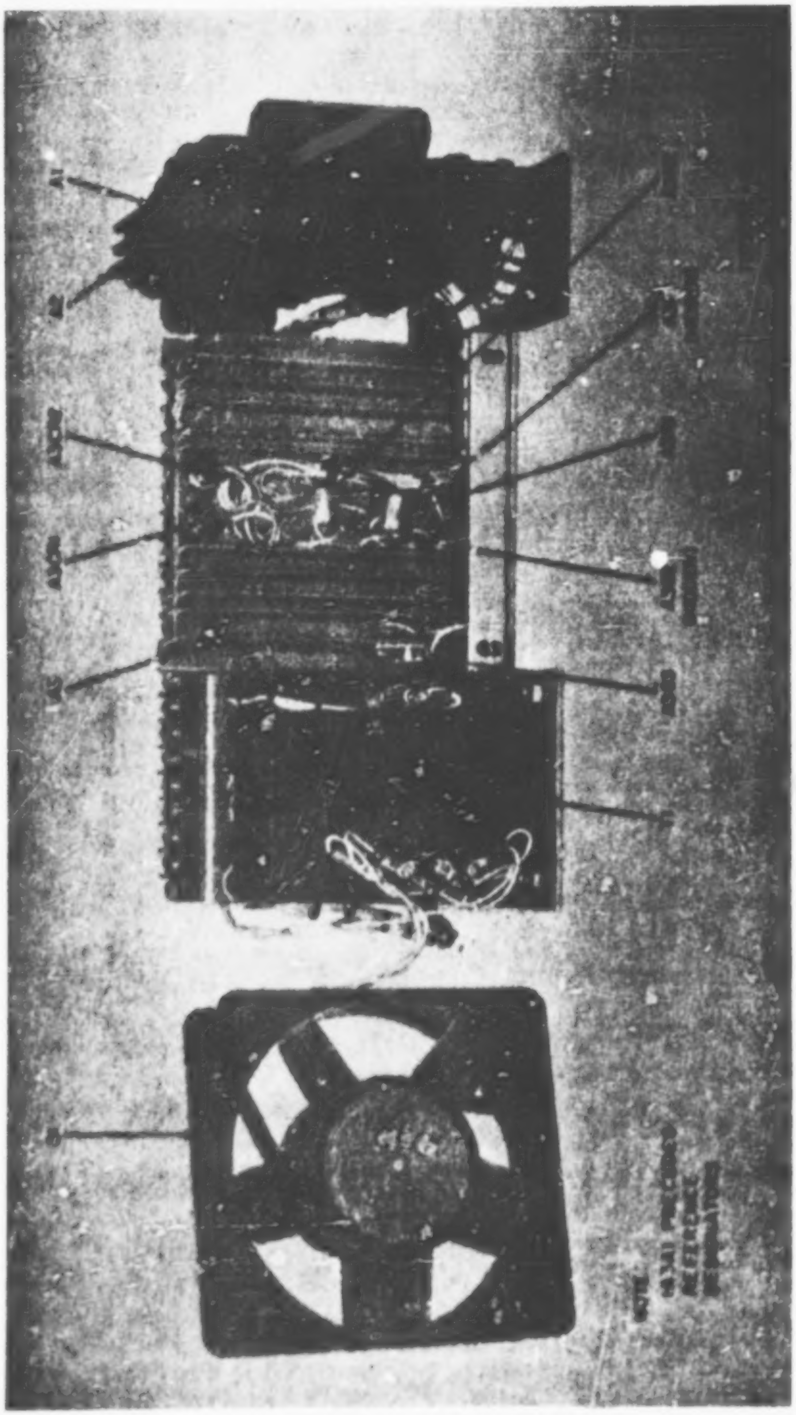


Figure 3-18. Power supply subassembly A1, partially disassembled, parts location.

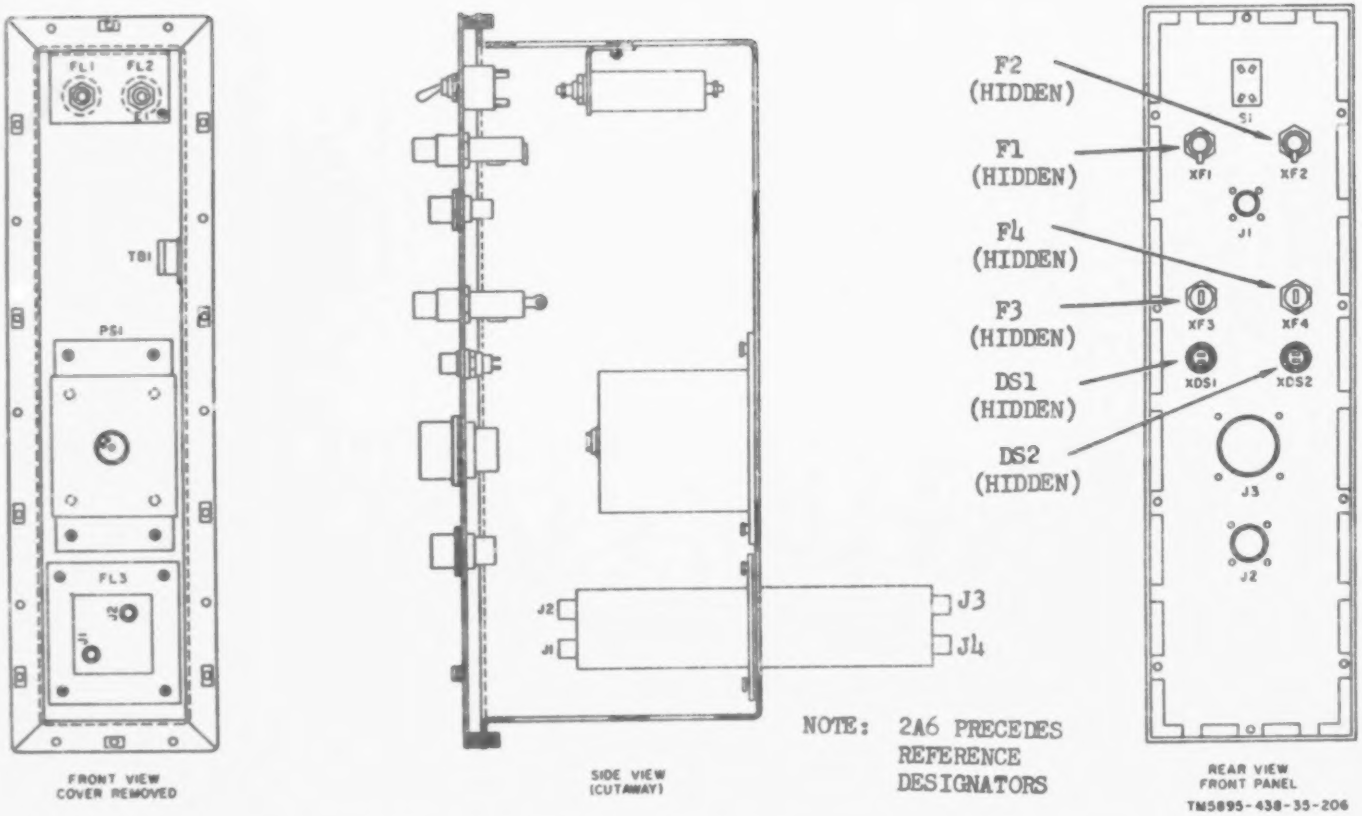

FL1
FL2
TB1
PS1
FL3
J2
J1
FRONT VIEW
COVER REMOVED
J2
J1
J3
J4
SIDE VIEW
(CUTAWAY)
NOTE: 2A6 PRECEDES
REFERENCE
DESIGNATORS
F2
(HIDDEN)
F1
(HIDDEN)
F4
(HIDDEN)
F3
(HIDDEN)
DS1
(HIDDEN)
DS2
(HIDDEN)
S1
XF1
XF2
J1
XF3
XF4
XDS1
XDS2
J3
J2
REAR VIEW
FRONT PANEL
TM5895-438-35-206

Figure 3-19. Isolator Assembly 2A6, front panel removed, parts location.

(2) Remove the two screws and nuts that secure the jack to the logic rack.

(3) Remove the jack.

b. Replacement. Replace the jack as follows:

(1) Insert the replacement jack into the vacated jack position.

(2) Secure the jack using the two screws and nuts removed from the defective jack.

(3) Starting from the center of the jack and working out toward either end, connect all leads to the jack's terminals (push in contact at end of each wire).

3-15. Replacement of T & R Filter A5FL1, A5FL2, or A5FL3 Subassemblies

(figs. 3-13 and 3-14)

To replace either A5FL1, A5FL2 or A5FL3 proceed as follows:

a. Removal. Remove filters A5FL1, A5FL2 or A5FL3 as follows:

(1) Remove the front cover of the T and R filter, by removing the eight screws in the rear cover, and let the cover hang down.

(2) Unfasten the twist lock fastener and swing the retaining gate down (fig. 3-13).

(3) Slide the defective filter assembly out of its nest and tag and remove the connecting wiring from TB1.

(4) Tag and remove the leads from the filter terminals and remove the filter.

b. Replacement. Replace a filter assembly as follows:

(1) Connect and solder the leads to the filter terminals and replace the filter in its nest.

(2) Connect filter leads to the appropriate terminals on TB1.

(3) Close the retaining gate and fasten the twist lock fastener.

(4) Replace the front cover of the T and R filter and secure in place with the eight screws and washers.

3-16. Replacement of Power Supply Subassembly A3

a. Removal.

(1) Tag and disconnect wires that connect TB1 on power supply to TCU red power supply chassis.

(2) Remove three screws that hold power supply subassembly to bottom of TCU red power supply chassis.

(3) Lift subassembly out of chassis.

b. Replacement.

(1) Mount subassembly in TCU red power supply chassis, using three screws removed in step *a*(2) above.

(2) Connect wires removed in step *a*(1) above to TB1.

3-17. Replacement of Power Supply Component Parts

(figs. 3-2, 3-17, and 3-18)

a. Removal.

(1) Remove two bolts that hold spacers between printed circuit boards and printed circuit board L-bracket.

(2) Unplug printed circuit boards.

(3) Tag and remove all wires connected to TB1 and expose terminals of T1.

(4) Remove two screws that hold fan bracket to subassembly chassis; remove fan and bracket.

(5) Remove two screws that hold fan bracket to fan.

(6) Unplug P3 from J3.

(7) Remove four screws that hold heat sink to subassembly chassis; remove heat sink.

(8) Remove four screws that hold transformer T1 to subassembly chassis.

(9) Carefully lift T1 away from subassembly chassis so that terminals on rear of T1 are exposed.

(10) Tag and remove all wires connected to T1; remove T1.

(11) Remove four nuts that hold brackets for capacitor C1 to subassembly chassis; remove brackets.

(12) Lift capacitor C1 away from subassembly chassis.

(13) Tag and remove all wires connected to C1; remove C1.

(14) Remove two screws that hold L-bracket to subassembly chassis between printed circuit board jacks J1 and J2; remove L-bracket.

(15) Remove four screws that hold jacks J1 and J2 mounting spacers to subassembly chassis.

(16) Lift jacks J1 and J2 and mounting spacers away from chassis.

(17) Remove screws that hold mounting spacers to jacks J1 and J2; remove spacers.

(18) Remove four screws that hold TB1 to chassis.

(19) Remove two screws that hold jack J3 to chassis mounting bracket.

(20) To remove jacks J1, J2, and J3, tag and unsolder all wires connected to the jacks.

b. Replacement.

Note. The following steps must be performed using only replacement components that are known to be good.

(1) Solder wires, removed in step *a*(20) to jacks J1, J2, and J3.

(2) Mount jack J3 on chassis mounting bracket, using two screws removed in step *a*(19).

(3) Mount TB1 on chassis, using four screws removed in step *a*(18).

(4) Attach mounting spacers to jacks J1 and J2, using screws removed in step *a*(17).

(5) Mount jacks J1 and J2 on chassis, using four screws removed in step *a*(15).

(6) Mount L-bracket on chassis between jacks J1 and J2, using two screws removed in step *a*(14).

(7) Connect wires, removed in step *a*(13), to capacitor C1.

(8) Mount C1 on chassis, using brackets and nuts removed in step *a*(11).

(9) Connect wires, removed in steps *a*(11) and *a*(3) to transformer T1.

(10) Mount transformer T1 on chassis, using four screws removed in step *a*(8).

(11) Mount heat sink on chassis, using four screws removed in step *a*(7).

(12) Plug P3 into J3.

(13) Mount fan bracket on fan, using two screws removed in step *a*(5).

(14) Mount fan and bracket on chassis, using two screws removed in step *a*(4).

(15) Connect wires, removed in step *a*(3) to TB1.

(16) Plug printed circuit boards, removed in step *a*(2) into jacks J1 and J2.

(17) Mount spacers between printed circuit boards and L-bracket, using bolts removed in step *a*(1).

3-18. Replacement of Isolator Assembly A6

(fig. 3-19)

a. Removal.

(1) Disconnect the three (3) slugs on the front panel of A6.

(2) Remove the 10 twist lock fasteners on the outer edge of the panel.

(3) Remove the front panel using care not to put stress on the interconnecting wires.

(4) Remove the 10 screws on the outer edges of Assembly A6.

(5) Slide the assembly forward until the back of the panel is accessible.

(6) Remove the two (2) plugs connected to the back of the assembly.

b. Replacement.

(1) Connect the two (2) plugs (P4 and P5) to their respective jack connectors on the rear of Assembly A6.

(2) Slide Assembly A6 into the rack and secure it with the 10 screws provided.

(3) Secure the front panel to the Assembly with the 10 twist lock fasteners provided on the front panel.

(4) Connect the three (3) plugs to their respective Jacks.

3-19. Replacement of Isolator Assembly Component Parts

(fig. 3-19)

a. Removal of PS1.

(1) Remove the four screws on the back mounting of PS1.

(2) Tag wires connected to the terminal header located on the front of PS1 and disconnect wires.

b. Replacement of PS1.

(1) Solder wires removed in step *a*(2) to the terminal header.

(2) Insert the four screws into the back mounting of PS1 and secure.

c. Removal of FL3.

(1) Remove P1 and P2.

(2) Remove the four screws on FL3's bracket.

(3) Pull FL3 forward until it is free of the Unit.

(4) Remove the shielding gasket from the rear of FL3's bracket.

d. Replacement of FL3.

(1) Place the shielding gasket on the rear bracket of FL3.

(2) Insert the four screws into the bracket, insuring that the screws hold the shielding gasket in place.

(3) Insert FL3 into the unit and secure with the screws.

(4) Reconnect P1 and P2.

3-20. Alignment Procedures

Complete alignment procedures for the TCU are found in TM 11-5815-335-12. Perform these procedures for each of the adjustments required.

Section II. GENERAL SUPPORT TESTING PROCEDURES

3-21. General

a. Testing procedures are prepared for use by Signal field maintenance shops and Signal service organizations responsible for general support maintenance of electronic equipment to determine the acceptability repaired electronic equipment must meet before it is returned to the using organization. The testing procedures may also be used as a guide to test equipment repaired at direct support if the proper tools and test equipment are available. A summary of the performance standards is given in paragraph 3-26.

b. Comply with the instructions preceding the body of each chart before proceeding to the chart. Perform each test in sequence. *Do not vary the sequence.* For each step, perform all the actions required in the *Control settings* column; then perform each specific test procedure and verify it against its performance standards.

3-22. Test Equipment, Tools and Materials

All test equipment, tools, and materials required to perform the testing procedures are listed in the following charts and are authorized under TA 11-17, Signal Field Maintenance Shops; and TA 11-100 (11-17), Allowances of Signal Corps Expendable Supplies for Signal Field Maintenance Shops (Continental United States); TOE 11-158D, Signal Depot Company; and TA 11-101 (11-158), Allowances for Signal Corps Expendable Supplies for Signal Depot Company, or are repair part items of the subject equipment authorized for stockage at general support level. Specific models and types of test equipment were used to perform the general support testing procedures. If these testing procedures are performed with other models or types of the test equipment, an allowance must be made for any test results that may differ from those given in the procedures.

a. Test Equipment. Table 3-1 lists the test equipment required for testing.

Table 3-1. Test Equipment Required for Testing Procedures

Equipment	Federal stock No.
Analyzer ZM-3/U (capacitor test set)	6625-229-1060
Multimeter AN/USM-162 (Abbey Electronics Model MM-5, or equal).	6625-953-1287
Oscilloscope (Hewlett-Packard model 140A, or equal), equipped with:	6625-957-0509
Dual-trace Amplifier (Hewlett-Packard model H06-1405A).	6625-930-8118
Time base and delay generator (Hewlett-Packard model 1415A).	6625-930-8119
Data Analysis Center (Radiation Corp model DAS-10).	7740-933-2349
Test Set, Transistor TS-2086/U	6625-902-9562
Voltmeter, digital (Hewlett-Packard model 405CR), or equal.	6625-822-5659
Variable frequency power source (Communication Measurements Laboratories Model 1430 C, or equal).	
Power Supply and Filter Assembly PP-4571/G.	
Regulated Power Supply	6625-051-5986
Tool Kit, Electronic TK-100/G	5180-605-0079

b. Materials. Materials required for testing are listed in table 3–2.

Table 3–2. Materials Required for Testing

Quantity	Item
2	Connector, plug, Burndy BT06AC 12–3S.
1	Connector, plug FW06–14S–2S.
2	Telephone, plug PJ–051B.
1	Connector, plug FW06–10SL–3S.
1	Connector, plug MS 3116F8–4S.
1	Connector, plug MS 3116F8–3S.
17 feet	Cable, power, three-conductor.
2 Do	Wire, electrical No. 18AWG.
7 Do	Wire, insulated electrical No. 18AWG.
1	Resistor, fixed, 12-ohm, 25-watt.
1	Resistor, fixed 1 ohm, 10 watt.
1	Resistor, fixed 60 ohm, 5 watt.
1	Resistor, fixed 6300 ohm, 10 watt.
1	Resistor, fixed 30 ohm, 10 watt
15	Alligator Clips.
15	Test Leads.
1	Polarized plug, three prong.
1	Mercury vapor lamp (with wide band transmission filter) FSN 6695–537–4470.

3–23. Fabrication of Test Cable Assemblies

a. Test Cable Assembly Fabrications. The plug-in units of the TCU are removed from the equipment cabinet for the general support testing procedures. To provide power to the power supply subassembly a fabricated test cable is used. The test cable consists of a three–pin plug and interconnecting wiring. To fabricate this cable follow the procedures given in *b* below. To fabricate a test cable assembly to test the simulation test unit follow the procedures given in *c* below. To fabricate a cable to connect the power supply to a standard wall outlet follow the procedure given in *d* below.

b. Fabricated Power Supply Adapter Cable Assembly (fig. 3–20).

(1) Connect and solder a 5-foot length of three-conductor power cable to the pins of the three-pin plug. Connect the red lead to the ground terminal (B).

(2) Remove about 2 inches of the outside insulation at the other end of the cable. Fan out the three conductors and remove one-half inch of insulation from each conductor.

(3) Connect the leads to the power source as follows: (B) to ground lug; (A) and (C) to output terminals.

c. Fabricated Telephone Cable Assembly (fig. 3–21).

(1) Connect and solder two 12-inch No. 18 wires to one phone plug.

(2) Connect and solder the other end of the two wires to the corresponding terminals on the second phone plug.

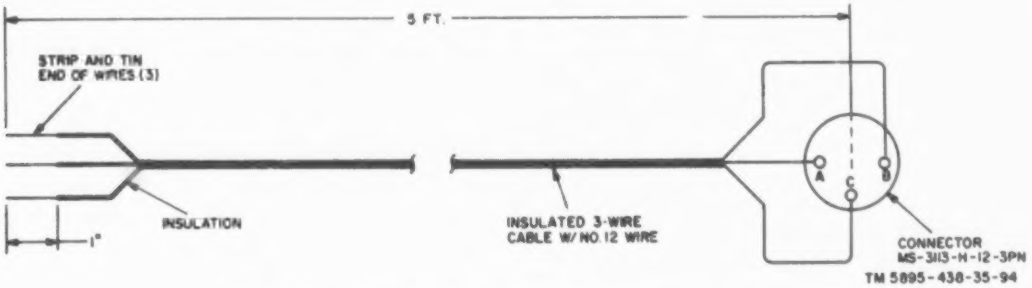

5 FT.
STRIP AND TIN END OF WIRES (3)
INSULATION
1"
INSULATED 3-WIRE CABLE W/ NO. 12 WIRE
A
C
B
CONNECTOR MS-3113-H-12-3PN
TM 5895-438-35-94

Figure 3–20. Power Supply Adapter Cable Fabrication diagram.

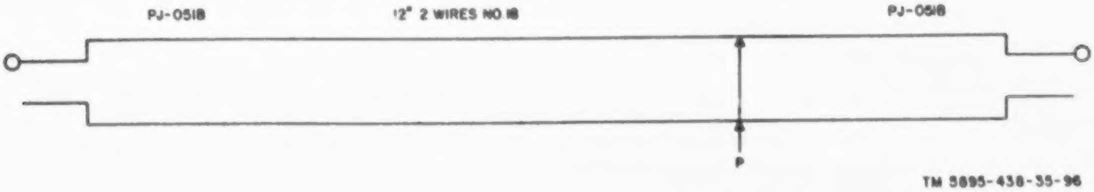
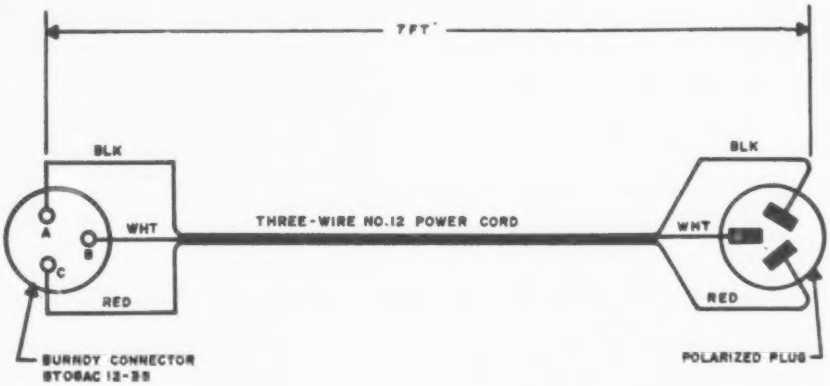


Figure 3–21. Telephone Cable Assembly, fabrication details.



TM5895-438-35-102

Figure 3-22. Power Supply Adapter Cable, fabrication details.

(3) Spot lace the two wires at 3- inch intervals.

d. Fabricated Power Supply Adapter Cable with Polarized Plug (fig. 3-22).

(1) Connect and solder a 7-foot length of three conductor power cable to the pins of the Burndy BT06AC 12-3S connector.

(2) Connect the white lead to pin B.

(3) Connect and solder the other end of the cable to the three-pin polarized plug; making sure the red lead is connected to pin B of the connector.

e. Fabrication of Power Supply Adapter Cable Assembly for Isolator Assembly, RF216/G (fig. 3-20). Fabricate this adapter cable in the manner described in *b* above, except substitute connector FW06-10SL-3S for connector MS-3113-H-12-3PN.

f. Fabrication of Adapter Cable Assemblies for Isolator Assembly, RF216/G (fig. 3-23).

(1) Cut six (6) lengths of No. 18 gauge insulated wire, 13 inches long.

(2) Strip off 1 inch of insulation from one end of each wire and tin.

(3) Connect and solder the other end of two of the wires to pins A and B of connector FW06-14S-2S.

(4) Connect and solder the other end of two different wires to pins A and B of connector MS 3116F8-4S.

(5) Connect and solder the other end of the remaining two wires to pins A and B of connector MS 3116F8-3S.

3-24. Modification Work Orders

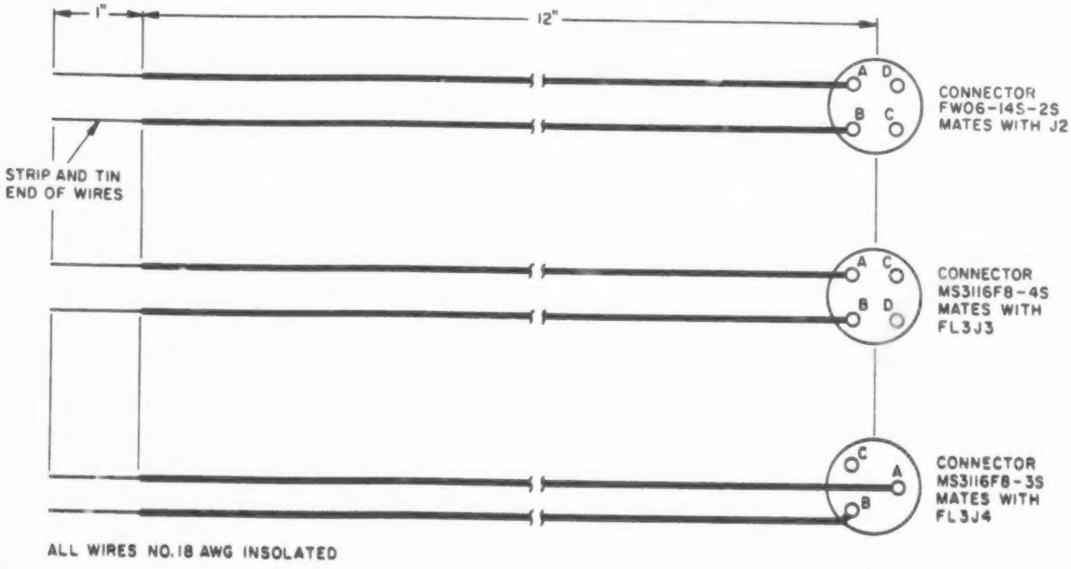
The performance standards listed in the test (para 3-25 through 3-30) assume that no modification work orders (MWO's) have been performed on the equipment. A listing of current modification work orders may be found in DA Pam 310-7. If a modification work order is performed on the equipment, allowance must be made for any test connections or test results that differ from those given in those test procedures.

3-25. Mechanical and Physical Inspection Test

a. Test Equipment and Materials. Mercury vapor lamp (with wide transmission filter).

b. Test Conditions. Perform the following procedure on the C-7050/G unit on which the general support tests are being conducted.

c. Procedure. The procedure for performing the mechanical and physical inspection test is given in table 3-3.


1"
12"
A
D
B
C
CONNECTOR
FW06-14S-2S
MATES WITH J2
STRIP AND TIN
END OF WIRES
A
C
B
D
CONNECTOR
MS3116F8-4S
MATES WITH
FL3J3
C
A
B
CONNECTOR
MS3116F8-3S
MATES WITH
FL3J4
ALL WIRES NO.18 AWG INSOLATED

TM5895-438-35-203

Figure 3-23. Isolator adapter cable assembly, fabrication details.

Table 3-2. Mechanical and Physical Inspection Test Procedures

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
1	N/A	Controls may be in any position.	*a.* Inspect all controls and mechanical assemblies for loose or missing screws, bolts, and nuts. *b.* Inspect all connectors, sockets, and receptacles for looseness and damage. *c.* Inspect chassis for damage, missing parts, and condition of finish and panel lettering. *Note.* Touchup painting is recommended in lieu of refinishing whenever practicable. Screwheads, receptacles, and plated fastener parts will not be painted or polished with abrasives.	*a.* Screws, bolts, and nuts are tight; none missing. *b.* No looseness or damage evident. *c.* No damage or missing parts evident. External surfaces intended to be painted do not show bare metal. Panel lettering legible.
2	N/A	Controls may be in any position.	*a.* Inspect interior printed circuit boards for burned, missing, or broken parts. *b.* Inspect solder connections of all parts and continuity of all printed circuit leads.	*a.* No damage or missing parts evident. *b.* All solder connections are clean and tight. Printed circuit leads are sound and show no breaks or shorts. No excess rosin on solder joints.

Table 3-3. Mechanical and Physical Inspection Test Procedures—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
			c. Inspect all cabling and wiring harnesses for damaged insulation, broken wires, kinks, and evidence of excessive wear or deterioration.	*c.* All cabling and wiring harnesses are properly secured. All insulation is sound. No broken, kinked, or damaged wires. All harnesses are properly laced.
			d. Inspect all wire leads connections to plugs and receptacles for faulty connections, insulating sleeve damage, and proper terminal connections if repair has been made.	*d.* All leads are properly insulated by sleeving at plug or receptacle pins; soldering to pins is clean; leads are connected to proper terminals.
			e. Inspect all markings on interior of chassis and on printed circuit board for legibility.	*e.* All lettering is legible.
3	Connect the mercury vapor lamp. Install wide transmission filter.	Controls may be in any position.	Turn on mercury vapor lamp and expose the portion of the equipment, that has been repaired or disturbed, to direct rays of lamp, while inspecting the condition of the moistureproofing and fungiproofing (MFP) varnish. *Note.* MFP varnish will appear blue-gray. There should be no MFP varnish on switch contacts or receptacle contacts.	All repaired or disturbed electrical components and chassis surfaces are covered. *Note.* Equipments that have had no MFP treatment do not require treatment during general support repair.
4	N/A	N/A	Check the equipment for applicable modification work orders. (See DA Pam 310-4 for list of MWO's.)	If MWO is performed. MWO number appears on equipment.

3-26. Control Indicator Panel Tests

a. Test Equipment and Materials.

(1) Power Supply PP-4571/G
(2) Multimeter, AN/USM-162
(3) Test leads
(4) Power supply adapter cable with polarized plug (para 3-23)
(5) Analyzer ZM-3/U

b. Test Connections and Conditions. Connect the equipment as shown in figure 3-24 and as directed in the test procedure.

c. Procedure. The procedure for performing the Control Indicator Panel tests is given in table 3-4.

***Caution:* Procedures given in table 3-4 require that continuity checks, using a multimeter, be made through closed relay contacts while the relay itself is energized; care must be exercised to insure that no potential is ever developed across the multimeter while using the resistance scale.**

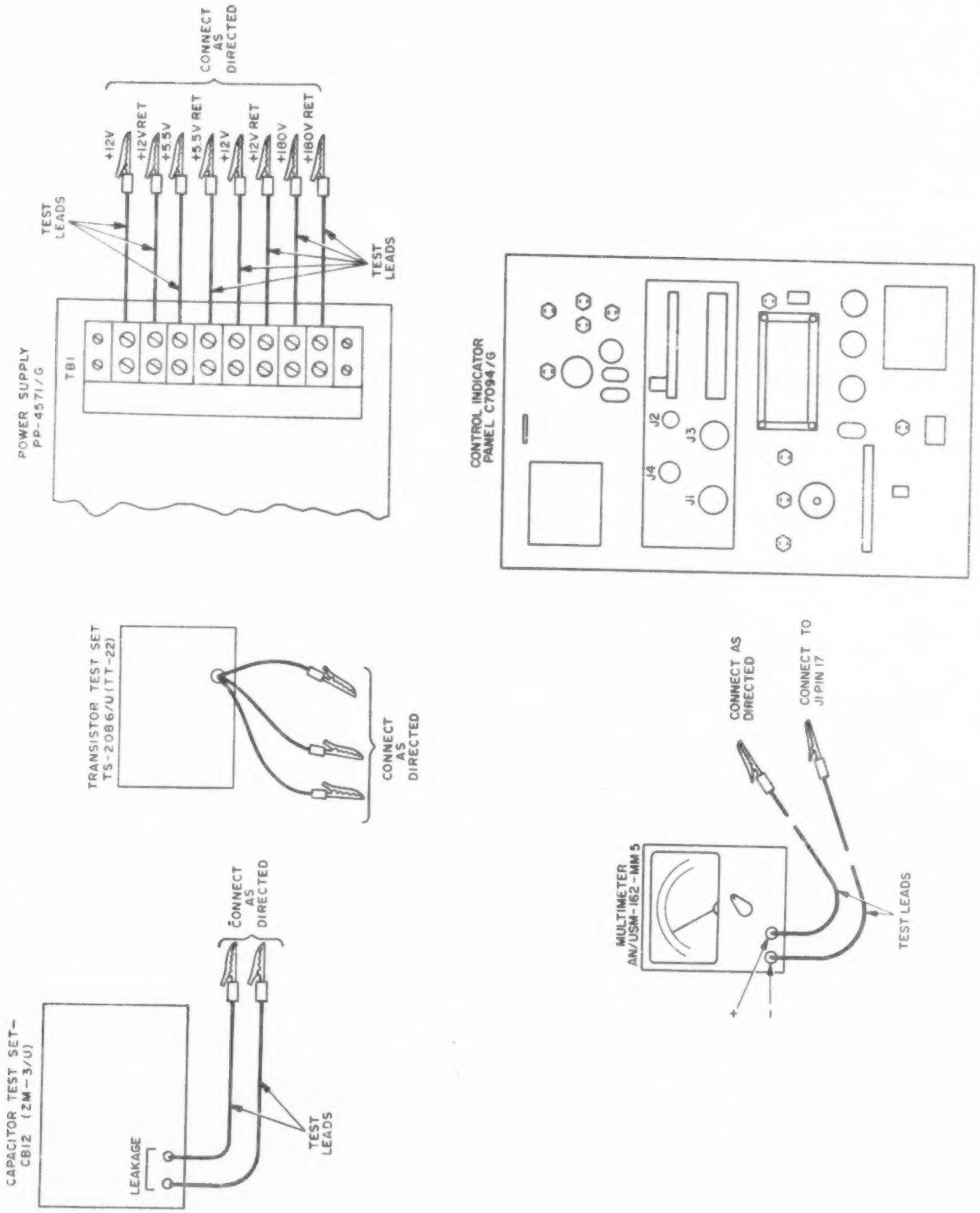

POWER SUPPLY
PP-4571/G
TB1
TEST LEADS
+12V
+12V RET
+5.5V
+5.5V RET
+12V
+12V RET
+180V
+180V RET
CONNECT AS DIRECTED
TEST LEADS
CONTROL INDICATOR
PANEL C7094/G
J1
J2
J3
J4
TRANSISTOR TEST SET
TS-2086/U(TT-22)
CONNECT AS DIRECTED
CAPACITOR TEST SET–
CB12 (ZM-3/U)
LEAKAGE
TEST LEADS
CONNECT AS DIRECTED
MULTIMETER
AN/USM-162-MM5
+
–
TEST LEADS
CONNECT AS DIRECTED
CONNECT TO J1 PIN 17
TM5895-348-35-93

Figure 3-24. Control Indicator Panel test setup.

Table 3-4. Control Indicator Panel Test Procedures

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
	Note. Prior to starting the checks, set the Control Indicator Controls as follows: *a.* TCU/CRYPTO switch to CRYPTO. *b.* XMIT/CANCEL switch off. *c.* STOP AT EOM/CONTINUE to CONTINUE. *d.* START XMIT switch off. *e.* UNITS, TENS, and HUNDREDS switches to 0. *f.* PRESET switch off. *g.* ON/OFF switch ON. *h.* ALARM TEST switch off.			
1	Setup multimeter to read a + dc voltage.		*a.* Apply +5.5 vdc TB3-6. *b.* Apply +5.5 vdc ground to TB3-5. *c.* Connect multimeter − lead to TB3-5. *d.* Connect multimeter + lead to J1-1.	Multimeter indicates +5.5v.
2			*a.* Apply +12 vdc to TB3-8. *b.* Apply −12 vdc to TB3-10. *c.* Apply + and −12 vdc grounds to TB3-9. Connect a test lead to TB3-9 and use this as a ground lead to ground points called out in procedure.	Multimeter indicates 0 vdc and lamp DS13 lights.
3			Disconnect multimeter + lead from J1-1 and connect it to J1-32.	Multimeter indicates 0 vdc.
4		Actuate and hold LAMP TEST switch.		*a.* Lamps DS9 thru DS14 light. *b.* Multimeter indicates +5 vdc.
5		Release LAMP TEST switch.	Apply ground to J1-2.	Lamp DS1 lights.
6			Remove ground from J1-2 and apply it to J1-3.	Lamp DS2 lights.
7			Remove ground from J1-3 and apply it to J1-4.	Lamp DS3 lights.
8			Remove ground from J1-4 and apply it to J1-5.	Lamp DS4 lights.
9			Remove ground from J1-5 and apply it to J1-6.	Lamp DS5 lights.
10			Remove ground from J1-6 and apply it to J1-7.	Lamp DS6 lights.
11			Remove ground from J1-7 and apply it to J1-8.	Lamp DS7 lights.
12			Remove ground from J1-8 and apply it to J1-9.	Lamp DS8 lights.
13			Remove ground from J1-9 and apply it to J1-14.	Lamp DS15 lights.
14			Remove ground from J1-14 and apply it to J1-18.	Lamp DS16 lights.
15	Setup multimeter to read resistance.	TCU/CRYPTO switch to TCU.	Disconnect multimeter + lead from J1-32 and connect it to J1-10.	*a.* Lamp DS9 lights. *b.* Multimeter indicates open circuit.

Table 3-4. Control Indicator Panel Test Procedures—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
16		TCU/CRYPTO switch to CRYPTO.		*a.* Lamp DS9 goes out. *b.* Multimeter indicates 100 ± 20 ohms.
17			Disconnect multimeter + lead from J1-32 and connect it to J3-61.	Multimeter indicates 100 ± 20 ohms.
18			Disconnect multimeter + lead from J3-61 and connect it to J1-17.	Multimeter indicates zero ohms.
19			Disconnect multimeter + lead from J1-17 and connect it to J1-16.	Multimeter indicates zero ohms.
20			Disconnect multimeter + lead from J1-16 and connect it to J1-12.	Multimeter indicates zero ohms.
21	Setup multimeter to read 5.5 volts DC.	Activate XMIT/CANCEL switch.	Disconnect multimeter + lead from J1-12 and connect it to J1-56.	Multimeter indicates +5.5 volts.
22		Set XMIT/CANCEL switch to off.		Multimeter indicates +0.0 v.
23			Disconnect multimeter + lead from J1-56 and connect it to J1-26.	Multimeter indicates +5.5 vdc.
24			Disconnect multimeter + lead from J1-26 and connect it to J1-23.	Multimeter indicates 0 vdc.
25	Setup multimeter to read resistance.			Multimeter indicates 100 ± 20 ohms.
26			Disconnect multimeter + lead from J1-23 and leave free.	
27		Set RECEIVE STOP AT EOM/CONTINUE switch to STOP AT EOM.	Connect multimeter + lead to J1-26.	*a.* Lamp DS14 lights. *b.* Multimeter indicates 100 ± 20 ohms.
28			Disconnect multimeter + lead from J1-26 and connect it to J1-29.	Multimeter indicates 100 ± 20 ohms.
29			Disconnect multimeter + lead from J1-29 and connect it to J1-30.	Multimeter indicates 100 ± 20 ohms.
30			Disconnect multimeter + lead from J1-30 and connect it to J1-31.	Multimeter indicates 100 ± 20 ohms.
31	Setup multimeter to read a + dc voltage.	*a.* Set REQUEST MES RT switch to on.		Multimeter indicates +5.5 vdc.
32		Set TRANSMIT STOP AT EOM switch to STOP AT EOM.	Connect voltmeter to J1-33	Meter reads +5.5 v.
33		Set START XMIT switch to on.	Connect voltmeter to J1-29	Meter KICKS upscale EACH TIME switch is OPERATED.

Table 3-4. Control Indicator Panel Test Procedures—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
34		Set MODE switch to TEST.	Disconnect multimeter + lead from J1-29 and connect it to J1-49.	*a.* Lamp DS10 lights. *b.* Multimeter indicates +5.5 vdc.
35		Set TCU/CRYPTO switch to TCU.	Disconnect multimeter + lead from J1-49 and connect it to J3-42.	Multimeter indicates +5 vdc.
36	Setup multimeter to read resistance.		Remove multimeter − lead from TB3-5 and + lead from J1-49. Use the two leads to perform the following continuity checks: *a.* J3-50 to J3-52. *b.* J3-37 to J4-10. *c.* J3-47 to J3-58.	Multimeter indicates zero ohms for *a*, *b*, and *c*.
37		Set MODE switch to NORMAL.	Check continuity between the following points: *a.* J3-47 to J3-58. *b.* J4-4 to J3-50. *c.* J4-8 to J3-52. *d.* J3-37 to J4-10.	Lamp DS11 lights. Multimeter indicates zero ohms for *a*, *b*, *c*, and *d*.
38	Setup multimeter to read a + dc voltage.		Measure between TB3-5 (−) and J3-42 (+) with the multimeter.	Multimeter indicates +5.5 vdc.
39			Disconnect multimeter + lead from J3-42.	
40	Setup multimeter to read resistance.	Set MODE switch to EMERGENCY.	Check continuity between the following points: *a.* J4-8 to J4-2. *b.* J4-10 to J4-4.	Lamp DS12 lights. Multimeter indicates zero ohms for *a* and *b*.
41			Measure between J4-8 and TB3-5 with the multimeter.	Multimeter indicates 6.8 K ± 680 ohms.
42		Set UNITS, TENS and HUNDREDS switches to 0. (MESSAGE NUMBER 000)	Check continuity between TB3-5 and the following points: *a.* J1-44. *b.* J1-43. *c.* J1-34. *d.* J1-33. *e.* J1-42. *f.* J1-41. *g.* J1-36. *h.* J1-35. *i.* J1-40. *j.* J1-39. *k.* J1-38. *l.* J1-37.	Multimeter indicates zero ohms at points *a* through *l*.
43		Set the UNITS, TENS, and HUNDREDS switches to 1.	Check continuity between TB3-5 and each pin listed in step 42.	Multimeter indicates open circuit at points *a*, *e*, and *i*. Multimeter indicates zero ohms at all other points.
44		Set the UNITS, TENS, and HUNDREDS switches to 2.	Check continuity between TB3-5 and each pin listed in step 42.	Multimeter indicates open circuit at points *b*, *f*, and *j*. Multimeter indicates zero ohms at all other points.

Table 3-4. Control Indicator Panel Test Procedures—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
45		Set the UNITS, TENS, and HUNDREDS switches to 3.	Check continuity between TB3-5 and each pin listed in step 42.	Multimeter indicates open circuit at points *a*, *b*, *e*, *f*, *i*, and *j*. Multimeter indicates zero ohms at all other points.
46		Set the UNITS, TENS, and HUNDREDS switches to 4	Check continuity between TB3-5 and each pin listed in step 42.	Multimeter indicates open circuit at points *c*, *g*, and *k*. Multimeter indicates zero ohms at all other points.
47		Set the UNITS, TENS, and HUNDREDS switches to 5.	Check continuity between TB3-5 and each pin listed in step 42.	Multimeter indicates open circuit at points *a*, *c*, *e*, *g*, *i*, and *k*. Multimeter indicates zero ohms at all other points.
48		Set the UNITS, TENS, and HUNDREDS switches to 6.	Check continuity between TB3-5 and each pin listed in step 42.	Multimeter indicates open circuit at points *b*, *c*, *f*, *g*, *j*, and *k*. Multimeter indicates zero ohms at all other points.
49		Set the UNITS, TENS, and HUNDREDS switches to 7.	Check continuity between TB3-5 and each pin listed in step 42.	Multimeter indicates open circuit at points *a*, *b*, *c*, *e*, *f*, *g*, *i*, *j*, and *k*. Multimeter indicates zero ohms at all other points.
50		Set the UNITS, TENS, and HUNDREDS switches to 8.	Check continuity between TB3-5 and each pin listed in step 42.	Multimeter indicates open circuit at points *d*, *h*, and *l*. Multimeter indicates zero ohms at all other points.
51		Set the UNITS, TENS, and HUNDREDS switches to 9.	Check continuity between TB3-5 and each pin listed in step 42.	Multimeter indicates open circuit at points *a*, *d*, *e*, *h*, *i*, and *l*. Multimeter indicates zero ohms at all other points.
52	Setup multimeter to read a + dc voltage.	Set the AUTO NO. ON/OFF switch to OFF.	Measure between TB3-5 (−) and J1-45 (+) with the multimeter.	*a.* Lamp DS17 lights. *b.* Multimeter indicates +5.5 vdc.
53		Set the PRESET switch to ON.	Measure between TB3-5 (—) and J1-46 (+) with the multimeter.	Multimeter indicates +5.5 vdc.
54			Remove multimeter leads from TCU.	
55	Setup multimeter to read resistance.	Set the AUTO. NO. ON/OFF switch to ON.	Measure between J1-45 and TB3-5.	Multimeter indicates 100 ± 10 ohms.
56		Set the PRESET switch to OFF.	Measure between J1-46 and TB3-5.	Multimeter indicates 100 ± 10 ohms.

Note. In steps 57 through 86 a total of four jumper wires will be connected from ground (TB2-5) and/or +5.5 vdc (TB3-6) to four pins on J3. four jumpers are mentioned in step 57; in the remaining steps only jumper connections that must be changed will be mentioned.

Step No.	Test equipment	Equipment under test	Test procedure	Performance standard
57	Connect the ground of the power supply 180 volt output (TB1-8) to TB3-5, connect the power supply 180 volt output (TB1-7) to J2-10.		Using four jumper wires, apply ground (from TB3-5) to the following pins of J3: pins 1, 4, 7, and 10.	HUNDREDS nixie tube indicates 0.
58			Remove ground from pin 1 and connect +5.5 vdc.	HUNDREDS nixie tube indicates 1.

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Table 3-4. Control Indicator Panel Test Procedures—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
59			Remove +5.5 vdc from pin 1 and apply ground. Remove ground from pin 4 and apply +5.5 vdc.	
60			Remove ground from pin 1 and apply +5.5 vdc.	HUNDREDS nixie tube indicates 3.
61			Remove +5.5 vdc from pins 1 and 4 and apply ground. Remove ground from pin 7 and apply +5.5 vdc.	HUNDREDS nixie tube indicates 4.
62			Remove ground from pin 1 and apply +5.5 vdc.	HUNDREDS nixie tube indicates 5.
63			Remove +5.5 vdc from pin 1 and connect ground. Remove ground from pin 4 and connect +5.5 vdc.	HUNDREDS nixie tube indicates 6.
64			Remove ground from pin 1 and connect +5.5 vdc.	HUNDREDS nixie tube indicates 7.
65			Remove +5.5 vdc from pins 1, 4, and 7. Remove ground from pin 10 and apply +5.5 vdc.	HUNDREDS nixie tube indicates 8.
66			Remove ground from pin 1 and apply +5.5 vdc.	HUNDREDS nixie tube indicates 9.
67			Remove jumper leads from J3 pins 1, 4, 7, and 10. Apply ground to pins 13, 16, 19, and 22.	TENS nixie tube indicates 0.
68			Remove ground from pin 13 and apply +5.5 vdc.	TENS nixie tube indicates 1.
69			Remove ground from pin 16 and apply +5 vdc. Remove +5.5 vdc from pin 13 and apply ground.	TENS nixie tube indicates 2.
70			Remove ground from pin 13 and apply +5.5 vdc.	TENS nixie tube indicates 3.
71			Remove +5.5 vdc from pin 13 and 16 and apply ground. Remove ground from pin 19 and apply +5 vdc.	TENS nixie tube indicates 4.
72			Remove ground from pin 13 and apply +5.5 vdc.	TENS nixie tube indicates 5.
73			Remove +5.5 vdc from pin 13 and apply ground. Remove ground from pin 16 and apply +5.5 vdc.	TENS nixie tube indicates 6
74			Remove ground from pin 13 and apply +5.5 vdc.	TENS nixie tube indicates 7.
75			Remove ground from pin 22 and apply +5.5 vdc. Remove +5.5 vdc from pins 13, 16, and 19 and apply ground.	TENS nixie tube indicates 8.
76			Remove ground from pin 13 and apply +5.5 vdc.	TENS nixie tube indicates 9.

Table 3-4. Control Indicator Panel Test Procedures—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
77	....	....	Remove jumper leads from pins 13, 16, 19, and 22. Apply ground to pins 25, 28, 31, 34.	UNITS nixie tube indicates 0.
78	....	....	Remove ground from pin 25 and apply +5.5 vdc.	UNITS nixie tube indicates 1.
79	....	....	Remove +5.5 vdc from pin 25 and apply ground. Remove ground from pin 28 and apply +5.5 vdc.	UNITS nixie tube indicates 2.
80	....	....	Remove ground from pin 25 and apply +5.5 vdc.	UNITS nixie tube indicates 3.
81	....	....	Remove +5.5 vdc from pins 25 and 28 and apply ground. Remove ground pin 31 and apply +5.5 vdc.	UNITS nixie tube indicates 4.
82	....	....	Remove ground from pin 25 and apply +5.5 vdc.	UNITS nixie tube indicates 5.
83	....	....	Remove +5.5 vdc from pin 25 and apply ground. Remove ground from pin 28 and apply +5.5 vdc.	UNITS nixie tube indicates 6.
84	....	....	Remove ground from pin 25 and apply +5.5 vdc.	UNITS nixie tube indicates 7.
85	....	....	Remove ground from pin 34 and apply +5.5 vdc. Remove +5.5 vdc from pins 25, 28 and 31 and apply ground.	UNITS nixie tube indicates 8.
86	....	....	Remove ground from pin 25 and apply +5.5 vdc.	UNITS nixie tube indicates 9.
87	....	....	Connect +12 vdc to J1-13. Vary the volume control.	Audible alarm output volume varies as VOLUME control is varied.
88	....	....	Remove +12 vdc from J1-13.	None.
89	....	Set the ALARM TEST switch to on.	....	Audible alarm sounds.
90	....	....	*a.* Remove all power supply inputs to the control-indicator panel. *b.* Remove all gnd straps from Control Panel to MAIN FRAME. Measure Resistance from each high side of C1 through C19.	Leakage is within specified limits given on the front panel of the capacitor analyzer.

Note. Return the control-indicator controls to their normal operating positions.

3-27. Power Supply and Filter Assembly PP-4571/G Tests

a. Test Equipment and Material (table 3-1).

(1) Fabricated 3-pin test cable assembly (para 3-23).
(2) Oscilloscope.
(3) Digital Voltmeter.
(4) Variable frequency power source.
(5) Test leads.
(6) Test loads.

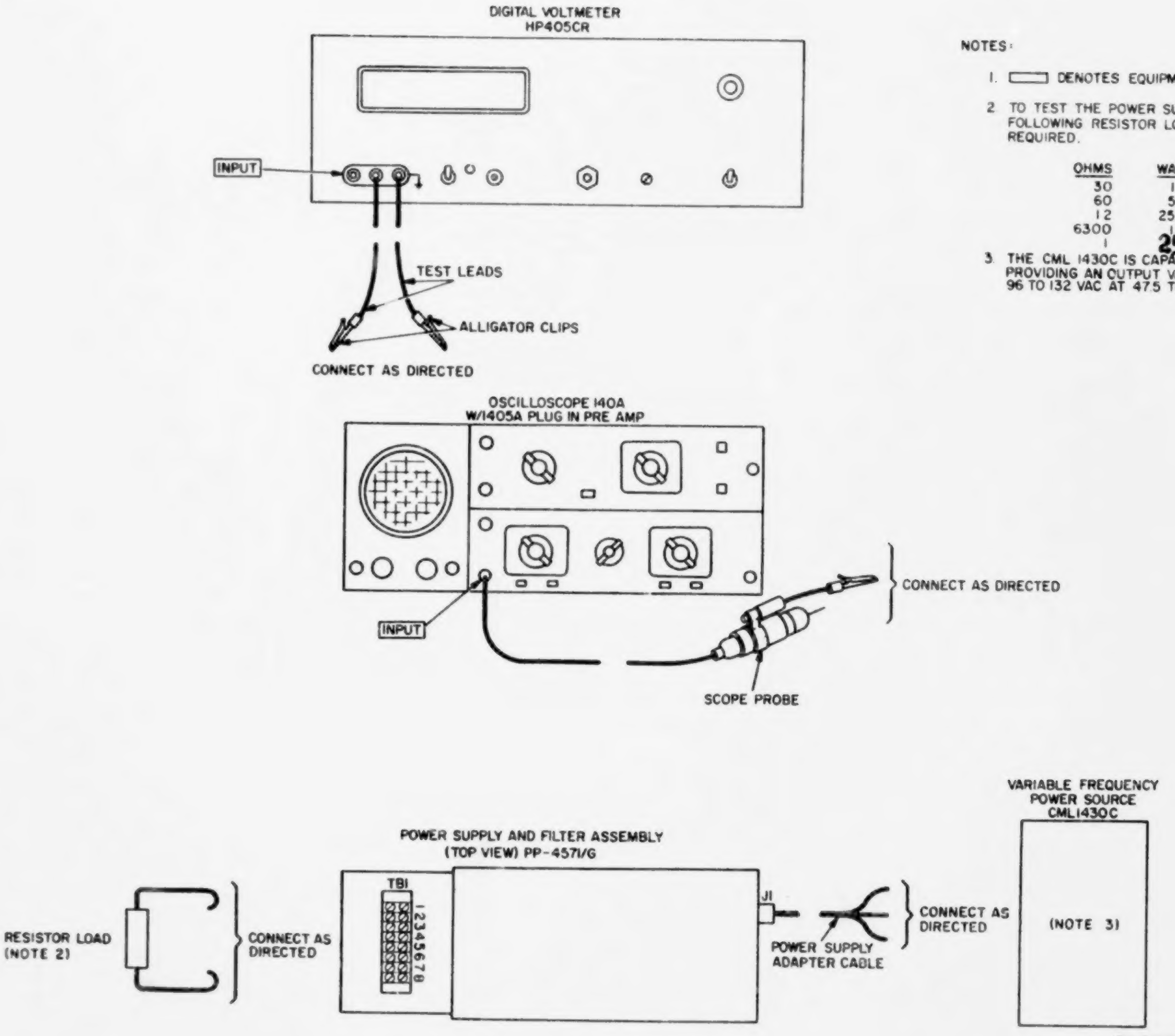
b. Test Connections and Conditions. Connect the equipment as shown in figure 3-25. Connect the three leads of the 3-pin fabricated cable assembly to the variable frequency power source (VFPS). Set the output controls of the power source to deliver a minimum voltage output and then turn the power source on.

Note. The PP-4571/G can be strapped for either 120 vac or 220 vac, 60 cycle operation. Prior to testing determine what mode of operation the power supply is strapped for (refer to TM 11-5815-335-12 para 2-12). If the power supply is strapped for 230 vac operation, restrap it for 120 vac operation for this test.

c. Procedure. The procedure for performing the power supply tests is given in table 3-5.

Table 3-5. Power Supply Test Procedures

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
1	Set up the variable frequency power source to deliver a 60 cycle 120 vac output.	Set the A/C POWER ON/OFF switch to ON.	Connect + probe of digital voltmeter (DVM) to TB1-3. Connect — probe to TB 1-4.	DVM indicates approximately +4.5 vdc.
2	....	....	Turn the 5.5V potentiometer from fully clockwise (CW) to fully counterclockwise (CCW) and note the voltmeter reading. Leave voltage at 4.5V.	The voltage variation is at least 2.4 volts with 4.5 volts as nominal.
3	....	....	*a.* Connect the DVM to TB1-5(+) and TB 1-6(−). *b.* Turn the +12V potentiometer from fully clockwise (CW) to fully counterclockwise (CCW) and note DVM reading. Leave voltage at 12.0V.	The voltage variation is at least 2 volts with 12.0V as nominal.
4	....	....	*a.* Connect the DVM to TB1-1(−) and TB1-2(+). *b.* Turn the −12V potentiometer from fully clockwise (CW) to fully counterclockwise (CCW) and note reading. Leave voltage at 12.0.	The voltage variation is at least 2 volts with 12.0V as nominal.
5	....	....	Connect DVM to TB1-7(+) and TB1-8(−).	DVM indicates 180 vdc ±10 volts.
6	Test load	....	*a.* Connect a 1-ohm, 25 watt load resistor between TB1-3 and TB1-4. *b.* Connect the DVM to TB1-3(+) and TB1-4(−). *c.* Adjust 5.5V potentiometer for a 4.50 vdc reading on the DVM.	DVM indicates +4.50 vdc ±0.1V.
7	Setup the VFPS to deliver a 63 cycle, 96 vac output.	....	Read DVM	DVM indicates 4.50 vdc ±0.055 volt.


DIGITAL VOLTMETER
HP405CR
INPUT
TEST LEADS
ALLIGATOR CLIPS
CONNECT AS DIRECTED
OSCILLOSCOPE 140A
W/1405A PLUG IN PRE AMP
INPUT
CONNECT AS DIRECTED
SCOPE PROBE
RESISTOR LOAD
(NOTE 2)
CONNECT AS DIRECTED
POWER SUPPLY AND FILTER ASSEMBLY
(TOP VIEW) PP-4571/G
TB1
12345678
J1
POWER SUPPLY ADAPTER CABLE
CONNECT AS DIRECTED
VARIABLE FREQUENCY
POWER SOURCE
CML1430C
(NOTE 3)
TM 5895-438-35-91

NOTES:

1. ▭ DENOTES EQUIPMENT MARKING.
2. TO TEST THE POWER SUPPLY THE FOLLOWING RESISTOR LOADS ARE REQUIRED.

OHMS	WATTS
30	10
60	5.0
12	25.0
6300	1.0
1	25

3. THE CML 1430C IS CAPABLE OF PROVIDING AN OUTPUT VARIABLE FROM 96 TO 132 VAC AT 47.5 TO 63 CPS.

Figure 3-25. Power Supply and Filter Assembly PP-4571/G test setup.

Table 3-5. Power Supply Test Procedures—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
8	Setup the VFPS to deliver a 47.5 cycle, 132 vac output.		Read DVM	DVM indicates 4.50 vdc ±0.055 volts.
9	Setup the VFPS to deliver. a 63 cycle, 132 vac output.		Read DVM	DVM indicates 4.50 vdc ±0.055 volt.
10			Remove the 1 ohm, 25-watt load resistor from TB1-3 and TB1-4 and repeat steps 7, 8, and 9.	In each case DVM indicates 4.50 vdc ±0.055 volt.
11	Setup VFPS to deliver a 60 cycle, 120 vac output.		*a.* Connect a 12 ohm, 25 watt load resistor between TB1-5 and TB1-6.	
			b. Connect the DVM to TB1-5(+) and TB1-6(−).	DVM indicates approximately 12.00 vdc.
			c. Adjust +12V potentiometer until the DVM indicates 12.00 vdc.	DVM indicates 12.00 vdc.
12	Setup the VFPS to deliver a 47.5 cycle, 96 vac output.		Read DVM	DVM indicates 12.00 vdc ±0.3 vdc.
13	Set up the VFPS to deliver a 63 cycle, 96 vac output.		Read DVM	DVM indicates 12±0.3 volts.
14	Set up the VFPS to deliver a 47.5 cycle, 132 vac output.		Read DVM	DVM indicates 12±0.3 volts.
15	Setup the VFPS to deliver a 63 cycle, 132 vac output.		Read DVM	DVM indicates 12±0.3 volts.
16			*a.* Remove 12 ohm load from TB1-5 and TB1-6 and repeat steps 12 through 15.	DVM indicates 12±0.3 volts.
17	Set up the VFPS to deliver a 60 cycle, 120 vac output.		*a.* Connect a 60 ohm 5 watt load resistor between TB1-1 and TB1-2.	DVM indicates −12.00 vdc (a, b, and c).
			b. Connect the DVM to TB1-1(−) and TB1-2(+).	
			c. Adjust −12v potentiometer for a −12.00 vdc reading on the DVM.	
18	Set up the VFPS to deliver a 47.5 cycle, 96 vac output.		Read DVM	DVM indicates 12±0.3 volts.
19	Set up the VFPS to deliver a 63 cycle, 96 vac output.		Read DVM	DVM indicates 12±0.3 volts.
20	Set up the VFPS to deliver a 47.5 cycle, 132 vac output.		Read DVM	DVM indicates 12±0.3 volts.
21	Set up the VFPS to deliver a 63 cycle, 132 vac output.		Read DVM	DVM indicates 12±0.3 volts.
22			*a.* Remove the 60 ohm load from TB1-1 and TB1-2 and repeat steps 18 through 21.	DVM indicates 12±0.3 volts.

Table 3-5. Power Supply Test Procedures—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
23	Set up the VFPS 1430C to to deliver a 60 cycle, 120 vac output.		*a.* Connect a 6300 ohm, 10 watt load between TB1-7 and TB1-8. *b.* Connect the DVM to TB1-7 (+) and TB1-8(−).	DVM indicates 180V ± 10 volts.
24	Set up the VFPS to deliver a 47.5 cycle, 96 vac output.		Read DVM	DVM indicates 180V ± 10 volts.
25	Set up the VFPS 1430C to deliver a 63 cycle, 96 vac output.		Read DVM	DVM indicates 180V ± 10 volts.
26	Set up the VFPS to deliver a 47.5 cycle, 132 vac output.		Read DVM	DVM indicates 180 ± 10 volts.
27	Set up the VFPS to deliver a 63 cycle, 132 vac output.		Read DVM	DVM indicates 180 ± 10 volts.
28			Remove 6300 ohm load from TB1-7 and TB1-8 and repeat steps 23 through 26.	DVM indicates 180 ± 10 volts.
29	*a.* Set up the VFPS to deliver a 60 cycle, 120 vac output. *b.* Set the oscilloscope controls as follows: (1) TIME/CM to 10 ms. (2) SWEEP to MAIN (3) MAIN SWEEP TRIGGER to LINE. (4) FUNCTION to A. (5) CHANNEL A VERNIER SENSITIVITY fully clockwise. (6) COUPLING to AC.		*a.* Connect a 12 ohm, 25 watt load between TB1-3 and TB1-4. *b.* Connect scope probe to TB1-3 and probe ground lead to TB1-4. *c.* Measure ripple and noise	Ripple and noise less than 50 mv peak to peak.
30	Same conditions specified in step 28 except set the CHANNEL A VERNIER SENSITIVITY to .1.		*a.* Remove the scope probe, ground lead, and load from TB1-3 and TB1-4. *b.* Connect a 12 ohm, 25 watt load between TB1-5 and TB1-6. *c.* Connect scope probe to TB1-5 and probe ground lead to TB1-6. *d.* Measure ripple and noise	Ripple and noise less than 200 mv peak to peak.

Table 3-5. Power Supply Test Procedures—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
31			*a.* Remove the scope probe, ground lead, and load from TB1-5 and TB1-6. *b.* Connect a 60 ohm, 5 watt load between TB1-1 and TB1-2. *c.* Connect the scope probe to TB1-1 and probe ground lead to TB1-2. *d.* Measure ripple and noise	Ripple and noise less than 200 mv peak to peak.
32	Same conditions specified in step 28 except set the CHANNEL A VERNIER SENSITIVITY to 2.		*a.* Remove the scope probe, ground lead, and load from TB1-1 and TB1-2. *b.* Connect a 6300 ohm, 10 watt load between TB1-7 and TB1-8. *c.* Connect the scope probe to TB1-7 and probe ground lead to TB1-8. *d.* Measure ripple and noise **e. Remove the scope, probe, ground lead, and load from TB1-7 and TB1-8.**	Ripple and noise less than 7.2 volts peak to peak.

3-28. Simulation Test Unit Tests.

a. Test Equipment and Materials.

(1) Power Supply and Filter Assembly PP-4571/G.
(2) Multimeter AN/USM-162.
(3) Test leads.
(4) Fabricated telephone cable assembly (para 3-23).
(5) Analyzer, ZM-3/U.

b. Test Connections and Conditions. Connect the equipment as shown in figure 3-26 and directed in the test procedure.

c. Procedure. The procedure for performing the Simulation Test Unit tests is given in table 3-6.

Table 3-6. Simulation Test Unit Test Procedures

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
1			Connect +12 vdc to J3-3. Connect +5.5 vdc to J3-4. Connect +5 vdc and +12 vdc grounds to J3-5. Attach one end of a test lead to J3-5. Use this ground lead whenever it is necessary to ground a point on the simulator panel.	
2			Ground J1-1	Lamp DS1 lights.
3			Ground J1-2	Lamp DS3 lights.

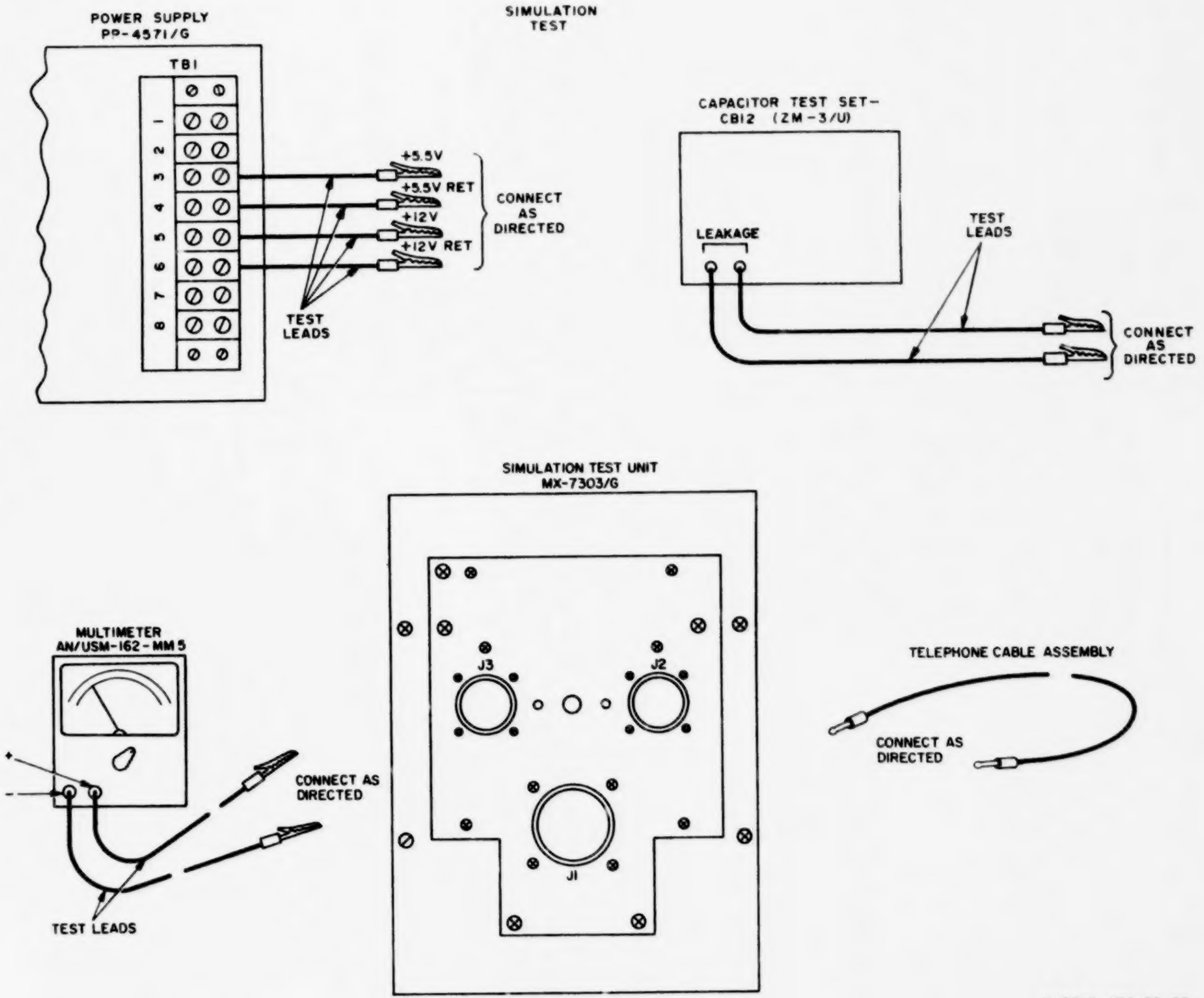

POWER SUPPLY
PP-4571/G
TB1
1
2
3
4
5
6
7
8
+5.5V
+5.5V RET
+12V
+12V RET
CONNECT AS DIRECTED
TEST LEADS
SIMULATION TEST
CAPACITOR TEST SET-CB12 (ZM-3/U)
LEAKAGE
TEST LEADS
CONNECT AS DIRECTED
SIMULATION TEST UNIT
MX-7303/G
J3
J2
J1
MULTIMETER
AN/USM-162-MM5
+
-
CONNECT AS DIRECTED
TEST LEADS
TELEPHONE CABLE ASSEMBLY
CONNECT AS DIRECTED
TM5895-438-35-92

Figure 3-26. Simulation Test Unit test setup.

Table 3-6. Simulation Test Unit Test Procedures—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
4			Ground J1-3.	Lamp DS2 lights.
5			Ground J1-4.	Lamp DS5 lights.
6			Ground J1-5.	Lamp DS4 lights.
7	Set up the multimeter to read a + dc voltage.	Set the RT ENABLE/DISABLE switch to ENABLE.	With the multimeter measure in turn between J3-5(−) and J1-6, 7, and 9(+).	Multimeter indicates zero volts.
8			With the multimeter measure between J3-5(−) and J1-8(+).	Multimeter indicates +5.5 vdc.
9		Set the RT ENABLE/DISABLE switch to DISABLE. Set the SYS CLR switch to on.	*a.* Measure between J3-5(−) and J1-10(+). *b.* Measure between J3-5(−) and J1-7(+).	Multimeter indicates +5.5 vdc.
10			Measure between J3-5(−) and J1-8(+). Measure between J3-5(−) and J1-9(+).	Multimeter indicates zero volts.
11		Actuate the LAMP TEST switch to on.	Measure between J3-5(−) and J1-6(+).	Multimeter indicates +5.5 vdc.
12	Set up multimeter to read resistance.	Set the LAMP TEST switch to off. Set the RT ENABLE/DISABLE switch to ENABLE. Set the SYS CLR switch to off.	With the multimeter measure between J-11 and J1-35.	Multimeter indicates zero resistance.
13			*a.* Measure between J1-9 and J1-10. *b.* Measure between J1-11 and J1-7. *c.* Measure between J1-11 and J1-6.	Multimeter indicates 100 ± 10 ohms.
14		Set the RT ENABLE/DISABLE switch to DISABLE.	With the multimeter measure between J1-11 and J1-8.	Multimeter indicates 100 ± 10 ohms.
15	Set up the capacitor analyzer to measure leakage.		Connect the capacitor analyzer leads between J1-11 and J1-10.	Leakage of C4 is within tolerance indicated on capacitor analyzer.
16		Set the RT ENABLE/DISABLE switch to ENABLE.	*a.* Remove the +5 vdc input from J3-4, and the +12 vdc input from J3-3. *b.* Connect the capacitor analyzer leads between J1-11 and J1-8.	Leakage of C3 is within tolerance indicated on capacitor analyzer.

Table 3-6. Simulation Test Unit Test Procedures—Continued

Step No.	Control Settings		Test Procedure	Performance Standard
	Test Equipment	Equipment Under Test		
17	....	Set the RT ENABLE/DISABLE switch to DISABLE.	Connect the capacitor analyzer leads between J1-11 and J1-7.	Leakage of C2 is within tolerance indicated on capacitor analyzer.
18	....	....	Connect the capacitor analyzer leads between J1-11 and J1-6.	Leakage of C1 is within tolerance indicated on capacitor analyzer.
19	....	....	*a.* Connect one plug of the telephone cable into J5 (SEND LINE) and the other plug into J4 (RECEIVE LINE).	
			b. Using the multimeter measure the resistance between J2-1 and J2-4.	Multimeter reads approx. 240 ohms.
			c. Measure the resistance between J2-3 and J2-6.	Multimeter reads zero ohms.
20	....	Set the SPEED SEL switch to 45.45.	Measure resistance between J1-34 and J1-28 through J1-33.	Resistance should be as follows: *Check* — *Resistance* (1) J1-34 to J1-28 — (1) zero (2) J1-34 to J1-29 — (2) open circuit (3) J1-34 to J1-30 — (3) open circuit (4) J1-34 to J1-31 — (4) zero (5) J1-34 to J1-32 — (5) open circuit (6) J1-34 to J1-33 — (6) open circuit
21	....	Set the SPEED SEL switch to 74.2	Measure resistance between J1-34 and J1-28 through J1-33.	Resistance should be as follows: *Check* — *Resistance* (1) J1-34 to J1-28 — (1) open circuit (2) J1-34 to J1-29 — (2) zero (3) J1-34 to J1-30 — (3) open circuit (4) J1-34 to J1-31 — (4) open circuit (5) J1-34 to J1-32 — (5) zero (6) J1-34 to J1-33 — (6) open circuit
22	....	Set the SPEED SEL switch to 75.	Measure resistance between J1-34 and J1-28 through J1-33.	Resistance should be as follows: *Check* — *Resistance* (1) J1-34 to J1-28 — (1) open circuit (2) J1-34 to J1-29 — (2) open circuit (3) J1-34 to J1-30 — (3) zero (4) J1-34 to J1-31 — (4) open circuit (5) J1-34 to J1-32 — (5) open circuit (6) J1-34 to J1-33 — (6) zero
23	....	Set the XMIT and RECEIVE switches to OFF.	Connect one lead of the multimeter to J1-11. Use the other lead of the multimeter to check continuity between J1-11 and J1-12 through J1-27.	The multimeter indicates zero ohms at pins 13 through 16, pins 24 through 27. All other pins indicate an open circuit.
24	....	Set the XMIT and RECEIVE switches to ACK-1.	Check continuity between J1-11 and J1-12 through J1-27.	The multimeter indicates zero ohms at pins 14 and 15 and 24 through 27. All other pins indicate an open circuit.

Table 3-6. Simulation Test Unit Test Procedures—Continued

Step No.	Control Settings		Test Procedure	Performance Standard
	Test Equipment	Equipment Under Test		
25	----------------	----------------	*a.* Check continuity between J1-16 and J1-17. *b.* Check continuity between J1-12 and J1-13.	The multimeter indicates zero ohms.
26	----------------	Set the XMIT and RECEIVE switches to ACK-2.	Check continuity between J1-11 and J1-12 through J1-27.	The multimeter indicates zero ohms at pins 13, 15, and 24 through 27. All other pins indicate an open circuit.
27	----------------	----------------	*a.* Check continuity between J1-16 and J1-18. *b.* Check continuity between J1-12 and J1-14.	The multimeter indicates zero ohms.
28	----------------	Set the XMIT and RECEIVE switches to STOP.	Check continuity between J1-11 and J1-12 through J1-27.	The multimeter indicates zero ohms at pins 13, 14 and 24 through 27. All other pins indicate an open circuit.
29	----------------	----------------	*a.* Check continuity between J1-12 and J1-15. *b.* Check continuity between J1-16 and J1-19.	The multimeter indicates zero ohms.
30	----------------	Set the XMIT and RECEIVE switches to REP.	Check continuity between J1-11 and J1-12 through J1-27.	The multimeter indicates zero ohms at pins 13, 14, 15, 25, 26 and 27. All other pins indicate an open circuit.
31	----------------	----------------	*a.* Check continuity between J1-16 and J1-20. *b.* Check continuity between J1-12 and J1-24.	The multimeter indicates zero ohms.
32	----------------	Set the XMIT and RECEIVE switches to RT.	Check continuity between J1-11 and J1-12 through J1-27.	The multimeter indicates zero ohms at pins 13, 14, 15, 24, 26, and 27. All other pins indicate an open circuit.
33	----------------	----------------	*a.* Check continuity between J1-16 and J1-21. *b.* Check continuity between J1-12 and J1-25.	The multimeter indicates zero ohms.
34	----------------	Set the XMIT and RECEIVE switches to CANCEL.	Check continuity between J1-11 and J1-12 through J1-27.	The multimeter indicates zero ohms at pins 13, 14, 15, 24, 25 and 27. All other pins indicate an open circuit.
35	----------------	----------------	*a.* Check continuity between J1-16 and J1-22. *b.* Check continuity between J1-12 and J1-26.	The multimeter indicates zero ohms.
36	----------------	Set the XMIT and RECEIVE switches to START.	Check continuity between J1-11 and J1-12 through J1-27.	The multimeter indicates zero ohms at pins 13, 14, 15, 24, 25 and 26. All other pins indicate an open circuit.
37	----------------	----------------	*a.* Check continuity between J1-16 and J1-23. *b.* Check continuity between J1-12 and J1-27.	The multimeter indicates zero ohms.

3–29. T-R Filter Tests

a. Test Equipment and Materials (table 3–1).

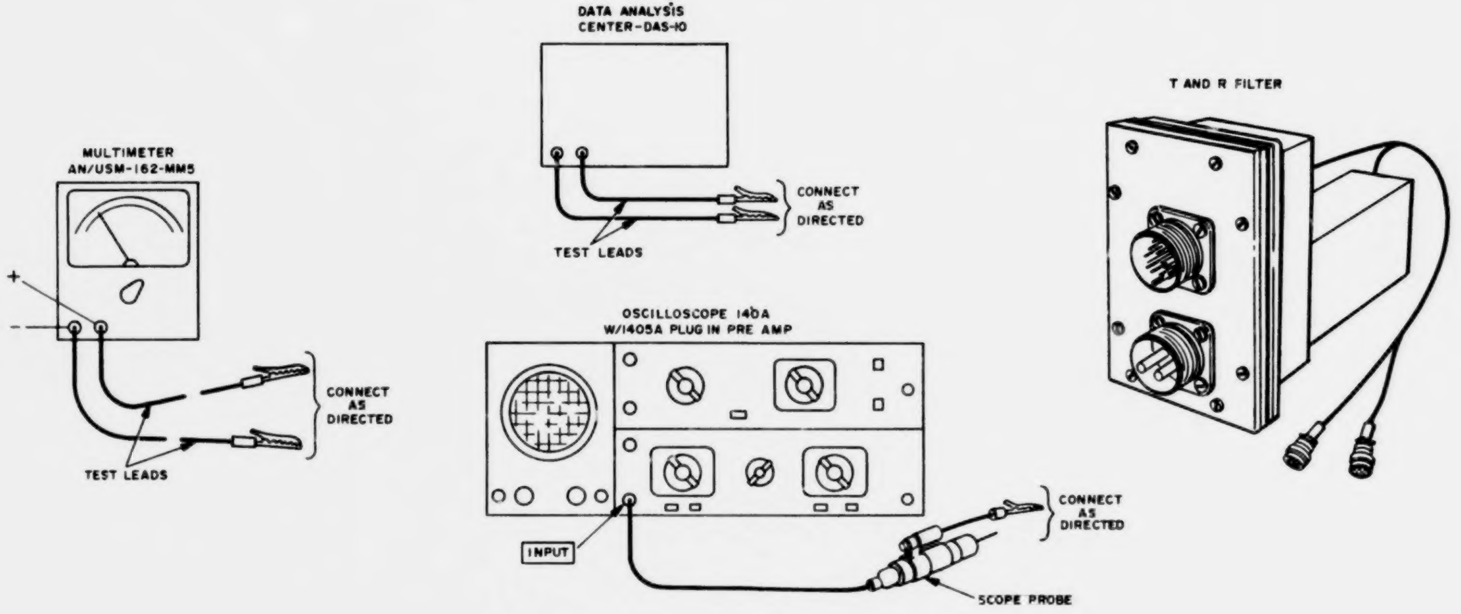
(1) Oscilloscope.
(2) Multimeter AN/USM–162.
(3) Data Analysis Center—DAS–10.

b. Connect the equipment as shown in figure 3–27 and directed in the test procedure.

c. Procedure. The procedure for performing the T-R filter tests is given in table 3–7.

Table 3–7. T-R Filter Test Procedures

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
1	Setup the multimeter to read resistance.		Measure between the following points with the multimeter. J1–Y to P1–10. J1–Z to P1–11. J1–W to P1–19. J1–X to P1–20. J1–R to P1–9. J1–S to P1–23. J1–M to P1–13. J1–K to P1–14. J1–L to P1–15. J1–E to TB1–1. J1–F to TB1–3. J1–G to TB1–4. J1–N to TB1–9. J1–P to TB1–11. J1–Q to TB1–12. J1–T to TB1–8. J1–U to TB1–5. J1–V to TB1–7. J1–A to P1–8. J1–C to P1–7. J1–B to P1–9. J1–B to P2–3. J1–A to P2–1. P1–25 to P2–4. P1–26 to P2–6. P1–27 to P2–5. J2–A to violet ground lead. J2–B to violet and white ground lead.	Multimeter indicates zero ohms for all checks.
2	*a.* Setup the data analysis center to deliver an RY output.		*a.* Connect the 6v Polar low impedance output of the data analysis center to J1–E and J1–F.	The output pulse train has the same bit pattern (RY) as that delivered by the data analysis center.
	b. Setup the oscilloscope to display a 12 volt input signal.		*b.* Connect the oscilloscope probe to P1–4 and the probe's ground lead to P1–5.	
3			*a.* Disconnect the two leads from J1–E and J1–F and connect them to J1–U and J1–V.	


MULTIMETER
AN/USM-162-MM5
+
-
TEST LEADS
CONNECT AS DIRECTED
DATA ANALYSIS CENTER-DAS-10
TEST LEADS
CONNECT AS DIRECTED
OSCILLOSCOPE 140A
W/1405A PLUG IN PRE AMP
INPUT
SCOPE PROBE
CONNECT AS DIRECTED
T AND R FILTER

TM5895-438-35-103

Figure 3-27. T-R Filter test setup.

Table 3-7. T-R Filler Test Procedures—Continued

Step No.	Control settings		Test Procedure	Performance Standard
	Test equipment	Equipment Under Test		
			b. Disconnect the oscilloscope probe from P1-4 and connect it to P1-1. Disconnect the probe's ground lead from P1-5 and connect it to P1-2.	The output pulse train has the same bit pattern (RY) as that delivered by the data analysis center.
4			*a.* Disconnect the two leads from J1-U and J1-V and connect them to J1-N and J1-P.	
			b. Disconnect the oscilloscope probe from P1-1 and connect it to P1-16. Disconnect the probe's ground lead from P1-2 and connect it to P1-17.	Same as above.

3-30. Isolator Assembly RE-216/G Tests

a. Test equipment and materials (table 3-1).

(1) Power Supply and Filter Assembly PP-4571/G.

(2) Digital voltmeter (DVM).

(3) Power supply.

(4) Multimeter AN/USM-162.

(5) Variable frequency power source (VFPS).

(6) Fabricated power supply adapter cable assembly for isolator assembly (para 3-22).

(7) Fabricated adapter cable assemblies for isolator assembly (para 3-20).

b. Connect the equipment as shown in figure 3-28 and directed in the test procedure.

c. Procedure. The procedure for performing the isolator assembly tests is given in table 3-8.

Table 3-8. Isolator Assembly RE216/G Testing Procedures

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
	Note. Do not apply A.C. power, except as directed in procedure.			
1	Set up the VFPS to deliver a 60 cycle 120V A.C. output power ON/OFF switch to OFF initially.	Power supply	*a.* Connect + probe of DVM to terminal 1 of TB1. *b.* Connect − probe of DVM to TB1-2. *c.* Apply 120V A.C. to the isolator assembly. *d.* Place S1 in the ON position.	*a.* None. *b.* None. *c.* None. *d.* 6.1 volts ±0.3V.
2	Set up the VFPS to deliver a 47.5 cycle, 96V A.C. output.		Read DVM	6.1 Volts ±0.3V.
3	Set up the VFPS to deliver a 63 cycle, 96V A.C. output.		Read DVM	6.1 Volts ±0.3V.
4	Set up the VFPS to deliver a 47.5 cycle, 132V A.C. output.		Read DVM	6.1 Volts ±0.3V.

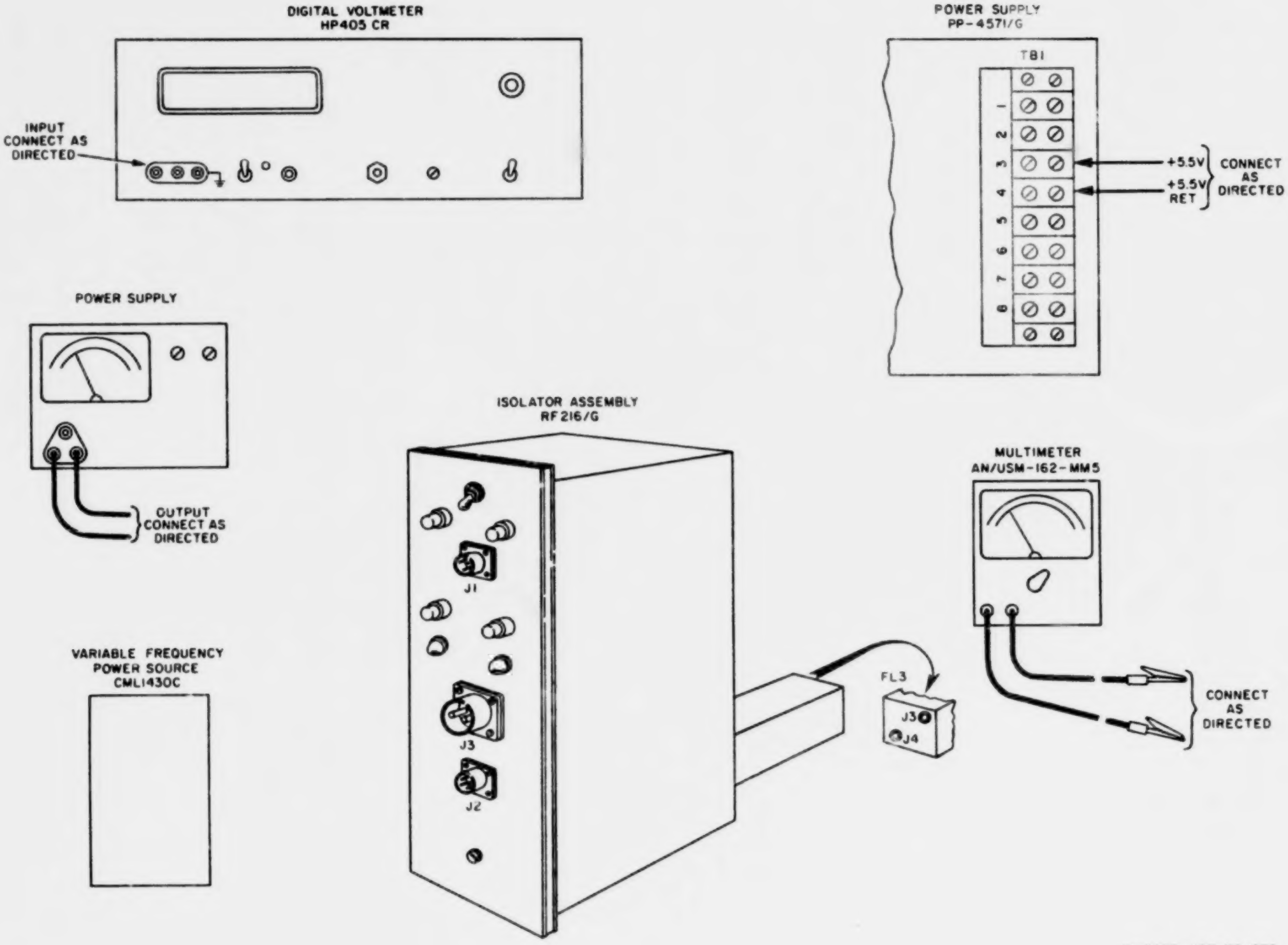

DIGITAL VOLTMETER
HP405 CR
INPUT CONNECT AS DIRECTED
POWER SUPPLY
PP-4571/G
TB1
1
2
3
4
5
6
7
8
+5.5V
+5.5V RET
CONNECT AS DIRECTED
POWER SUPPLY
OUTPUT CONNECT AS DIRECTED
ISOLATOR ASSEMBLY
RF216/G
J1
J3
J2
FL3
J3
J4
MULTIMETER
AN/USM-162-MM5
CONNECT AS DIRECTED
VARIABLE FREQUENCY POWER SOURCE
CML1430C
TM5895-438-35-202

Figure 3-28. Isolator assembly test setup.

Table 3-8. Isolator Assembly RE216/G Testing Procedures—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
5	Set up the VFPS to deliver a 63 cycle, 132V A.C. output.		Read DVM	6.1 Volts ±0.3V.
6	Set up the VFPS to deliver a 60 cycle 120V A.C. output. Place power ON/OFF switch to OFF.		*a.* Connect + probe of DVM to TB1-2. *b.* Connect − probe of DVM to TB1-3. *c.* Apply A.C. power to the Isolator Ass.	*a.* None. *b.* *c.* 6.1 Volts ±0.3V.
7	Same as step 2		Read DVM	6.1 Volts ±0.3V.
8	Same as step 3		Read DVM	6.1 Volts ±0.3V.
9	Same as step 4		Read DVM	6.1 Volts ±0.3V.
10	Same as step 5		Read DVM	6.1 Volts ±0.3V.
11	Remove A.C. Power from the isolator assembly.		Connect PS1 for 230V A.C. operation.	None.
12	Set up the VFPS to deliver 230V A.C. 60 cycle output. Power ON/OFF switch to OFF.		*a.* Connect + probe of DVM to terminal 1 of TB1. *b.* Connect − probe of DVM to TB1-2.	*a.* None. *b.* None.
13	Set up the VFPS to deliver 207V A.C. 47.5 cycles.		Read DVM	6.1 Volts ±0.3V.
14	Set up the VFPS to deliver 207V A.C. 63 cycles.		Read DVM	6.1 Volts ±0.3V.
15	Set up the VFPS to deliver 253V A.C. 47.5 cycles.		Read DVM	6.1 Volts ±0.3V.
16	Set up the VFPS to deliver 253V A.C. 63 cycles.		Read DVM	6.1 Volts ±0.3V.
17	Set up the VFPS to deliver 230V A.C. 60 cycles. Place power ON/OFF switch to OFF.		*a.* Connect + probe of DVM to TB1-2. *b.* Connect − probe of DVM to TB1-3. *c.* Apply A.C. Power to Isolator Assembly.	*a.* None. *b.* None. *c.* 6.1 Volts ±0.3 volt.
18	Same as step 13		Read DVM	6.1 volts ±0.3 volt.
19	Same as step 14		Read DVM	6.1 volts ±0.3 volt.
20	Same as step 15		Read DVM	6.1 volts ±0.3 volt.
21	Same as step 16		Read VDVM	6.1 volts ±0.3 volt.
22	Remove A.C. power from isolator assembly and convert PS1 back to 120V A.C. operation.		See Note 1 of Schematic Diagram for conversion of PS1.	None.
23	Set up the VFPS to deliver 120V A.C. at 60 cycles.	FL3	*a.* Connect multimeter + lead to pin A of J2, connect the common or − lead to pin B of J2. Set Meter to read +6V D.C. *b.* Apply A.C. power	*b.* 0V ±0.5V.
24	Connect +5.5 volts and +5.5 volt return from PP-4571/G to FL3J3 pins A and B respectively.			0 Volts, ±0.5V.
25	Connect +6 volts and ground from power supply to FL3J4 pins A and B respectively.		Read multimeter	+6 volts ±1.0 volts.

Table 3-8. Isolator Assembly RE216/G Testing Procedures—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
26	Repeat steps 2 through 6.		Read multimeter.	+6 volts ± 1.0V.
27	Set output of power supply to +2.0V ±.2V.		Read multimeter.	+6 Volts ± 1.0V.
28	Repeat steps 2 through 6.		Read multimeter.	+6 volts ± 1.0V.
29	Remove power from FL3J3 and FL3J4.			
30	Repeat steps 11 and 12. Apply A.C. power.			
31	Repeat step 24.		Read multimeter.	0 volts ±0.5V.
32	Repeat step 25.		Read multimeter.	+6 volts ±0.5V.
33	Repeat steps 13 through 16.		Read multimeter.	+6 volts ±0.5V.
34	Set output of power supply +0+2.0V +2 volts.		Read multimeter.	+6 volts ±0.5V.
35	Repeat steps 13 through 17.		Read multimeter.	+6 volts ± 1.0V.
36	Repeat step 29.		Read multimeter.	+6 volts ± 1.0V.
37	Remove A.C. power and disconnect test equipment.	*Note.* PS1 is connected for 230V A.C. operation. It may be necessary to convert to 120V A.C. operation.		

3-31. Summary of Performance Standards

Arrange a checklist similar to the one shown in table 3-9. In the *Test Data* column, record the actual indications obtained during each of the indicated tests. This data may be used as a check against the performance standards.

Table 3-9. Performance Test Checklist

Step No.	Unit	Test	Performance standard	Test data
1	Control Indicator Panel.	+5 vdc.	+5 vdc.	
2		Lamp DS13.	DS13 lights.	
3		Operation of S10.	0 volts.	
4		Lamp Test Switch.	Lamps DS9 thru DS 14 light.	
5		Lamp DS1.	DS1 lights.	
6		Lamp DS2.	DS2 lights.	
7		Lamp DS3.	DS3 lights.	
8		Lamp DS4.	DS4 lights.	
9		Lamp DS5.	DS5 lights.	
10		Lamp DS6.	DS6 lights.	
11		Lamp DS7.	DS7 lights.	
12		Lamp DS8.	DS8 lights.	
13		Lamp DS15.	DS15 lights.	
14		Lamp DS16.	DS16 lights.	
15		TCU/CRYPTO switch.	a. DS9 lights. b. zero ohms.	
16		TCU/CRYPTO switch.	a. DS9 goes out. b. 100± 20 ohms.	
17			100± 20 ohms	
18		Shield.	zero ohms.	
19		Shield.	zero ohms.	
20		Shield.	zero ohms.	
21		R14.	100 ± 20 ohms.	

Table 3-9. Performance Test Checklist—Continued

Step No.	Unit	Test	Performance standard	Test data
22		XMIT/CANCEL switch	+5 vdc.	
23		STOP AT EOM/CONTINUE switch	+5 vdc.	
24		STOP AT EOM/CONTINUE switch	zero volts.	
25		R2	100 ± 20 ohms.	
27		STOP AT EOM/CONTINUE switch and R3.	a. DS14 lights. b. 100 ± 20 ohms.	
28		R17	100 ± 20 ohms.	
29		R18	100 ± 20 ohms.	
30		R19	100 ± 20 ohms.	
31		REQUEST MES RT switch	+5 vdc.	
32		STOP AT EOM/CONTINUE switch	+5 vdc.	
33		START XMIT switch	+5 vdc.	
34		MODE switch	*a.* DS10 lights. *b.* +5 vdc.	
35		MODE switch	+5 vdc.	
36		MODE switch	zero ohms.	
37		MODE switch	*a.* DS11 lights. *b.* zero ohms.	
38		MODE switch	+5 vdc.	
40		MODE switch	*a.* DS12 lights. *b.* zero ohms.	
41		R20	680 ohms.	
42		UNITS, TENS and HUNDREDS switches.	*a* through *l*.	
43		UNITS, TENS, and HUNDREDS switches.	*a.* Points *a*, *e*, *i*—open. *b.* All other points—zero ohms.	
44		UNITS, TENS and HUNDREDS switches.	*a.* Points *b*, *f*, *j*—open. *b.* All other points—zero ohms.	
45		UNITS, TENS and HUNDREDS switches.	*a.* Points *a*, *b*, *e*, *f*—open. *b.* All other points—zero ohms.	
46		UNITS, TENS and HUNDREDS switches.	*a.* Points *c*, *g*, *k*—open. *b.* All other points—zero ohms.	
47		UNITS, TENS, and HUNDREDS switches.	*a.* Points *a*, *c*, *e*, *g*, *i*, *k*—open. *b.* All other points—zero ohms.	
48		UNITS, TENS, and HUNDREDS switches.	*a.* Points *b*, *c*, *f*, *g*, *j*, *k*—open. *b.* All other points—zero ohms.	
49		UNITS, TENS, and HUNDREDS switches.	*a.* Points *a*, *b*, *c*, *e*, *f*, *g*—open. *b.* All other points—zero ohms.	
50		UNITS, TENS, and HUNDREDS switches.	*a.* Points *d*, *h*, *l*—open. *b.* All other points—zero ohms.	
51		UNITS, TENS and HUNDREDS switches.	*a.* Points *a*, *d*, *e*, *h*—open. *b.* All other points.	
52		ON/OFF switch	*a.* DS17 lights. *b.* +5 vdc.	
53		PRESET switch	+5 vdc.	
54		R22	1.2 K ± 120 ohms.	
56		R24	100 ± 10 ohms.	
57		HUNDREDS nixie indicator	Indicates 0.	
58		HUNDREDS nixie indicator	Indicates 1.	
59		HUNDREDS nixie indicator	Indicates 2.	
60		HUNDREDS nixie indicator	Indicates 3.	
61		HUNDREDS nixie indicator	Indicates 4.	
62		HUNDREDS nixie indicator	Indicates 5.	
63		HUNDREDS nixie indicator	Indicates 6.	
64		HUNDREDS nixie indicator	Indicates 7.	
65		HUNDREDS nixie indicator	Indicates 8.	

Table 3-9. Performance Test Checklist—Continued

Step No.	Unit	Test	Performance standard	Test data
66		HUNDREDS nixie indicator	Indicates 9.	
67		TENS nixie indicator	Indicates 0.	
68		TENS nixie indicator	Indicates 1.	
69		TENS nixie indicator	Indicates 2.	
70		TENS nixie indicator	Indicates 3.	
71		TENS nixie indicator	Indicates 4.	
72		TENS nixie indicator	Indicates 5.	
73		TENS nixie indicator	Indicates 6.	
74		TENS nixie indicator	Indicates 7.	
75		TENS nixie indicator	Indicates 8.	
76		TENS nixie indicator	Indicates 9.	
77		UNITS nixie indicator	Indicates 0.	
78		UNITS nixie indicator	Indicates 1.	
79		UNITS nixie indicator	Indicates 2.	
80		UNITS nixie indicator	Indicates 3.	
81		UNITS nixie indicator	Indicates 4.	
82		UNITS nixie indicator	Indicates 5.	
83		UNITS nixie indicator	Indicates 6.	
84		UNITS nixie indicator	Indicates 7.	
85		UNITS nixie indicator	Indicates 8.	
86		UNITS nixie indicator	Indicates 9.	
87		R4 and AUDIBLE ALARM	Audible alarm volume can be varied.	
89		ALARM TEST switch	Audible alarm sounds.	
90		Capacitor leakage	Leakage is within tolerances specified on front panel of capacitor analyzer.	
1	Power Supply	5.5 vdc power supply output	+4.5 vdc.	
2		Obtainable variation in 5.5 vdc output	2 volts.	
3		Obtainable variation in +12 vdc output	2 volts.	
4		Obtainable variation in −12 vdc output	2 volts.	
5		180 vdc output	180± 10 volts.	
6		5.5 vdc output with characteristic load	+4.5 vdc.	
7		63 cycle, 96 vac input	+4.50 vdc±0.055 volts.	
8		47.5 cycle, 132 vac input	+4.50 vdc±0.055 volts.	
9		63 cycle, 132 vac input	+4.50 vdc±0.055 volts.	
10		+5.5 vdc output unloaded	+4.50 vdc ±0.055 volts.	
11		+12 vdc output with characteristic load	+12.00 vdc.	
12		47.5 cycle, 96 vac input	+12 vdc ±0.3 volts.	
13		63 cycle, 96 vac input	+12 vdc ±0.3 volts.	
14		47.5 cycle, 132 vac input	+12 vdc ±0.3 volts.	
15		63 cycle, 132 vac input	+12 vdc ±0.3 volts.	
16		+12 vdc output unloaded	+12 vdc ±0.3 volts.	
17		−12 vdc output with characteristic load	−12.00 vdc.	
18		47.5 cycle, 96 vac input	−12 vdc ±0.3 volts.	
19		63 cycle, 96 vac input	−12 vdc ±0.3 volts.	
20		47.5 cycle, 132 vac input	−12 vdc ±0.3 volts.	
21		63 cycle, 132 vac input	−12 vdc ±0.3 volts.	
22		−12 vdc output unloaded	−12 vdc ±0.3 volts.	
23		+180 vdc output with characteristic load	180 vdc ±10 volts.	
24		47.5 cycle, 96 vac input	180 vdc ±10 volts.	
25		63 cycle, 96 vac input	180 vdc ±10 volts.	
26		47.5 cycle, 132 vac input	180 vdc ±10 volts.	
27		63 cycle, 132 vac input	180 vdc ±10 volts.	
28		+180 vdc output unloaded	180 vdc ±10 volts.	
29		+5.5 vdc ripple	Less than 50 mv peak to peak.	
30		+12 vdc ripple	Less than 200 mv peak to peak.	
31		−12 vdc ripple	Less than 200 mv peak to peak.	

Table 3-9. Performance Test Checklist—Continued

Step No.	Unit	Test	Performance standard	Test data
32		+180 vdc ripple	Less than 7.2 volts peak to peak.	
2	Simulator Test Panel.	DS1	DS1 lights.	
3		DS2	DS2 lights.	
4		DS3	DS3 lights.	
5		DS4	DS4 lights.	
6		DS5	DS5 lights.	
7		ENABLE/DISABLE switch and LAMP TEST switch.	zero volts.	
8		ENABLE/DISABLE switch	+5 vdc.	
9		SYS CLR switch and ENABLE/DISABLE switch.	+5 vdc.	
10		ENABLE/DISABLE switch and SYS CLR switch.	zero volts.	
11		LAMP TEST switch	+5 vdc.	
12		Continuity	zero ohms.	
13		R4, R2, R1	100 ± 10 ohms.	
14		R3	100 ± 10 ohms.	
15		C4	Leakage in tolerance.	
16		C3	Leakage in tolerance.	
17		C2	Leakage in tolerance.	
18		C1	Leakage in tolerance.	
19		J4 and J5	zero ohms.	
20		SPEED SEL switch	*a.* Check (1), (4)—zero ohms. *b.* Check (2), (3), (5) and (6)—open.	
21		SPEED SEL switch	*a.* Check (2), (5)—zero ohms. *b.* Check (1), (3), (4), and (6)—open.	
22		SPEED SEL switch	*a.* Check (3), (6)—zero ohms. *b.* Check (1), (2), (4), (5)—open.	
23		XMIT and RECEIVE switches	*a.* 13, 14, 15, 24, 25, 26, 27—zero. *b.* 12, 13, 16, 17, 18, 19, 20, 21, 22, 23—open.	
24		XMIT and RECEIVE switches	*a.* 14, 15, 24, 25, 26, 27—zero. *b.* 12, 13, 16, 17, 18, 19, 20, 21, 22, 23—open.	
25		XMIT and RECEIVE switches	zero ohms.	
26		XMIT and RECEIVE switches	*a.* 13, 15, 16, 17, 18, 19, 20, 21, 22, 23—zero. *b.* 12, 14, 24, 25, 26, 27—open.	
27		XMIT and RECEIVE switches	zero ohms.	
28		XMIT and RECEIVE switches	*a.* 13, 14, 24, 25, 26, 27—zero. *b.* 12, 15, 16, 17, 18, 19, 20, 21, 22, 23—open.	
29		XMIT and RECEIVE switches	zero ohms.	
30		XMIT and RECEIVE switches	*a.* 13, 14, 24, 25, 26 and 27—zero. *b.* 12, 15, 16, 17, 18, 19, 20, 21, 22, 23—open.	
31		XMIT and RECEIVE switches	zero ohms.	
32		XMIT and RECEIVE switches	*a.* 13, 14, 15, 25, 26 and 27—zero. *b.* 12, 16, 17, 18, 19, 20, 21, 22, 23, 24—open.	
33			zero ohms.	
34		XMIT and RECEIVE switches	*a.* 13, 14, 15, 26 and 27—zero. *b.* 12, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25—open.	

Table 3-8. Performance Test Checklist—Continued

Step No.	Unit	Test	Performance standard	Test data
35		XMIT and RECEIVE switches	zero ohms.	
36		XMIT and RECEIVE switches	*a.* 13, 14, 15, 25 and 27—zero. *b.* 12, 16, 17, 18, 19, 20, 21, 22, 23, 24, 26—open.	
37		XMIT and RECEIVE switches	zero ohms.	
38		XMIT and RECEIVE switches	*a.* 13, 14, 15, 25 and 26—zero. *b.* 12, 16, 17, 18, 19, 20, 21, 22, 23, 24 and 27—open.	
39		XMIT and RECEIVE switches	zero ohms.	
1	T-R Filter	Continuity between the following points: J1-Y to P1-10. J1-Z to P1-11. J1-C to P1-7. J1-W to P1-19. J1-X to P1-20. J1-R to P1-22. J1-S to P1-23. J1-A to P1-8. J1-K to P1-14. J1-L to P1-15. J1-M to P1-13. J1-A to P2-1. J1-B to P1-9. J1-B to P2-3. P1-25 to P2-4. P1-26 to P2-6. P1-27 to P2-5. J2-A to violet ground lead J2-B to violet and white ground lead.	Zero ohms between all points measured.	
2		Operation of A5A1	Output bit pattern correct (RY).	
3		Operation of A5A2	Output bit pattern correct (RY).	
4		Operation of A5A3	Output bit pattern correct (RY).	

3-32. Logic Rack Assembly A2 Tests

Use a multimeter and perform a continuity test of assembly A2. Use figure 2-3 as a guide to the correct wiring configuration.

Section III. DEPOT OVERHAUL STANDARDS

3-33. Applicability of Depot Overhaul Standards

The tests outlined in this section are designed to measure the performance capability of a repaired equipment. Equipment that meets the minimum standards stated in the tests will have performance capabilities equivalent to those of new equipment. Tests that measure the performance capability of repaired equipment components are included in the technical publication listed below.

3-34. Applicable References

a. Repair Standards. Applicable procedures of the depots performing these tests and the general standards for repaired electronic equipment given in TB SIG 355-1, TB SIG 355-2, and TB SIG 355-3 form a part of the requirements for testing this equipment.

b. Technical Publications. TM 11-5815-335-12 is applicable to this equipment.

c. Modification Work Orders. Perform all applicable modification work orders pertaining to this equipment before making the tests specified. DA Pam 310-7 lists all current MWO's.

3-35. Test Facilities Required

The following test equipment, or suitable equivalent, will be used to determine compliance with the requirements of this specific depot overhaul standard.

a. Test Equipment.

Equipment	Quantity required
MULTIMETER TS-352B/U	2
Data Analysis Center AN/GGM-11 (Stelma DAC-7B)	1
Oscilloscope AN/USM-309(V) (HP model 140A with No. H06-1405A and No. 1421A plug-in units)	1
Probe, Voltage Divider MX-6346/U (HP No. C0-2-10003A)	1
Probe, Voltage Divider MX-5116/USM (HP No. C0-2-10003B)	1
Cart, Oscilloscope MX-6348/U (HP No. 1115)	1
Generator, Square Wave, (Precision Model E-310)*	1
Power Supply, Variable Frequency (Comm. Meas. Labs Model N1500/SG13A)	1
Autotransformer 115/230 Volts, 500VA	1
Resistor, Decade (General Radio Model 1434M)	1
Teletypewriter Set AN/FGC-58 or AN/FGC-25	2
Interface Conversion Group AN/UGA-8	2

*Equivalent must have a positive reference ground.

b. Additional Equipment.

Equipment	Quantity required
Test tapes	6
Signal interface adapter cable	2
System interface adapter cable	2
Power adapter cable with polarized plug	2

c. Materials.

Quantity	Item
1	Terminal board (16 double screw contacts).
2	Connector, plug MS3106K-24-28S.
3	Connector, plug MS3106K-10SL-3S.
2	Connector, plug MS3106K-14-2S.
19 ft.	Cable, power, three conductor.
100 ft.	Wire, insulated twisted pair, No. 22 AWG.
1	Resistor, 600 ohm, 1/4 watt.

3-36. Fabrication of Test Cable Assemblies

Fabricate test cable assemblies using materials listed in paragraph 3-35c and following the procedures given in *a*, *b*, and *c* below.

a. Signal Interface Adapter Cable Assembly (fig. 3-29).

(1) Cut 13 lengths of No. 22 gage twisted pair wire in 5-foot lengths.

(2) Strip 1 inch of insulation from both ends of each length of wire.

(3) Stencil the terminal board as shown in figure 3-29.

(4) Tin and connect eight lengths of the twisted pair wire between connector MS3106K-24-28S and the terminal board, as shown in figure 3-29.

(5) Tin and connect five lengths of the twisted pair wire between the 26-pin connector and the terminal board, as shown in figure 3-29.

b. System Interface Adapter Cable Assembly (fig. 3-30).

(1) Cut seven lengths of No. 22 gage twisted pair wire in 5-foot lengths.

(2) Strip 1 inch of insulation from both ends of each length of wire.

(3) Tin and connect five lengths of the twisted pair wire between connector MS-3106K-24-28S and the 26-pin connector of the AN/UGA-8, as shown in figure 3-30.

(4) Tin and connect two lengths of wire to connector MS3106K-24-28S, as shown in figure 3-30. Tag the loose ends of the wires as shown.

c. Power Adapter Cable with Polarized Plug (fig. 3-20). Refer to paragraph 3-23*d* for fabrication of the power cable.

3-37. Fabrication of Test Tapes

To perform the different tests on the TCU, the following test tapes must be fabricated. The test tapes are punched on chadless tape so that the tapes can be looped.

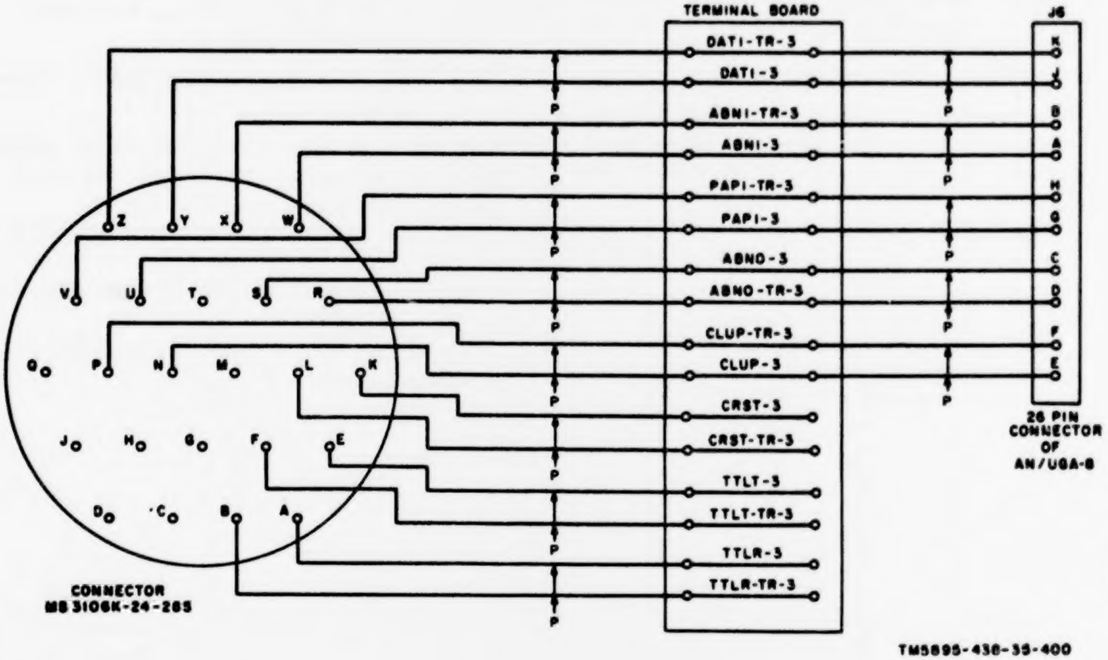
Note. Type consecutive letters at the beginning and end of each test tape so that the test tape can be looped.

a. General. The symbols given below do not appear on the test tapes but signify:

(1) CR: Carriage return.
(2) LF: Line feed.
(3) SP: Space.
(4) FIG: Figures.

b. Test Tape Punching. Set the switch at the left of the teletypewriter keyboard to KT.

c. Test Tape No. 1. On the teletypewriter keyboard, type: LETTERS CR CR LF P SP TCUTEST CR CR LF THE SP QUICK SP



TERMINAL BOARD
J6
DATI-TR-3
DATI-3
ABNI-TR-3
ABNI-3
PAPI-TR-3
PAPI-3
ABNO-3
ABNO-TR-3
CLUP-TR-3
CLUP-3
CRST-3
CRST-TR-3
TTLT-3
TTLT-TR-3
TTLR-3
TTLR-TR-3
K
J
B
A
H
G
C
D
F
E
P
Z
Y
X
W
V
U
T
S
R
Q
N
M
L
J
H
G
F
E
D
C
B
A
26 PIN CONNECTOR OF AN/UGA-8
CONNECTOR MS3106K-24-28S
TM5895-430-35-400

Figure 3-29. Signal interface adapter cable assembly, fabrication diagram.

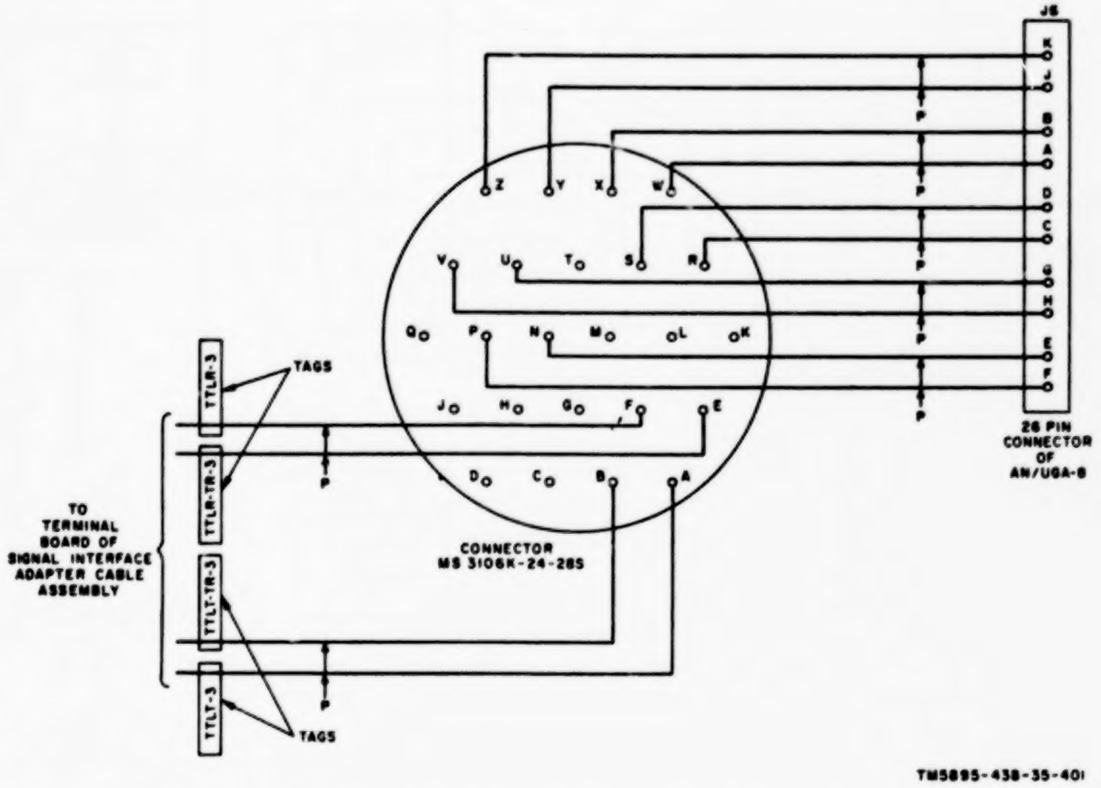

J6
K
J
B
A
D
C
G
H
E
F
P
Z
Y
X
W
V
U
T
S
R
Q
P
N
M
L
K
J
H
G
F
E
D
C
B
A
TAGS
TTLR-3
TTLR-TR-3
TTLT-TR-3
TTLT-3
TAGS
TO TERMINAL BOARD OF SIGNAL INTERFACE ADAPTER CABLE ASSEMBLY
CONNECTOR MS 3106K-24-28S
26 PIN CONNECTOR OF AN/UGA-8
TM5895-438-35-401

Figure 3-30. System interface adapter cable assembly, fabrication diagram.

BROWN SP FOX SP JUMPED SP OVER SP THE SP LAZY SP DOG FIG Δ LETTERS S SP BACK CR CR LF FIG 1234567890.

d. Test Tape No. 2. On the teletypewriter keyboard, type: LETTERS CR CR LF P SP B (repeat for 60 consecutive B's).

e. Test Tape No. 3. On the teletypewriter keyboard, type : LETTERS CR CR LF P SP TCUTEST CR CR LF THE SP QUICK SP BROWN SP FOX SP JUMPED SP OVER SP THE SP LAZY SP DOG FIG Δ LETTERS S SP BACK FIG CR CR LF 1234567890 CR CR LF LETTERS NNNN.

f. Test Tape No. 4. On the teletypewriter keyboard, type: LETTERS CR CR LF W (repeat for 60 consecutive W's).

3–38. TCU Test Mode Operational Test

The TCU test mode operational test evaluates the performance of the TCU in the test mode. Check the control sequences generated by the TCU by operating the controls and monitoring the indicators on the simulator test panel.

a. Test Equipment and Materials.

(1) Teletypewriter Set AN/FGC-58 or AN/FGC-25.

(2) Interface Conversion Group AN/UGA-8.

(3) Test tape No. 1.

(4) Signal interface adapter cable (two required).

(5) Power adapter cable with polarized plug.

(6) Terminal board (16 double screw contacts).

b. Test Connections and Conditions. Connect the equipment as shown in figure 3-31.

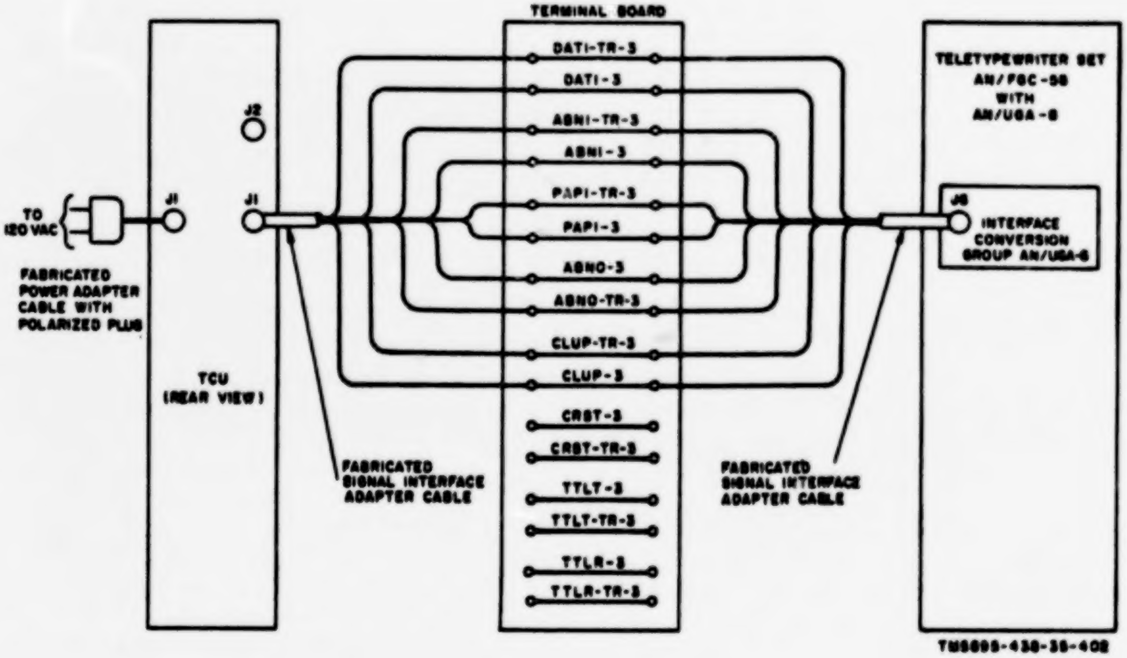

TERMINAL BOARD
DATI-TR-3
DATI-3
ABNI-TR-3
ABNI-3
PAPI-TR-3
PAPI-3
ABNO-3
ABNO-TR-3
CLUP-TR-3
CLUP-3
CRST-3
CRST-TR-3
TTLT-3
TTLT-TR-3
TTLR-3
TTLR-TR-3
TO 120 VAC
J1
J2
J1
FABRICATED POWER ADAPTER CABLE WITH POLARIZED PLUG
TCU (REAR VIEW)
FABRICATED SIGNAL INTERFACE ADAPTER CABLE
FABRICATED SIGNAL INTERFACE ADAPTER CABLE
TELETYPEWRITER SET AN/FGC-58 WITH AN/UGA-6
J6
INTERFACE CONVERSION GROUP AN/UGA-6
TM5895-438-35-402

Figure 3-31. TCU test mode operational test setup.

c. *Test Procedure.*

Step No.	Test procedure	Performance standard	
		Simulator test panel	Control indicator panel
	Note: TCU power supply must be strapped for 120 vac for this test. Procedure for strapping TCU power supply is given in TM 11-5815-335-12.		
1	Set controls on TCU control indicator panel as follows: *a.* MODE switch to TEST. *b.* TCU/CRYPTO switch to TCU. *c.* STOP AT EOM/CONTINUE switch to CONTINUE. *d.* AUTO NO. OFF/ON switch to ON. NUMBER SELECT switches to 000. VOLUME control to approximately midposition.		
2	Set controls on TCU simulator test panel as follows: *a.* SPEED SEL switch to 75. *b.* RT ENABLE/DISABLE switch to RT ENABLE. *c.* Red and black knobs of CON SEQ SIMULATOR switch to OFF.		

Step No.	Test procedure	Performance standard	
		Simulator test panel	Control indicator panel
	Note: All control settings referred to in this test procedure are located on simulator test panel unless specifically stated otherwise.		
3	Turn on teletypewriter. Set TCU power supply AC POWER ON/OFF switch to ON. Insert test tape No. 1.	N/A.	POWER ON, CANCEL XMITTED, TEST, and TCU lamps light.
4	Depress LAMP TEST switch.	All lamps light.	N/A.
5	Activate SYS CLR switch.	ACK-2R and ACK-2T. lamps light.	N/A.
6	Turn red and black knobs of CON SEQ SIMULATOR switch to ACK-1.	MON lamp blinks ACK-1R and ACK-1T lamps light.	N/A.
7	Turn red and black knobs of CON SEQ SIMULATOR switch to ACK-2, and activate SYS CLR switch.	MON lamp blinks. ACK-2R and ACK-2T lamps light.	N/A.
8	Turn red and black knobs of CON SEQ SIMULATOR switch to STOP, and activate SYS CLR switch.	MON lamp blinks.	STOP lamp blinks.
9	Turn red and black knobs of CON SEQ SIMULATOR switch to REP, and activate SYS CLR switch.	MON lamp blinks.	STOP lamp stops blinking (extinguishes).
10	Turn red knob of CON SEQ SIMULATOR switch to ACK-2.	MON lamp blinks.	N/A.
11	Turn red and black knobs of CON SEQ SIMULATOR switch to RT, and activate SYS CLR switch.	MON lamp blinks.	ALARM lamp lights, and AUDIBLE ALARM sounds.

Step No.	Test procedure	Performance standard	
		Simulator test panel	Control indicator panel
12	Turn red knob of CON SEQ SIMULATOR switch to CANCEL.	MON lamp blinks.	Same as step 11.
13	Turn red knob of the CON SEQ SIMULATOR switch to ACK-2.	MON lamp blinks.	Same as step 11.
14	Turn red and black knobs of CON SEQ SIMULATOR switch to CANCEL, and activate SYS CLR switch.	MON lamp blinks.	ALARM lamp extinguishes, and AUDIBLE ALARM stops sounding.
15	Turn red knob of CON SEQ SIMULATOR switch to ACK-2.	MON lamp blinks.	N/A.
16	Turn red and black knobs of CON SEQ SIMULATOR switch to START, and activate SYS CLR switch.	MON lamp blinks.	N/A.
17	Turn red knob of the CON seq simulator switch to ACK-2. Place black knob of CON SEQ simulator switch to OFF, and activate SYS CLR switch.	MON lamp lights.	N/A.
18	Activate control indicator panel XMIT CANCEL switch, and quickly monitor simulator test panel.	MON lamp extinguishes and then relights.	N/A.
19	Turn red knob of CON SEQ SIMULATOR switch to RT, and activate SYS CLR switch.	MON lamp extinguishes.	N/A.
20	Insert test tape No. 1, and activate control indicator panel START XMIT switch.	N/A.	XMIT IN PROGRESS and RECEIVE IN PROGRESS lamps light, and CANCEL XMITTED lamp extinguishes. Teletypewriter prints out test tape No. 1.

Step No.	Test procedure	Performance standard	
		Simulator test panel	Control indicator panel
21	Activate control indicator panel REQUEST MES RT switch. *Note:* If data handling and control sequence test is to be performed, do not disconnect test setup.	MON lamp blinks.	ALARM lamp lights, AUDIBLE ALARM sounds, STOP lamp blinks, and teletypewriter stops message printout.
22	Turn TCU power supply AC POWER ON/OFF switch to OFF. Turn off teletypewriter. Disconnect test setup.		

3-39. Data Handling and Control Sequence Test

The data handling and control sequence test evaluates the performance of the TCU under simulated normal traffic conditions. All control sequences generated during normal traffic conditions are checked as well as the ability of the TCU to receive and transmit data simultaneously. An additional TCU is used to simulate the distant station.

a. Test Equipment and Materials.

(1) Teletypewriter Set AN/FGC-58 or AN/FGC-25 (two required).

(2) Interface Conversion Group AN/UGA-8 (two required).

(3) Teletypewriter Control Unit C-7050/G.

(4) Test tape No. 3.

(5) Signal interface adapter cable (two required).

(6) System interface adapter cable (two required).

(7) Power adapter cable with polarized plug (two required).

(8) Terminal board (16 double screw contacts).

b. Test Connections and Conditions. Connect the equipment as shown in figure 3-32.

c. Special Conditions.

(1) Strapping connections are required on printed circuit board 1A2A17 on the TCU under test and on the spare unit. Remove the boards from the equipments. Record any jumpered connections already on the boards. With insulated jumper wires (with tinned ends) make the following connections:

(*a*) Terminal 1 to terminals 11 and 12.

(*b*) Terminal G to terminals 13, 14, and 15.

(*c*) Terminal 2 to terminals 21, 23, and 24.

(*d*) Terminal G to terminals 22 and 25.

(*e*) Terminal 3 to terminals 31 and 32.

(*f*) Terminal G to terminals 33, 34, and 35.

(2) Reinsert the boards into the teletypewriter control units and perform the tests given in *d* below.

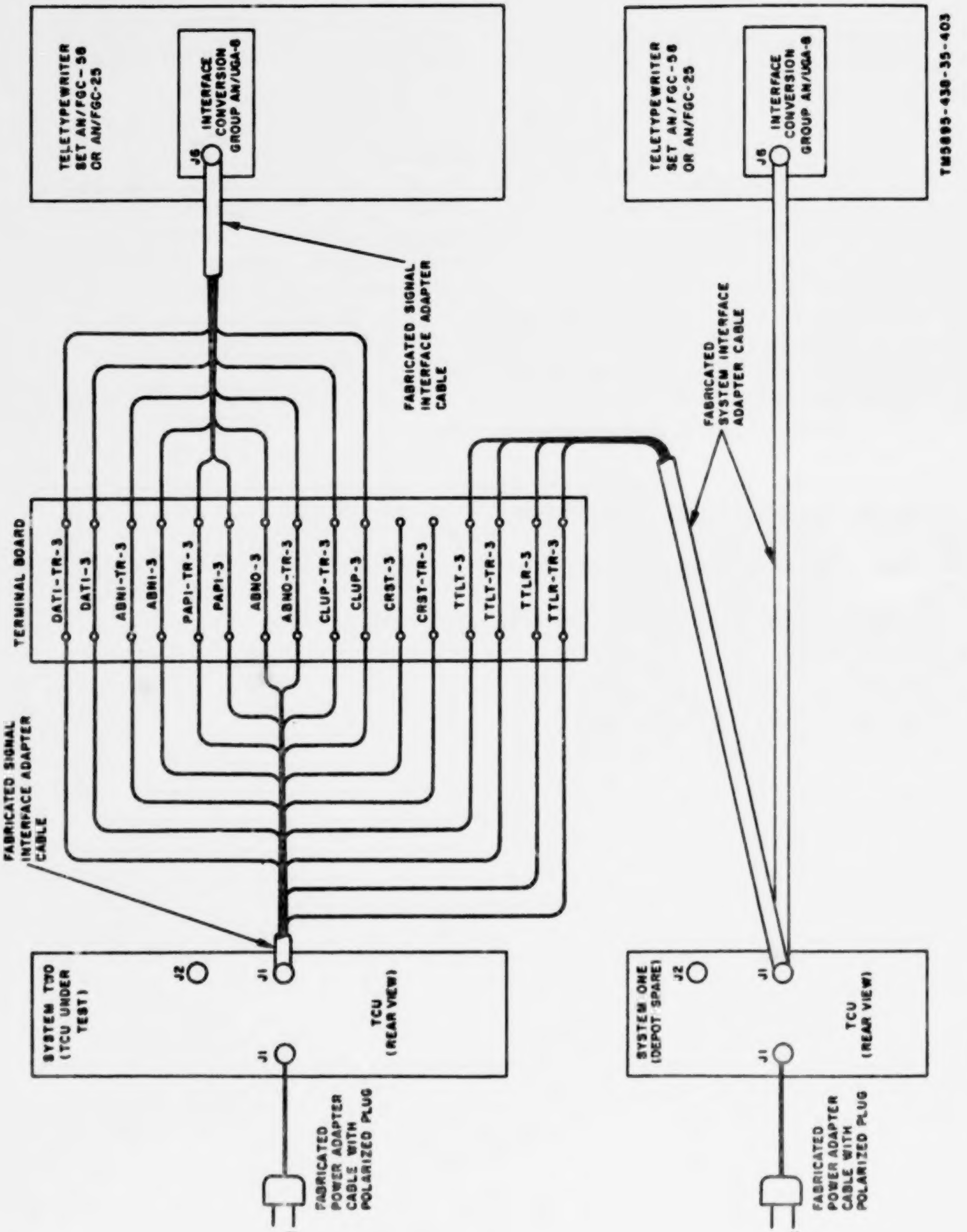

TELETYPEWRITER SET AN/FGC-58 OR AN/FGC-25
J6
INTERFACE CONVERSION GROUP AN/UGA-8
TELETYPEWRITER SET AN/FGC-58 OR AN/FGC-25
J6
INTERFACE CONVERSION GROUP AN/UGA-8
TM5815-438-35-403
FABRICATED SIGNAL INTERFACE ADAPTER CABLE
FABRICATED SYSTEM INTERFACE ADAPTER CABLE
TERMINAL BOARD
DATI-TR-3
DATI-3
ABNI-TR-3
ABNI-3
PAPI-TR-3
PAPI-3
ABNO-3
ABNO-TR-3
CLUP-TR-3
CLUP-3
CRST-3
CRST-TR-3
TTLT-3
TTLT-TR-3
TTLR-3
TTLR-TR-3
FABRICATED SIGNAL INTERFACE ADAPTER CABLE
SYSTEM TWO (TCU UNDER TEST)
J2
J1
J1
TCU (REAR VIEW)
SYSTEM ONE (DEPOT SPARE)
J2
J1
J1
TCU (REAR VIEW)
FABRICATED POWER ADAPTER CABLE WITH POLARIZED PLUG
TO 120 VAC
FABRICATED POWER ADAPTER CABLE WITH POLARIZED PLUG
TO 120 VAC

Figure 3-32. General test setup.

d. Test Procedure.

Step No.	Test procedure	Performance standard System No. 1	Performance standard System No. 2
	Note: TCU power supply must be strapped for 120 vac for this test. Procedure for strapping TCU-power supply is given in TM 11-5815-335-12.		
1	Preset controls on control indicator panels of TCU system No. 1 (depot spare) and TCU system No. 2 (TCU under test) as follows: *a.* MODE switch to NORMAL. *b.* TCU/CRYPTO switch to TCU. *c.* STOP AT EOM/CONTINUE switch to CONTINUE. *d.* AUTO NO. OFF/ON switch to ON. *e.* NUMBER SELECT switches to 000. *f.* VOLUME control to approximately midposition.		
2	Preset controls on simulator test panels of both TCU's as follows: SPEED SEL switch to 75.0. RT ENABLE/DISABLE switch to RT ENABLE. Red and black knobs of CON SEQ SIMULATOR to OFF.		

Step No.	Test procedure	Performance standard	
		System No. 1	System No. 2
	Note: All control settings referred to in this test procedure are located on control indicator panels unless specifically stated otherwise.		
3	Set power supply AC POWER ON/OFF switch on TCU systems No. 1 and No. 2 to ON. Turn on teletypewriters. Activate SYS CLR switch on simulator test panel of system No. 1; then, within 4 seconds, activate SYS CLR switch on system No. 2.	POWER ON CANCEL XMITTED, NORMAL, and TCU lamps light.	Same as system No. 1.
4	Place test tapes No. 3 in both tape readers.	N/A.	N/A.
5	Set system No. 2 NUMBER SELECT switches as follows: *a.* HUNDREDS switch to 5. *b.* TENS switch to 8. *c.* UNITS switch to 5.		
6	Activate system No. 2 PRESET switch.	N/A.	N/A
7	Depress system No. 2 LAMP TEST switch.	N/A.	All lamps (except fuse indicators) light.
8	Activate system No. 2 START XMIT switch.	RECEIVE IN PROGRESS lamp lights during message reception, and teletypewriter prints out: VZCZC AFA 585 TCUTEST THE QUICK BROWN FOX JUMPED OVER THE LAZY DOG △ S BACK 1234567890 NNNN.	CANCEL XMITTED lamp extinguishes. XMIT IN PROGRESS lamp lights during message transmission. MESSAGE NUMBER reads 585.

N/A.

iission.
tops sou

Step No.	Test procedure	Performance standard	
		System No. 1	System No. 2
9	Allow system No. 2 to continue transmitting test tape.	Same as above, except message number increases by one unit each time message is printed.	MESSAGE NUMBER advances on unit (for example, 586, 587) each time test tape is transmitted.
10	Activate system No. 2 XMIT CANCEL switch.	RECEIVE IN PROGRESS lamp extinguishes, and the teletypewriter stops message printout.	XMIT IN PROGRESS lamp extinguishes, and CANCEL XMITTED lamp lights. Teletypewriter stops sending test tape.
11	Activate system No. 1 START XMIT switch.	CANCEL XMITTED lamp extinguishes. XMIT IN PROGRESS lamp lights during message transmission. MESSAGE NUMBER is undetermined and indicated XXX.	RECEIVE IN PROGRESS lamp lights during message reception, and teletypewriter prints out: VZCZC AFA XXX TCUTEST THE QUICK BROWN FOX JUMPED OVER THE LAZY DOG △S BACK 1234567890 NNNN.
12	Place system No. 2 STOP AT EOM/CONTINUE switch to STOP AT EOM during receipt of a message.	STOP lamp blinks when message transmission ends.	STOP AT EOM lamp lights. At end of message, ALARM lamp lights, and AUDIBLE ALARM sounds. Teletypewriter stops sending test tape.
13	Activate system No. 2 RESET switch.	N/A.	AUDIBLE ALARM stops sounding.
14	Place system No. 2 STOP AT EOM/CONTUE switch to CONTINUE.	STOP lamp extinguishes. Teletypewriter begins to transmit test tape.	ALARM and STOP AT EOM lamps extinguish. Teletypewriter continues message printout.
15	Activate system No. 1 XMIT CANCEL switch.	At end of message, XMIT IN PROGRESS lamp extinguishes, and CANCEL XMITTED lamp lights. Teletypewriter stops message transmission.	RECEIVE IN PROGRESS lamp extinguishes at end of message. Teletypewriter stops message printout.
16	Activate system No. 2 START XMIT switch.	Same as step 8, except for message number.	Same as step 8, except for message number.
17	Activate system No. 2 STOP AT EOM switch during transmission of a message.	RECEIVE IN PROGRESS lamp extinguishes at end of message printout.	STOP AT EOM lamp lights. At end of message, XMIT IN PROGRESS lamp extinguishes, and ALARM lamp lights. AUDIBLE ALARM sounds. Teletypewriter stops message transmission.
18	Activate system No. 2 RESET switch.	N/A.	AUDIBLE ALARM stops sounding.

Step No.	Test procedure	Performance standard	
		System No. 1	System No. 2
19	Activate system No. 2 START XMIT switch.	Same as step 8, except for message number.	Same as step 8, except for message number.
20	Activate system No. 1 START XMIT switch.	Same as step 11.	Same as step 11
21	Activate system No. 2 REQUEST MESSAGE RT switch during receipt of a message.	STOP lamp blinks, and XMIT IN PROGRESS lamp extinguishes. CANCEL XMITTED lamp lights. AUDIBLE ALARM sounds, and ALARM lamp lights. Tape reader stops message transmission.	RECEIVE IN PROGRESS lamp extinguishes, and teletypewriter stops message printout.
22	Activate system No. 1 RESET switch.	AUDIBLE ALARM stops sounding.	N/A.
23	Activate system No. 1 START XMIT switch.	ALARM and CANCEL XMITTED lamps extinguish. STOP lamp extinguishes. XMIT IN PROGRESS lamp lights, and tape reader begins message transmission.	Same as step 11.
24	Activate system No. 1 REQUEST MESSAGE RT switch during receipt of a message.	RECEIVE IN PROGRESS lamp extinguishes, and teletypewriter stops message printout.	STOP lamp blinks, XMIT IN PROGRESS lamp extinguishes, and CANCEL XMITTED lamp lights. AUDIBLE ALARM sounds, and ALARM lamp lights. Tape reader stops message transmission.
25	Activate system No. 2 RESET switch.	N/A.	AUDIBLE ALARM stops sounding.
26	Activate system No. 2 START XMIT switch.	Same as step 8, except for message number.	ALARM, CANCEL XMITTED, and STOP lamps extinguish. XMIT IN PROGRESS lamp lights, and tape reader begins message transmission.
27	Remove paper from teletypewriter in system No. 2 during receipt of a message.	N/A.	OUTPUT and ALARM lamps light, and AUDIBLE ALARM sounds.
28	Activate system No. 2 RESET switch, and reposition paper in teletypewriter.	N/A.	AUDIBLE ALARM sounds, and OUTPUT and ALARM lamps extinguish.
29	Remove test tape from tape reader in system No. 2.	N/A.	INPUT and ALARM lamps light, and AUDIBLE ALARM sounds.

Step No.	Test procedure	Performance standard	
		System No. 1	System No. 2
30	Activate system No. 2 RESET switch. Reposition tape in tape reader of system No. 2, and activate START XMIT switch.	N/A.	AUDIBLE ALARM stops sounding. INPUT and ALARM lamps extinguish, and 3 RPT and ALARM lamps light. AUDIBLE ALARM sounds
31	Place system No. 1 MODE switch to EMERGENCY, and activate system No. 2 XMIT CANCEL switch.	N/A.	
32	Place system No. 1 MODE switch to NORMAL. Place power supply AC POWER ON/OFF switch on TCU systems No. 1 and No. 2 to OFF. Turn off teletypewriter. *Note:* If enquiry response test set is to be performed, do not disconnect test setup.	N/A.	N/A.
33	Disconnect test setup.	END OF TEST.	

3-40. Enquiry Response Test

The enquiry response test determines whether a TCU equipped with enquiry response logic will correctly transmit its routing indicator in response to an enquiry input command. A second TCU is used to simulate the distant station and receive the routing indicator. The routing indicator will be printed out on the teletypewriter under control of the second TCU.

a. Test Equipment and Materials.

(1) Teletypewriter Set AN/FGC-58 or AN/FGC-25 (two required).

(2) Interface Conversion Group AN/UGA-8 (two required).

(3) Teletypewriter Control Unit C-7050/G.

(4) Test tape No. 4.

(5) Signal interface adapter cable (two required).

(6) System interface adapter cable (two required).

(7) Power adapter cable with polarized plug (two required).

(8) Terminal board (16 double screw contacts).

b. Test Connections and Conditions. Connect the equipment as shown in figure 3-32.

c. *Test Procedure.*

Step No.	Test procedure	Performance standard	
		System No. 1 (depot spare)	System No. 2 (TCU under test)
	Note: TCU power supply must be strapped for 120 vac for this test. The procedure for strapping the TCU is given in TM 11-5815-335-12.		
1	Set controls on control indicator panels of TCU system No. 1 (depot spare) and TCU system No. 2 (TCU under test) as follows: *a.* MODE switch to NORMAL. *b.* TCU/CRYPTO switch to TCU. *c.* STOP AT EOM/CONTINUE switch to CONTINUE. *d.* AUTO NO. OFF/ON switch to ON. *e.* NUMBER SELECT switches to 000. *f.* VOLUME control to approximately midposition.		
2	Preset controls on simulator test panels of both TCU's as follows: *a.* SPEED SEL switch to 75.0. *b.* RT ENABLE/DISABLE switch to RT ENABLE.		

Step No.	Test procedure	Performance standard	
		System No. 1 (depot spare)	System No. 2 (TCU under test)
	c. Red and black knobs of CON SEQ SIMULATOR switch to OFF. *Note:* All control settings referred to in this test procedure are located on control indicator panels unless specifically stated otherwise.		
3	Set power supply AC POWER ON/OFF switch on TCU systems No. 1 and No. 2 to ON. Turn on teletypewriters. Activate SYS CLR switch on simulator test panel of system No. 1; then, within 4 seconds activate SYS CLR switch on system No. 2.	POWER ON, CANCEL XMITTED, NORMAL, and TCU lamps light.	Same as system No. 1.
4	Position test tape No. 4 in tape reader of system No. 1 so that WW are first two letters to be printed.	N/A	N/A
5	Place system No. 1 MODE switch to EMERGENCY.	Teletypewriter prints out VZCZC, followed by from four to seven letters. These letters are routing indicator of TCU and vary for each site.	N/A
6	Place system No. 1 MODE switch to NORMAL.	N/A	N/A

Step No.	Test procedure	Performance standard	
		System No. 1 (depot spare)	System No. 2 (TCU under test)
7	Set power supply AC POWER ON/OFF switch on TCU systems No. 1 and No. 2 to OFF. Turn teletypewriters off. *Note:* If emergency operation test is to be performed, do not disconnect test setup.	N/A	N/A
8	Disconnect test setup.		

3-41. Emergency Operation Test

The emergency operation test determines the TCU's ability to transmit and receive messages while operating in the emergency mode. A second TCU is used to simulate the distant station.

a. Test Equipment and Materials.

(1) Teletypewriter Set AN/FGC-58 or 3FGC-25 (two required).

(2) Interface Conversion Group AN/UGA-8(two required).

(3) Teletypewriter Control Unit C-7050/G.

(4) Test tape No. 3.

(5) Signal interface adapter cable (two required).

(6) System interface adapter cable (two required).

(7) Power adapter cable with polarized plug (two required).

(8) Terminal board (16 double screw contacts).

b. Test Connections and Conditions. Connect the equipment as shown in figure 3-32.

c. *Test Procedure.*

Step No.	Test procedure	Performance standard	
		System No. 1 (depot spare)	System No. 2 (TCU under test)
	Note: The TCU power supply must be strapped for 120 vac for this test. Procedure for strapping TCU power supply is given in TM 11-5815-335-12.		
1	Set controls on control indicator panel of TCU systems No. 1 (depot spare) and No. 2 (TCU under test) as follows: *a.* MODE switch to NORMAL. *b.* TCU/CRYPTO switch to TCU. *c.* STEP AT EOM/CONTINUE switch to CONTINUE. *d.* AUTO NO. OFF/ON switch to ON. *e.* NUMBER SELECT switches to 000. *f.* VOLUME control to approximately midposition.		
2	Set controls on simulator test panels of both TCU's as follows: *a.* SPEED SEL switch to 75.0. *b.* RT ENABLE/DISABLE switch to RT ENABLE.		

Step No.	Test procedure	Performance standard	
		System No. 1 (depot spare)	System No. 2 (TCU under test)
	c. Red and black knobs of CON SEQ SIMULATOR switch to OFF. *Note:* All control settings referred to in this test procedure are located on control indicator panels unless specifically stated otherwise.		
3	Set power supply AC POWER ON/OFF OFF switch on TCC systems No. 1 and No. 2 to ON. Turn on teletypewriters. Activate SYS CLR switch on system No. 1 simulator test panel; then, within 4 seconds, activate SYS CLR switch on system No. 2 simulator test panel.	POWER ON, CANCEL XMITTED, NORMAL, and TCU lamps light.	POWER ON, CANCEL XMITTED, NORMAL, and TCU lamps light.
4	Place test tape 3 in tape readers.	N/A.	N/A.
5	Activate systems No. 1 and No. 2 START XMIT switches.	CANCEL XMITTED lamp extinguishes, XMIT IN PROGRESS lamp lights, and RECEIVE IN PROGRESS lamp lights. Teletypewriter prints out: VZCZC TCUTEST THE QUICK BROWN FOX JUMPED OVER THE LAZY DOG'S BACK 123456 7890 NNNN.	CANCEL XMITTED lamp extinguishes, XMIT IN PROGRESS lamp lights, and RECEIVE IN PROGRESS lamp lights. Teletypewriter prints out: VZCZC TCUTEST THE QUICK BROWN FOX JUMPED OVER THE LAZY DOG'S BACK 1234567890 NNNN.

Step No.	Test procedure	Performance standard System No. 1 (depot spare)	 System No. 2 (TCU under test)
6	Allow systems No. 1 and No. 2 to continue transmitting test tapes and, during next message, place systems No. 1 and No. 2 MODE switches to EMERGENCY.	NORMAL lamp extinguishes, EMERGENCY lamp lights, and teletypewriter continuously prints out test message.	NORMAL lamp extinguishes, EMERGENCY lamp lights, and teletypewriter continuously prints out test message.
7	Set systems No. 1 and No. 2 MODE switches to NORMAL, and AC POWER ON/OFF switches to OFF. Turn off teletypewriters. *Note:* If crypto circuitry test is to be performed, do not disconnect test setup.	N/A.	N/A.
8	Disconnect test setup.		

4-42. Crypto Circuitry Test

The crypto circuitry test evaluates the performance of a TCU while operating in the crypto mode. Messages at the cyrpto baud rate are received by the TCU and printed on the teletypewriter under TCU control. A square wave generator is used to simulate the crypto step signal input.

a. Test Equipment and Materials.

(1) Teletypewriter Set AN/FGC-58 or AN/FGC-25.

(2) Interface Conversion Group AN/UGA-8.

(3) Test tape No. 3.

(4) Square Wave Generator, Precision Model E310.

(5) Oscilloscope AN/USM-309(V).

(6) Signal interface adapter cable (two required).

(7) Power adapter cable with polarized plug.

(8) Terminal board (16 double screw contacts).

b. Test Connections and Conditions. Connect the equipment as shown in figure 3-33.

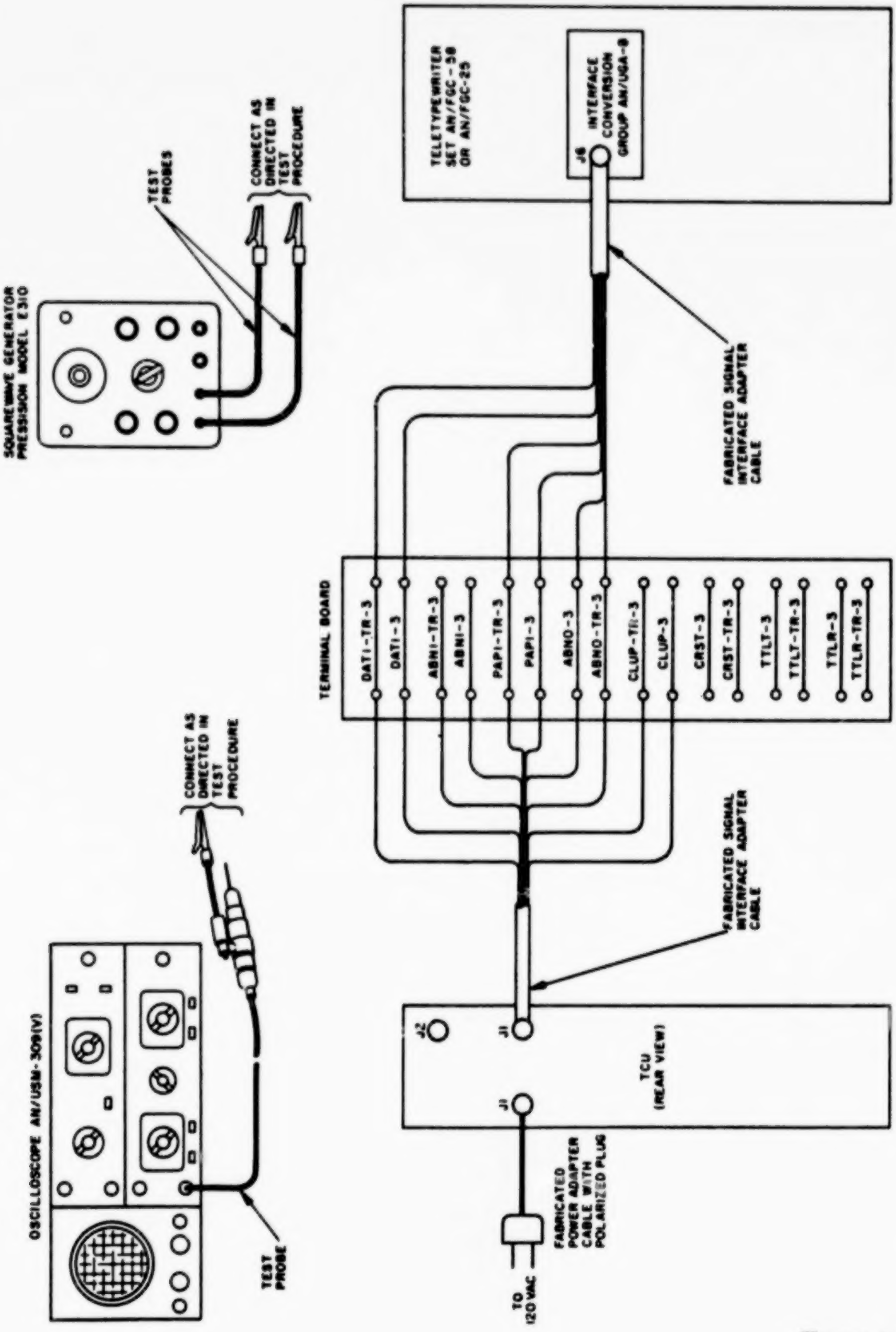

SQUAREWAVE GENERATOR PRESSISSION MODEL E310
TEST PROBES
CONNECT AS DIRECTED IN TEST PROCEDURE
TELETYPEWRITER SET AN/FGC-38 OR AN/FGC-25
J6
INTERFACE CONVERSION GROUP AN/UGA-8
TM5895-438-35-404
FABRICATED SIGNAL INTERFACE ADAPTER CABLE
TERMINAL BOARD
DATI-TR-3
DATI-3
ABNI-TR-3
ABNI-3
PAPI-TR-3
PAPI-3
ABNO-3
ABNO-TR-3
CLUP-TR-3
CLUP-3
CRST-3
CRST-TR-3
TTLT-3
TTLT-TR-3
TTLR-3
TTLR-TR-3
CONNECT AS DIRECTED IN TEST PROCEDURE
FABRICATED SIGNAL INTERFACE ADAPTER CABLE
OSCILLOSCOPE AN/USM-309(V)
TEST PROBE
J2
J11
J1
TCU (REAR VIEW)
FABRICATED POWER ADAPTER CABLE WITH POLARIZED PLUG
TO 120 VAC

Figure 3-33. Crypto circuitry test setup.

c. *Test Procedure.*

Step No.	Test procedure	Performance standard
	Note: TCU power supply must be strapped for 120 vac for this test. Procedure for strapping TCU is given in TM 11-5815-335-12. Preliminary test conditions: *a*. Turn on square wave generator and oscilloscope and allow 15-minute warmup period. *b*. Connect 600-ohm resistor across output terminals of square wave generator. *c*. Set square wave generator controls as follows: (1) RANGE TO X 1. (2) AMPLITUDE (output) to zero. (3) FREQUENCY dial to 10 cps. *d*. Set oscilloscope controls as follows: (1) FUNCTION switch to A.	

Step No.	Test procedure	Performance standard
	(2) SENSITIVITY (CHANNEL A) to .2V/CM. (3) SWEEP TIME to 20 MILLISECONDS/CM. (4) TRIGGER SOURCE to INT+ *e*. Set TCU control inditor panel controls as follows: (1) MODE switch to TEST. (2) TCU/CRYPTO switch to TCU. (3) STOP AT EOM/CONTINUE switch to CONTINUE. (4) AUTO NO. OFF/ON switch to ON. (5) NUMBER SELECT switches to 000. (6) VOLUME (control) to approximately midposition. *f*. Set TCU simulator test panel controls as follows:	

Step No.	Test procedure	Performance standard
	(1) SPEED SEL switch to 75. (2) RT ENABLE/DISABLE switch to RT ENABLE. (3) Red and black knobs of CON SEQ SIMULATOR switch to OFF. *Note:* All control settings referred to in this test procedure are loacated on control indicator panel unless specifically stated otherwise.	
2	Set TCU power supply AC POWER ON/OFF switch ON. Set teletypewriter switch to ON.	POWER ON, CANCEL XMITTED, and TCU lamps light.
3	Set TCU/CRYPTO switch to CRYPTO.	TCU lamp extinguishes.
4	Connect red lead of square wave generator to CRST-3 lead on terminal board. Connect black lead of square wave generator to CRST-TR-3 lead on terminal board. Connect oscilloscope probe to red lead of square wave generator.	N/A.
5	Adjust square wave generator amplitude control until 10 volts peak-to-peak is observed on oscilloscope. Adjust square wave generator	N/A.

Step No.	Test procedure	Performance standard
	frequency dial until oscilloscope displays one cycle in 5 cm.	
6	Activate simulator test panel SYS CLR switch.	N/A.
7	Activate START XMIT switch.	CANCEL XMITTED lamp extinguishes. As message is being printed, XMIT IN PROGRESS and RECEIVE IN PROGRESS lamps will light. After four N's in message have printed on printer, XMIT IN PROGRESS and RECEIVE IN PROGRESS lamps should extinguish. Lamps will stay off until message starts again. *Note:* If output signal characteristics, distortion and source impedance test is to be performed, do not disconnect test setup.
8	Set TCU power AC POWER ON/OFF switch to OFF. Place teletypewriter power switch to OFF. Disconnect test setup.	

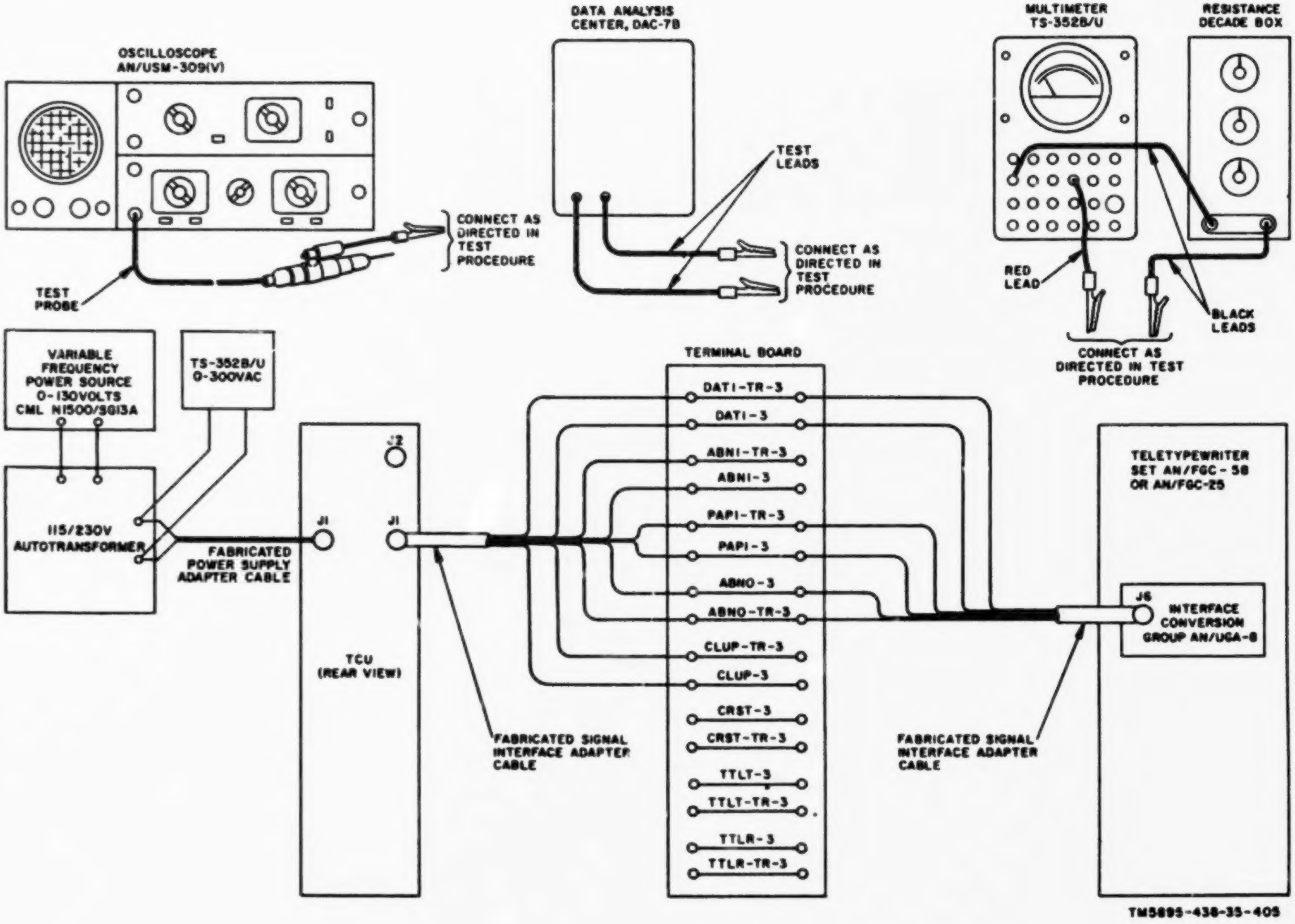

OSCILLOSCOPE
AN/USM-309(V)
TEST PROBE
CONNECT AS DIRECTED IN TEST PROCEDURE
DATA ANALYSIS CENTER, DAC-7B
TEST LEADS
CONNECT AS DIRECTED IN TEST PROCEDURE
MULTIMETER
TS-352B/U
RESISTANCE DECADE BOX
RED LEAD
BLACK LEADS
CONNECT AS DIRECTED IN TEST PROCEDURE
VARIABLE FREQUENCY POWER SOURCE 0-130VOLTS CML N1500/3G13A
TS-352B/U 0-300VAC
115/230V AUTOTRANSFORMER
FABRICATED POWER SUPPLY ADAPTER CABLE
J2
J1
J1
TCU (REAR VIEW)
FABRICATED SIGNAL INTERFACE ADAPTER CABLE
TERMINAL BOARD
DATI-TR-3
DATI-3
ABNI-TR-3
ABNI-3
PAPI-TR-3
PAPI-3
ABNO-3
ABNO-TR-3
CLUP-TR-3
CLUP-3
CRST-3
CRST-TR-3
TTLT-3
TTLT-TR-3
TTLR-3
TTLR-TR-3
FABRICATED SIGNAL INTERFACE ADAPTER CABLE
TELETYPEWRITER SET AN/FGC-58 OR AN/FGC-25
J6
INTERFACE CONVERSION GROUP AN/UGA-8
TM5895-438-35-405

Figure 3-34. Output signal characteristics, distortion and source impedance test setup.

3-43. Output Signal Characteristics, Distortion and Source Impedance Test

The output signal characteristics, distortion and source impedance test checks the characteristics (amplitude, risetime, falltime) of the output waveforms on TTLT, PAPI, and CLUP lines. The test also checks the distortion on the TTLT and PAPI lines, and the source impedance of the TTLT, PAPI, and CLUP output circuits. The test is performed with the line voltage and frequency adjusted for 96 volts ac, 47.5 cycles per second (cps); 132 volts ac, 63 cps; 217 volts ac, 47.5 cps; and 253 volts ac, 63 cps.

a. Test Equipment and Materials.

(1) Teletypewriter Set AN/FGC-58 or AN/FGC-25.

(2) Interface Conversion Group AN/UGA-8.

(3) Test tapes No. 1 and 2.

(4) Oscilloscope AN/USM-309(V).

(5) Autotransformer 115/230VAC, 500 va.

(6) Data Analysis Center, DAC-7B.

(7) Resistance Decade Box, General Radio Co. Model 1434M.

(8) Variable frequency power source, CML N1500/SG-13A.

(9) Multimeter TS-352B/U (two required).

(10) Signal interface adapter cable (two required).

(11) Power supply adapter cable.

(12) Terminal board (16 double screw contacts).

b. Test Connections and Conditions. Connect the equipment as shown in figure 3-34.

c. ***Test Procedure.***

Step No.	Test procedure	Performance standard
	Note: TCU power supply must be strapped for 120 vac for this test. Procedure for strapping TCU power supply is given in TM 11-5815-335-12.	
1	Turn on variable frequency power source and adjust output for 120 vac, 60 cps. Turn on data analysis center and oscilloscope and allow 15-minute warmup period.	
2	Connect multimeter black lead to one side of resistance decade box, as shown in figure 3-34. Set multimeter to 10-milliampere range. Set resistance decade box controls for 600 ohms.	
3	Set data analysis center controls as follows: *a.* BAUD RATE to 75.0. *b.* UNITS INTERVAL to 7.0. *c.* DISTORTION SELECT to AVG. *d.* AUTO/MAN RESET to the center off position. *e.* FILTER IN/OUT to OUT. *f.* POLARITY PLUS/MINUS to PLUS. *g.* TRANSITION	

Step No.	Test procedure	Performance standard
	SELECT to ALL.	
4	Set TCU control indicator panel controls as follows: *a.* MODE switch to TEST. *b.* TCU CRYPTO switch to TCU. *c.* STOP AT EOM/CONTINUE switch to CONTINUE. *d.* AUTO NO. OFF/ON switch to ON. *e.* NUMBER SELECT switches to 000. *f.* VOLUME control to approximately midposition.	
5	Set TCU simulator test panel controls as follows: *a.* SPEED SEL switch to 75.0. *b.* RT ENABLE/DISABLE switch to DISABLE. *c.* Red and black knobs on CON SEQ SIMULATOR switch to OFF. *Note:* All control settings referred to in this test procedure are located on	

Step No.	Test procedure	Performance standard
	control indicator panel unless specifically stated otherwise.	
6	Set TCU power supply AC POWER ON/OFF switch to ON. Turn on teletypewriter.	POWER ON, CANCEL XMITTED, TEST, and TCU lamps light.
7	Insert test tape No. 1 tape reader.	N/A.
8	Connect oscilloscope probe to CLUP-3 lead on terminal board.	Oscilloscope indicates -6.0-volt dc level ±1.0.
9	Connect black lead of resistance decade box to CLUP-3 lead, and connect red lead of multimeter to CLUP-TR-3 lead on terminal board. Vary resistance of resistance decade box (begin with lowest resistance scale) until multimeter reads 10 milliamperes.	Oscilloscope indicates -6.0-volt dc level ±1.0.
10	Disconnect test leads from CLUP-3 and CLUP-TR-3 terminals on terminal board.	N/A
11	Activate TCU control indicator panel START XMIT switch.	CANCEL XMITTED lamp extinguishes, and XMIT IN PROGRESS and RECEIVE IN PROGRESS lamps light on control indicator panel. Test tape No. 1 is printed out on teletypewriter.
12	Adjust oscilloscope to read +6-volt dc level, and connect oscilloscope probe to CLUP-3 lead on terminal board.	Oscilloscope indicates +6.0-volt dc level ±1.0. Record voltage level obtained.
13	Connect red lead of multimeter to	Oscilloscope indicates dc level

Step No.	Test procedure	Performance standard
	CLUP-3 lead, and black lead of resistance decade box to CLUP-TR-3 lead on terminal board. Vary resistance of resistance decade box (begin with lowest resistance scale) until multimeter reads 10 milliampres.	that is ±1.0 volts dc of reading obtained in step 9 above.
14	Determine source impedance of CLUP-3 line by using following formula: $\frac{E_{NL} - E_L}{10 \text{ ma}}$ = source impedance in ohms. E_{NL} = voltage of CLUP-3 line without a load. Use reading obtained in steps 12 above. E_L = voltage of CLUP-3 line with a load. Use reading obtained in step 13 above. 10 ma = 0.01.	
15	Activate control indicator panel XMIT CANCEL switch. After 5 seconds, place MODE switch at NORMAL.	CANCEL XMITTED lamp lights, and XMIT IN PROGRESS lamp extinguishes. After 5 seconds, TEST lamp extinguishes, and NORMAL lamp lights.
16	Connect oscilloscope probe to TTLT-3 lead on terminal board.	Oscilloscope indicates +6.0-volt dc ±1.0. Record voltage level obtained.
17	Connect red lead of multimeter to TTLT-3 lead, and black lead of re-	Oscilloscope indicates dc level that is ±1.0 volts dc of reading

Step No.	Test procedure	Performance standard
	sistance decade box to TTLT-TR-3 lead on terminal board. Vary resistance decade box (begin with lowest resistance scale) until multimeter reads 10 milliamperes.	obtained in step 16 above.
18	Determine source impedance of TTLT-3 line by using following formula: $\frac{E_{NL} - E_L}{10\text{ ma.}}$ = source impedance in ohms. E_{NL} = Reading obtained in step 16 above. E_L = Reading obtained in step 17 above.	Source impedance calculated is less than 100 ohms.
19	Connect oscilloscope probe to PAPI-3 lead on terminal board.	Oscilloscope indicates +6.0-volt dc ±1.0. Record voltage level obtained.
20	Connect red lead of multimeter to PAPI-3 lead, and black lead of resistance decade box to PAPI-TR-3 lead on terminal board. Vary resistance decade box (begin with lowest resistance scale) until multimeter reads 10 milliamperes.	Oscilloscope indicates dc level that is ±1.0 volts dc of reading obtained in step 19 above.
21	Determine source impedance of PAPI-3 line by using following formula: $\frac{E_{NL} - E_L}{10\text{ ma.}}$ = source impedance in ohms.	Source impedance calculated is less than 100 ohms.

Step No.	Test procedure	Performance standard
	E_{NL} = Reading obtained in step 19 above. E_L = Reading obtained in step 20 above.	
22	Disconnect test leads from CLUP-3 and CLUP-TR-3 terminals on terminal board.	N/A
23	Turn control indicator panel MODE switch to TEST. Activate simulator test panel SYS CLR switch.	TEST lamp lights, and NORMAL lamp extinguishes.
24	Activate control indicator panel START XMIT switch. After 5 seconds, turn MODE switch to NORMAL.	CANCEL XMITTED lamp extinguishes, and XMIT IN PROGRESS and RECEIVE IN PROGRESS lamps light. Test tape No. 1 is printed out on teletypewriter. After 5 seconds, TEST lamp extinguishes, and NORMAL lamp lights.
25	Connect oscilloscope probe to TTLT-3 lead on terminal board.	Oscilloscope displays 12-volt peak-to-peak signal ±2.0 volts.
26	Connect DAS-10 probe to TTLT-3 lead on terminal board and adjust DAS-10 VFO knob to obtain lowest distortion reading possible.	DAS-10 meter indicates less than 2% distortion.
27	Turn control indicator panel MODE switch to TEST.	NORMAL lamp extinguishes, and TEST lamp lights.
28	Connect oscilloscope probe to PAPI-3 lead on terminal board.	Oscilloscope displays 12-volt peak-to-peak signal ±2.0 volts.

Step No.	Test procedure	Performance standard
29	Connect DAS-10 probe to PAPI-3 lead on terminal board, and adjust DAS-10 VFO knob to obtain lowest distortion reading possible.	DAS-10 meter indicates less than 2% distortion.
30	Activate control indicator panel XMIT CANCEL switch.	XMIT IN PROGRESS and RECEIVE IN PROGRESS lamps extinguish, and CANCEL XMITTED lamp lights.
31	Insert test tape No. 2 in tape reader.	N/A.
32	Activate control indicator panel START XMIT switch.	Same as step 11 above.
33	Connect oscilloscope probe to PAPI-3 lead on terminal board, and adjust oscilloscope controls to display character B.	Fig. 3-35.
34	Adjust oscilloscope controls to display first bit of character B, and measure risetime of pulse between 10% and 90% point of bit.	0.665 to 1.8 ms. Refer to figure 3-35.
35	Measure falltime of same bit between 10% and 90% points.	0.665 to 1.8 ms. Refer to figure 3-35.
36	Turn control indicator panel MODE switch to NORMAL.	TEST lamp extinguishes, and NORMAL lamp lights.
37	Connect oscilloscope probe to TTLT-3 lead on terminal board, and adjust oscilloscope controls to display character B.	Fig. 3-35.
38	Adjust oscilloscope controls to display first bit of character B, and measure risetime	0.665 to 1.8 ms. Refer to figure 3-35.

Step No.	Test procedure	Performance standard
	of pulse between 10% and 90% point of bit.	
39	Measure falltime of same bit between 10% and 90% points.	0.665 to 1.8 ms. Refer to figure 3-35.
40	Adjust variable frequency power source to deliver 96-volt ac, 47.5-cps output.	N/A.
41	Repeat steps 7 through 39 above.	
42	Adjust variable frequency power source to deliver 132-volt ac, 63-cps output.	N/A.
	Warning: Before performing step 44 below, remove all ac power from TCU.	
43	Repeat steps 7 through 39 above.	
44	To perform following steps, TCU power supply must be strapped for 230 volts ac. Procedure for strapping TCU power supply is given in TM 11-5815-335-12.	
45	Adjust variable frequency power source to deliver 213-volt ac, 47.5-cps output and repeat steps 6 through 39 above.	
46	Adjust variable frequency power source to deliver 253-volt ac, 63-cps output and repeat steps 6 through 39 above.	
47	Disconnect test setup.	

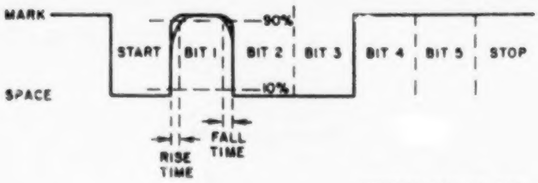

MARK
SPACE
START
BIT 1
BIT 2
BIT 3
BIT 4
BIT 5
STOP
90%
10%
RISE TIME
FALL TIME

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Figure 3-35. Character B.

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MAPS
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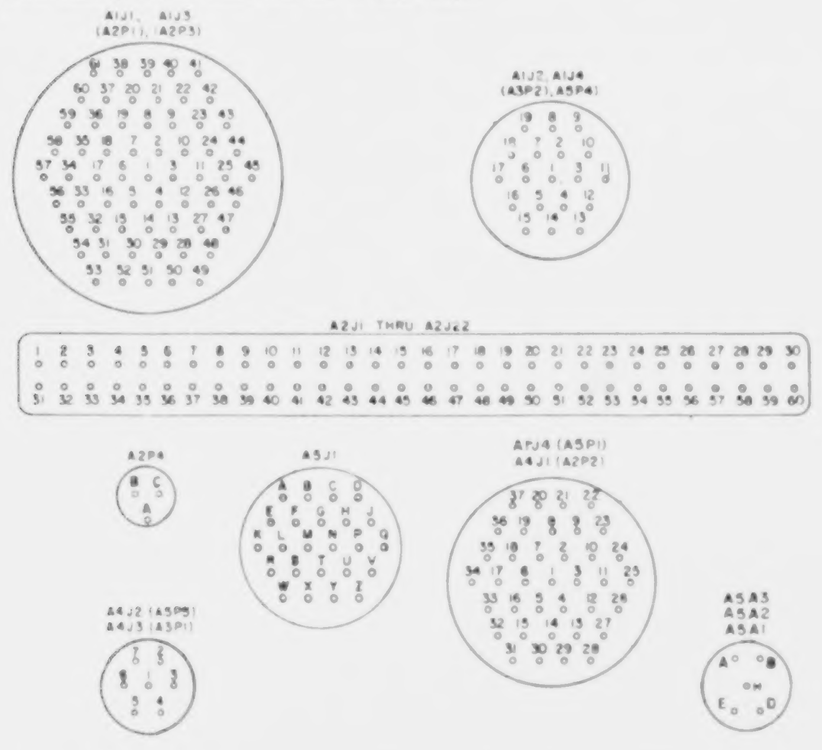
NOTES

1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS AND CAPACITANCES ARE IN MICROFARADS
2. ▭ INDICATES EQUIPMENT MARKING
3. ⏚ INDICATES CHASSIS GROUND. ALL OTHER GROUNDS ARE POWER OR SIGNAL GROUND
4. REFERENCE DESIGNATIONS ARE ABBREVIATED WITHIN EACH ASSEMBLY. PREFIX EACH REFERENCE DESIGNATION WITH THE APPLICABLE ASSEMBLY DESIGNATION
5. WAFER SWITCHES SHOWN IN EXTREME COUNTERCLOCKWISE POSITION AND ARE VIEWED FROM FRONT, EXCEPT AS OTHERWISE INDICATED. FRONT OF WAFER IS SIDE TOWARD CONTROL KNOB. WAFER NEAREST CONTROL KNOB IS SECTION A. SEGMENTS ON WAFERS ARE IDENTIFIED BY X, Y, Z
6. PIN ARRANGEMENTS ON CONNECTORS ARE AS SHOWN BELOW


A1J1, A1J3
(A2P1, A2P3)
A1J2, A1J4
(A3P2), A5P4)
A2J1 THRU A2J22
A2P4
A3J1
A1J5 (A5P1)
A4J1 (A2P5)
A4J2 (A5P5)
A4J3 (A3P1)
A5A3
A5A2
A5A1

7. TERMINAL NUMBERS SUCH AS 4-4 SHOWN ON WIRES INDICATE CONNECTION POINT PRIOR TO INTERNAL STRAPPING
8. THE WIRING SHOWN APPLIES WHEN THE ABNI AND ABNO SIGNALS ARE RECEIVED FROM A CONTACT CLOSURE. WHEN THE ABNI AND ABNO SIGNALS ARE RECEIVED FROM A ±6 VOLT SOURCE, CHANGE THE WIRING OF A1A1A3 AS FOLLOWS

CONNECT	DISCONNECT
5 TO 6	1 FROM 3
17 TO 18	13 FROM 15
	6 FROM 10
	18 FROM 22
	5 FROM 11
	17 FROM 11

9. LOGIC CARDS 2A1, 2A2, 2A3 (WHEN EQUIPPED) OCCUPY LOGIC RACK POSITIONS 1A2A20, 1A2A21 AND 1A2A13 RESPECTIVELY
10. PRECEDE REFERENCE DESIGNATIONS OF ALL CONNECTORS WITH UNIT DESIGNATOR 1

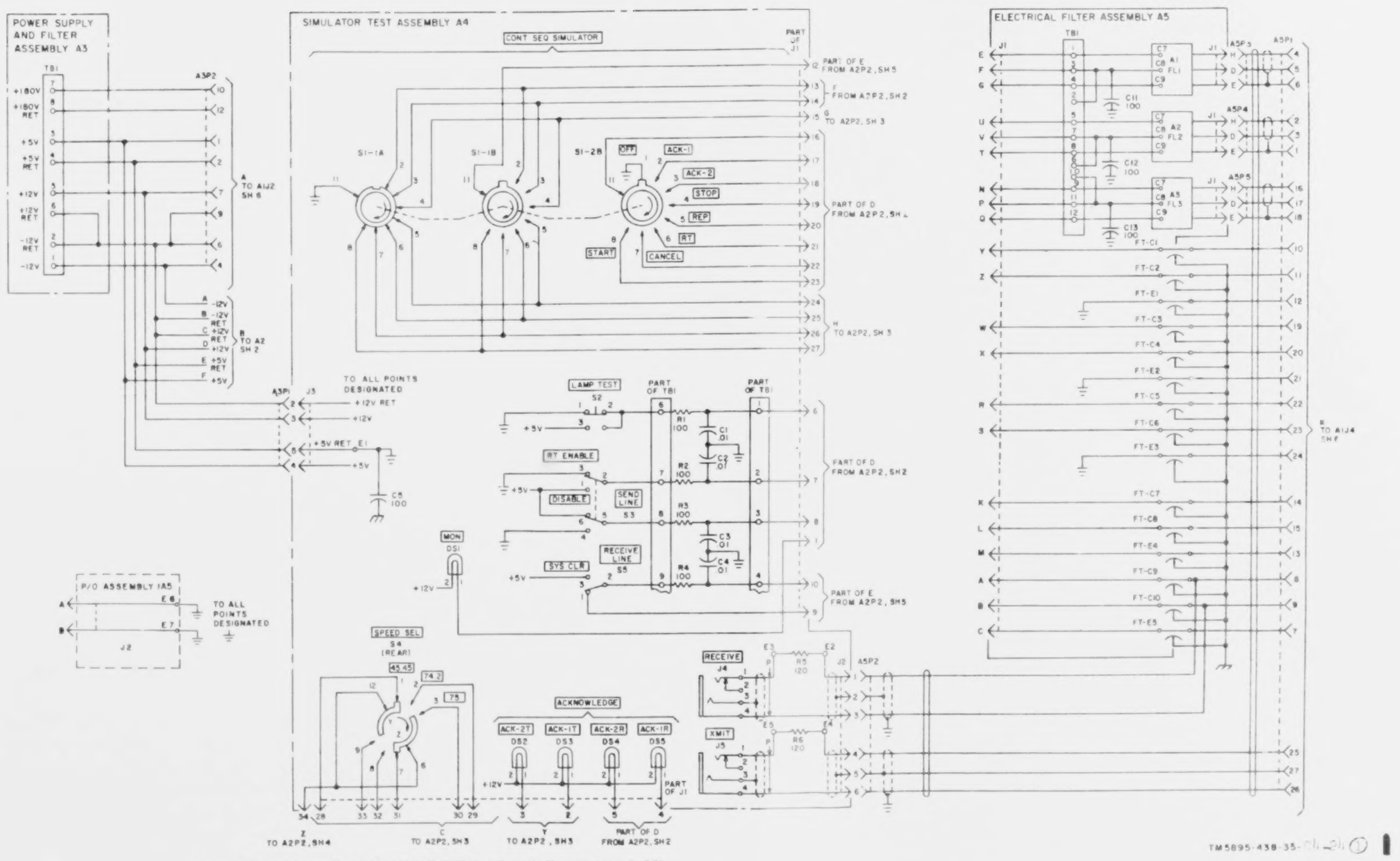

POWER SUPPLY AND FILTER ASSEMBLY A3
TB1
+180V
+180V RET
+5V
+5V RET
+12V
+12V RET
-12V RET
-12V
A3P2
TO A1J2 SH 6
TO A2 SH 2
TO ALL POINTS DESIGNATED
I/O ASSEMBLY A6
TO ALL POINTS DESIGNATED
SIMULATOR TEST ASSEMBLY A4
CONT SEQ SIMULATOR
S1-1A
S1-1B
S1-2B
OFF
ACK-1
ACK-2
STOP
REP
ST
START
CANCEL
PART OF J1
PART OF E FROM A2P2, SH 5
FROM A2P2, SH 2
TO A2P2, SH 3
PART OF D FROM A2P2, SH 4
TO A2P2, SH 5
LAMP TEST
PART OF TB1
ST ENABLE
DISABLE
SEND LINE
RECEIVE LINE
SYS CLR
MON
DS1
PART OF D FROM A2P2, SH 2
PART OF E FROM A2P2, SH 5
SPEED SEL
S4 (REAR)
ACKNOWLEDGE
ACK-2T
ACK-1T
ACK-2R
ACK-1R
DS2
DS3
DS4
DS5
RECEIVE
J4
XMIT
J5
R5 120
R6 120
Z TO A2P2, SH4
C TO A2P2, SH3
Y TO A2P2, SH3
PART OF D FROM A2P2, SH2
ELECTRICAL FILTER ASSEMBLY A5
TB1
A1 FL1
A2 FL2
A3 FL3
C11 100
C12 100
C13 100
A5P3
A5P4
A5P5
A5P1
TO A1J4 (H) P

Figure 1-3①. Teletypewriter Control Unit C-7050/G, schematic diagram (part 1 of 6).

TM5895-438-35-C4-24①

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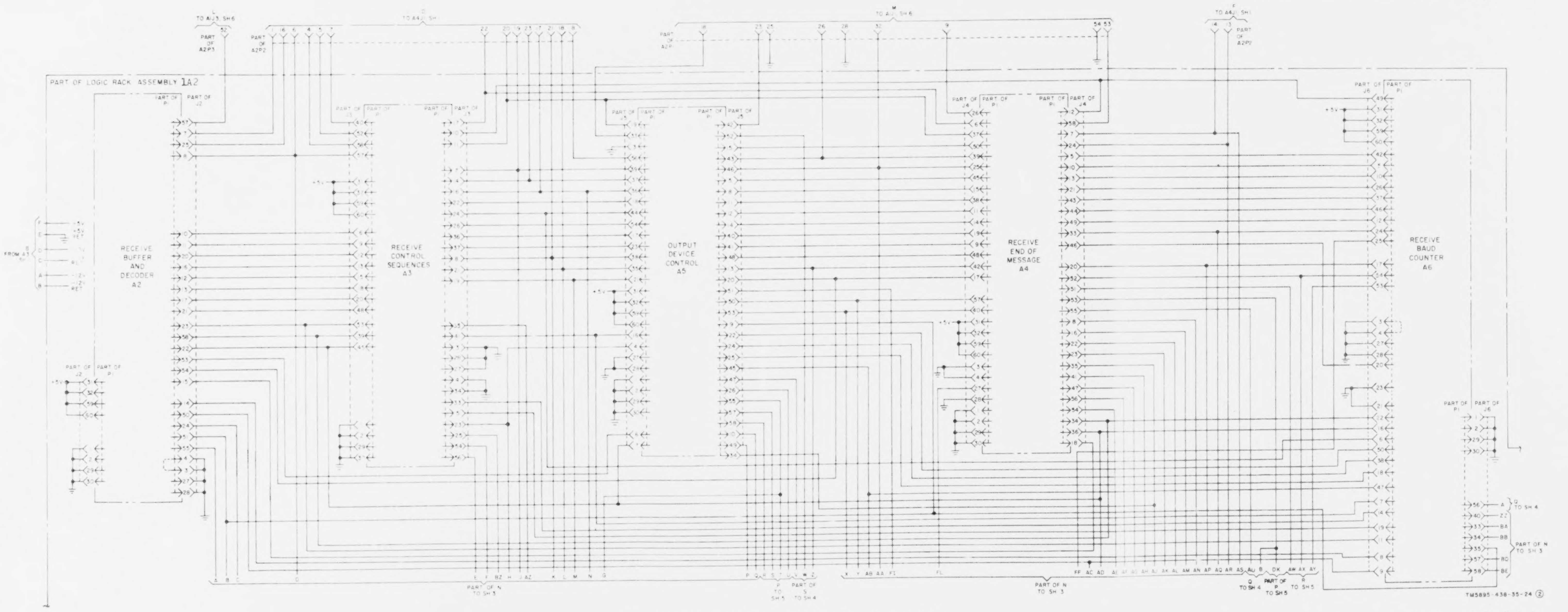

PART OF LOGIC RACK ASSEMBLY 1A2
RECEIVE BUFFER AND DECODER A2
RECEIVE CONTROL SEQUENCES A3
OUTPUT DEVICE CONTROL A5
RECEIVE END OF MESSAGE A4
RECEIVE BAUD COUNTER A6
FROM
PART OF N TO SH 3
PART OF N TO SH 3
Q TO SH 4
PART OF P TO SH 5
R TO SH 5
P TO SH 5
PART OF S TO SH 4
TM5895-438-35-24 ②

Figure 1-3②. Teletypewriter Control Unit C-7050/G, schematic diagram (part 2 of 6).

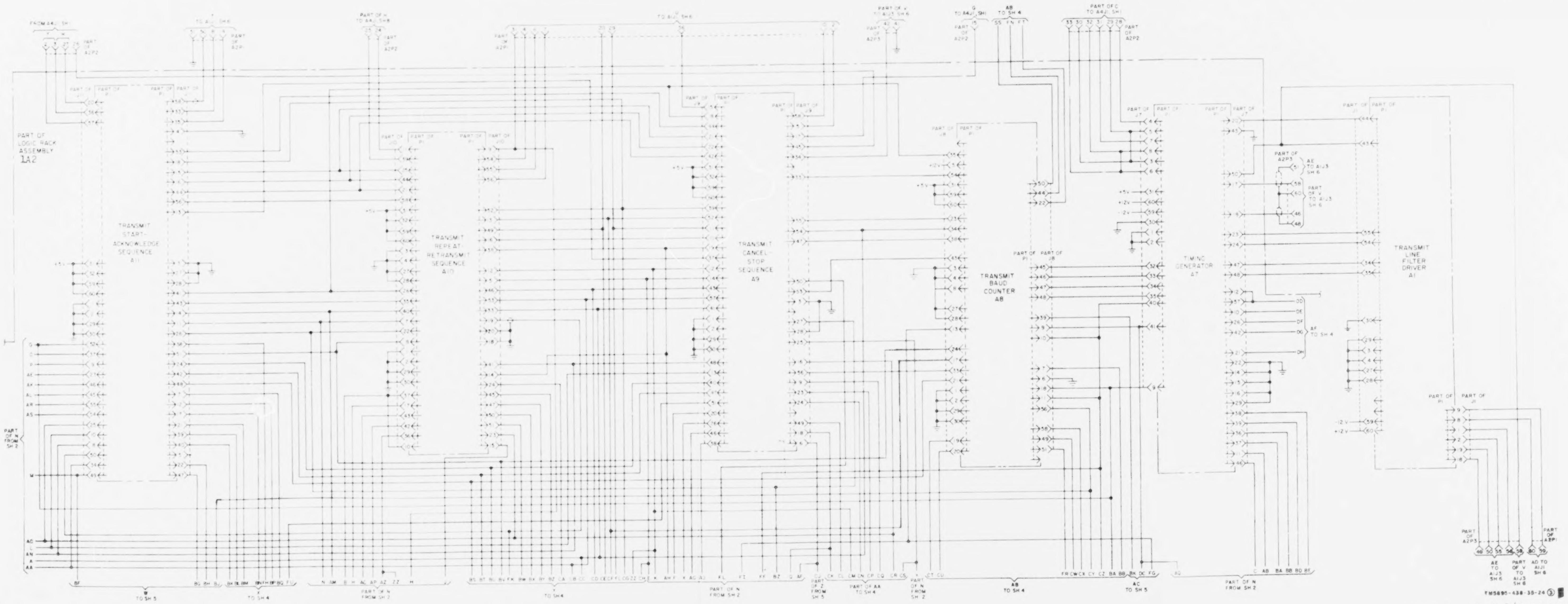
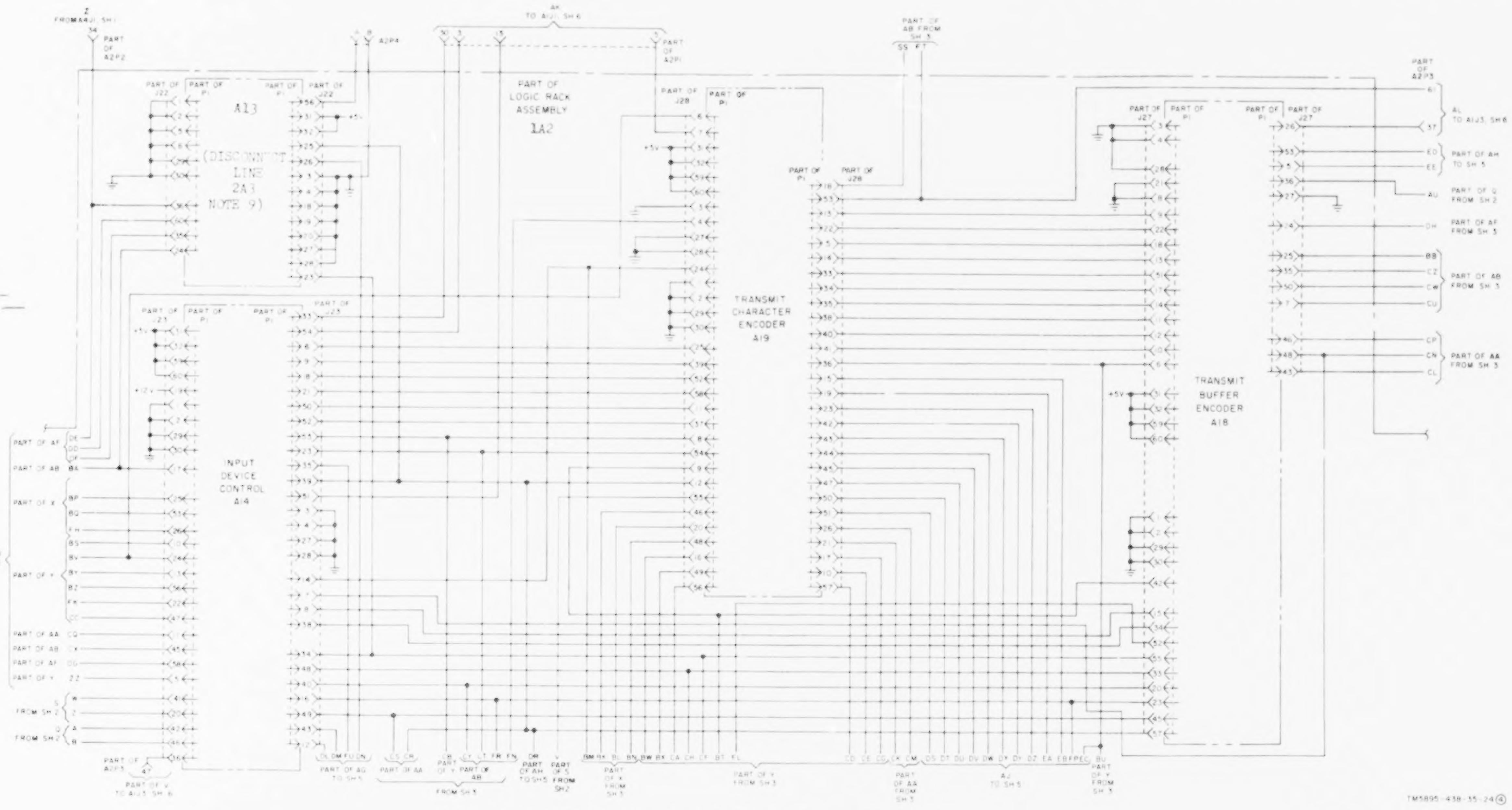

PART OF LOGIC RACK ASSEMBLY 1A2
TRANSMIT START ACKNOWLEDGE SEQUENCE A11
TRANSMIT REPEAT RETRANSMIT SEQUENCE A10
TRANSMIT CANCEL STOP SEQUENCE A9
TRANSMIT BAUD COUNTER A8
TIMING GENERATOR A7
TRANSMIT LINE FILTER DRIVER A1
TO SH 4
TO SH 5
PART OF N FROM SH 2
PART OF AA TO SH 4
AB TO SH 4
AC TO SH 5
TM5895-438-35-24

Figure 1-35. Teletypewriter Control Unit C-7050/G, schematic diagram (part 3 of 6).


A13
PART OF LOGIC RACK ASSEMBLY
1A2
TRANSMIT CHARACTER ENCODER
A19
INPUT DEVICE CONTROL
A14
TRANSMIT BUFFER ENCODER
A18
PART OF J22
PART OF P1
PART OF J28
PART OF J27
PART OF A2P3
AL TO A1J3, SH 6
FROM SH 3
PART OF AT
PART OF AB
PART OF X
PART OF Y
PART OF AA
PART OF AB
PART OF AF
PART OF Y
FROM SH 2
PART OF AH TO SH 5
PART OF S FROM SH2
PART OF X FROM SH 3
PART OF Y FROM SH 3
PART OF AA FROM SH 3
AJ TO SH 5
PART OF Y FROM SH 3

TM5895-438-35-24④

Figure 1-8④. Teletypewriter Control Unit C-7050/G, schematic diagram (part 4 of 6).

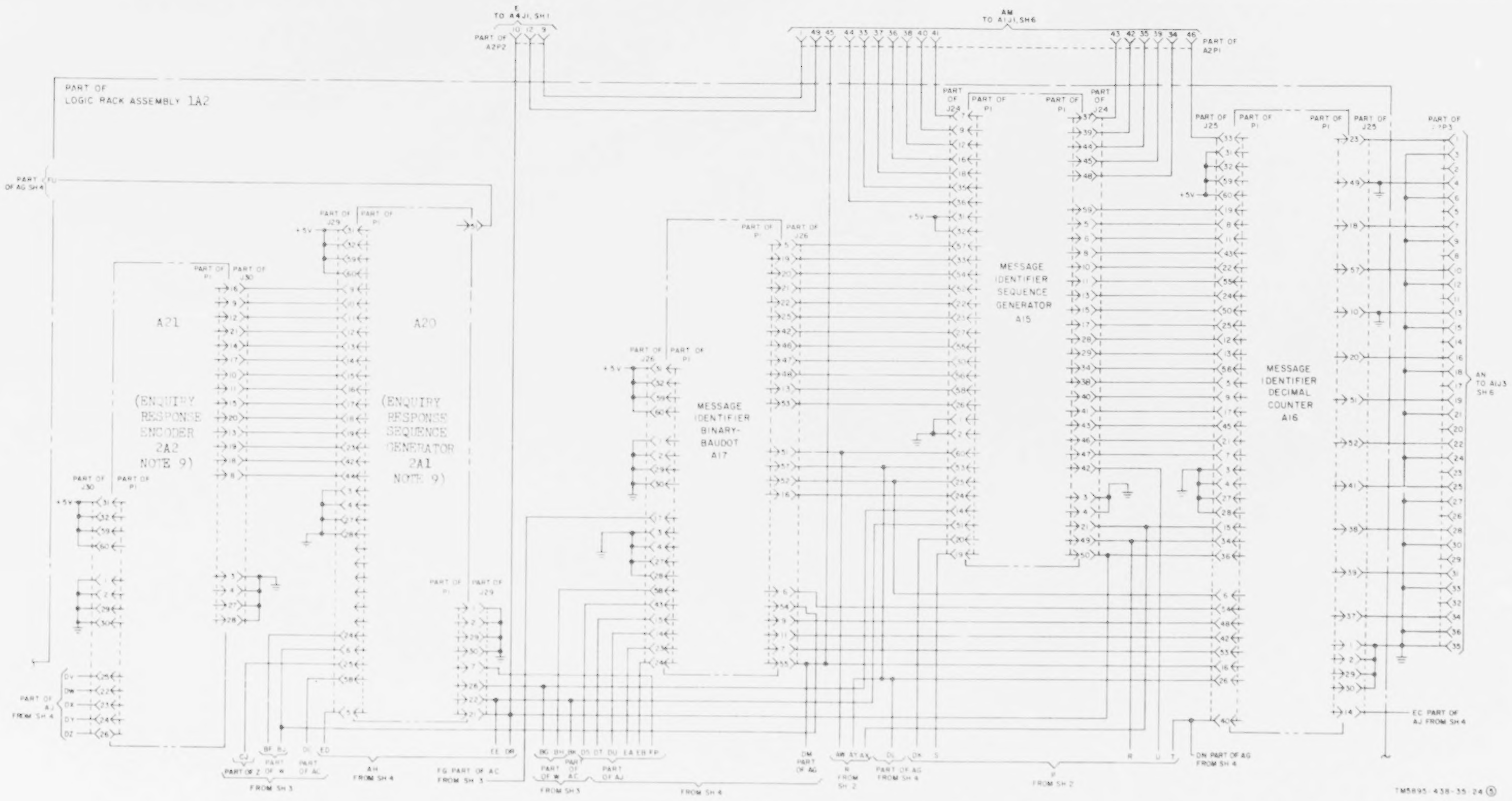

PART OF LOGIC RACK ASSEMBLY 1A2
A21
(ENQUIRY RESPONSE ENCODER 2A2 NOTE 9)
A20
(ENQUIRY RESPONSE SEQUENCE GENERATOR 2A1 NOTE 9)
MESSAGE IDENTIFIER BINARY-BAUDOT A17
MESSAGE IDENTIFIER SEQUENCE GENERATOR A15
MESSAGE IDENTIFIER DECIMAL COUNTER A16
PART OF A2P1
EC PART OF AJ FROM SH 4
DN PART OF AG FROM SH 4
FROM SH 3
FROM SH 4
FROM SH 2
TM5895-438-35-24 ⑤

Figure 1-3⑤. Teletypewriter Control Unit C-7050/G, schematic diagram (part 5 of 6).

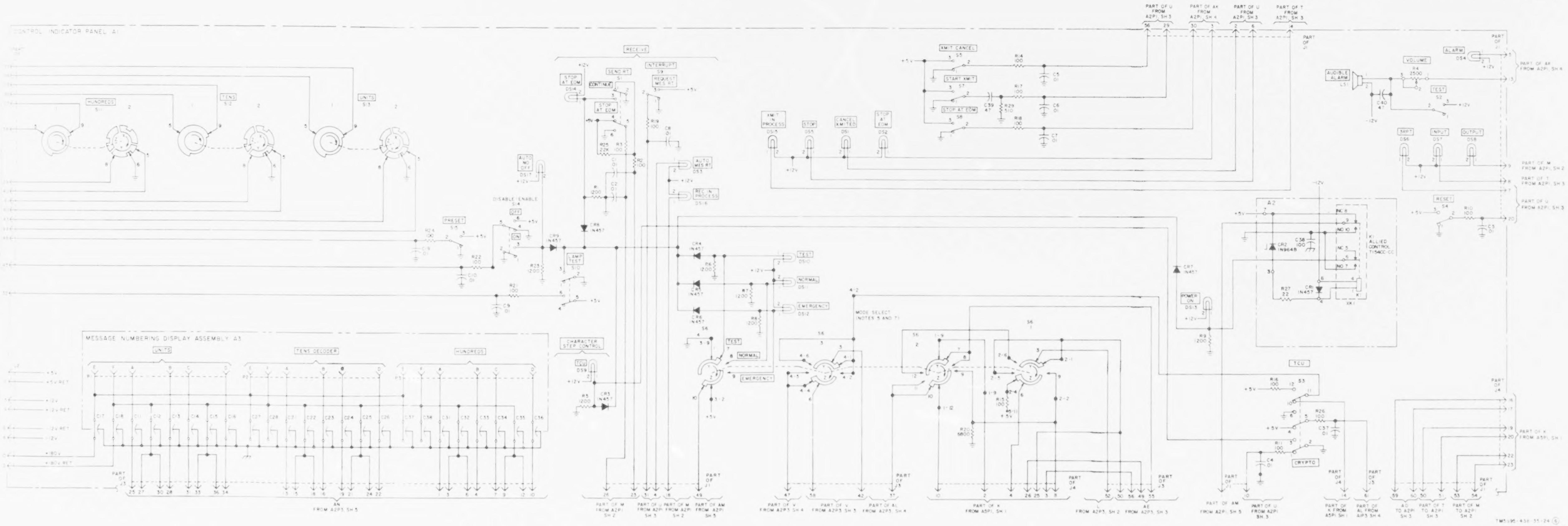
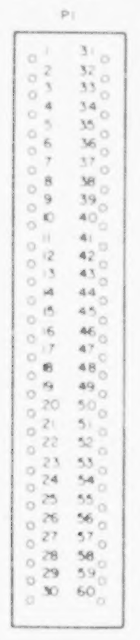

CONTROL INDICATOR PANEL A1
HUNDREDS
TENS
UNITS
PRESET
DISABLE ENABLE
RECEIVE
INTERRUPT
CONTINUE
STOP AT EOM
XMIT CANCEL
START XMIT
XMIT IN PROCESS
AUDIBLE ALARM
VOLUME
ALARM
TEST
RESET
POWER ON
NORMAL
EMERGENCY
MODE SELECT (NOTES 5 AND 7)
CHARACTER STEP CONTROL
MESSAGE NUMBERING DISPLAY ASSEMBLY A3
TENS DECODER
TCU
CRYPTO
PART OF M FROM A2P1 SH 2
PART OF AM FROM A2P1 SH 5
PART OF V FROM A2P3 SH 4
PART OF AL FROM A2P3 SH 4
PART OF K FROM A5P1 SH 1
TM5895-436-35-24 ⑥

Figure 1-3⑥. Teletypewriter Control Unit C-7050/G, schematic diagram (part 6 of 6).

NOTES

1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS. CAPACITANCES ARE IN UF.
2. IDENTIFICATION NUMBERS SHOWN WITHIN LOGIC SYMBOLS ALSO ESTABLISH PHYSICAL LOCATION ON EACH PRINTED WIRING BOARD ASSEMBLY. ALL PRINTED WIRING BOARD ASSEMBLIES LOCATE NUMBER 1 IN UPPER LEFT (CONTACT FINGER END) WITH NUMBER 25 IN LOWER RIGHT OF THE ITEM.
3. LOGIC ELEMENT TERMINALS ARE NUMBERED COUNTERCLOCKWISE FROM 1 THROUGH 10 WHEN VIEWED FROM THE TOP. TERMINAL 10 COINCIDES WITH THE KEY.
4. TERMINAL 1 IS GROUND AND TERMINAL 6 IS +5VOLTS ON ALL LOGIC ELEMENTS.
5. LOGIC CAN POSITIONS 1,6,11,16,19,20,21,22 ARE NOT USED.
6. RECEPTACLE VIEWED FROM PIN SIDE.


P1
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
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28
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7. GUARD CONDUCTOR NOT CONNECTED TO ANY CIRCUIT ELEMENTS.
8. SPRAGUE ELECTRIC TYPE NO. TN-56.

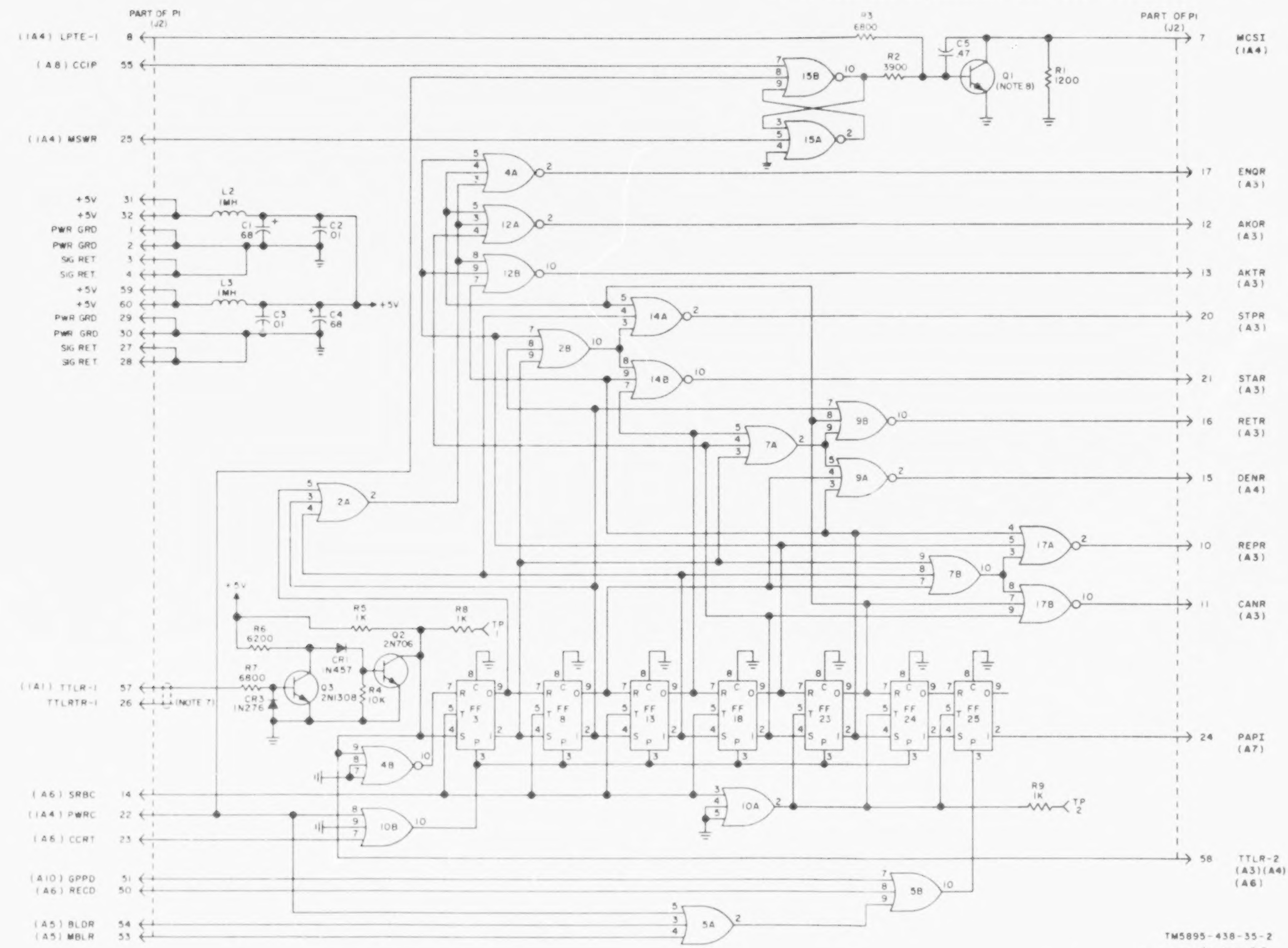

PART OF P1 (J2)
(1A4) LPTE-1 8
(A8) CCIP 55
(1A4) MSWR 25
+5V 31
+5V 32
PWR GRD 1
PWR GRD 2
SIG RET 3
SIG RET 4
+5V 59
+5V 60
PWR GRD 29
PWR GRD 30
SIG RET 27
SIG RET 28
L2 1MH
L3 1MH
C1 68
C2 .01
C3 .01
C4 68
+5V
R3 6800
R2 3900
C5 .47
Q1 (NOTE 8)
R1 1200
15B
15A
4A
12A
12B
14A
14B
2B
2A
7A
9B
9A
17A
7B
17B
+5V
R5 1K
R8 1K
TP 1
R6 6200
R7 6800
CR1 1N457
Q2 2N706
Q3 2N1308
R4 10K
CR3 1N276
(1A1) TTLR-1 57
TTLRTR-1 26
(NOTE 7)
FF 3
FF 8
FF 13
FF 18
FF 23
FF 24
FF 25
4B
10B
10A
R9 1K
TP 2
5B
5A
(A6) SRBC 14
(1A4) PWRC 22
(A6) CCRT 23
(A10) GPPD 51
(A6) RECD 50
(A5) BLDR 54
(A5) MBLR 53
PART OF P1 (J2)
7 MCSI (1A4)
17 ENQR (A3)
12 AKOR (A3)
13 AKTR (A3)
20 STPR (A3)
21 STAR (A3)
16 RETR (A3)
15 DENR (A4)
10 REPR (A3)
11 CANR (A3)
24 PAPI (A7)
58 TTLR-2 (A3)(A4) (A6)
TM5895-438-35-2

Figure 1-4. 1A2A2, Receive Buffer-Decoder FL-1139/G, schematic diagram.

NOTES

1 UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UF

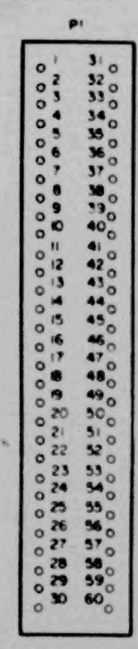
2 IDENTIFICATION NUMBERS SHOWN WITHIN LOGIC SYMBOLS ALSO ESTABLISH PHYSICAL LOCATION ON EACH PRINTED WIRING BOARD ASSEMBLY ALL PRINTED WIRING BOARD ASSEMBLIES LOCATE NUMBER 1 IN UPPER LEFT (CONTACT FINGER END) WITH NUMBER 25 IN LOWER RIGHT OF THE ITEM

3 LOGIC ELEMENT TERMINALS ARE NUMBERED COUNTERCLOCKWISE FROM 1 THROUGH 10 WHEN VIEWED FROM THE TOP TERMINAL 10 COINCIDES WITH THE KEY

4 TERMINAL 1 IS GROUND AND TERMINAL 6 IS +5VOLTS ON ALL LOGIC ELEMENTS

5 LOGIC CAN POSITIONS 4,5,10,14 ARE NOT USED

6 RECEPTACLE VIEWED FROM PIN SIDE


P1
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30
31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60

7 GUARD CONNECTOR NOT CONNECTED TO ANY CIRCUIT ELEMENTS

8 SPRAGUE ELECTRIC TYPE NO TN-56

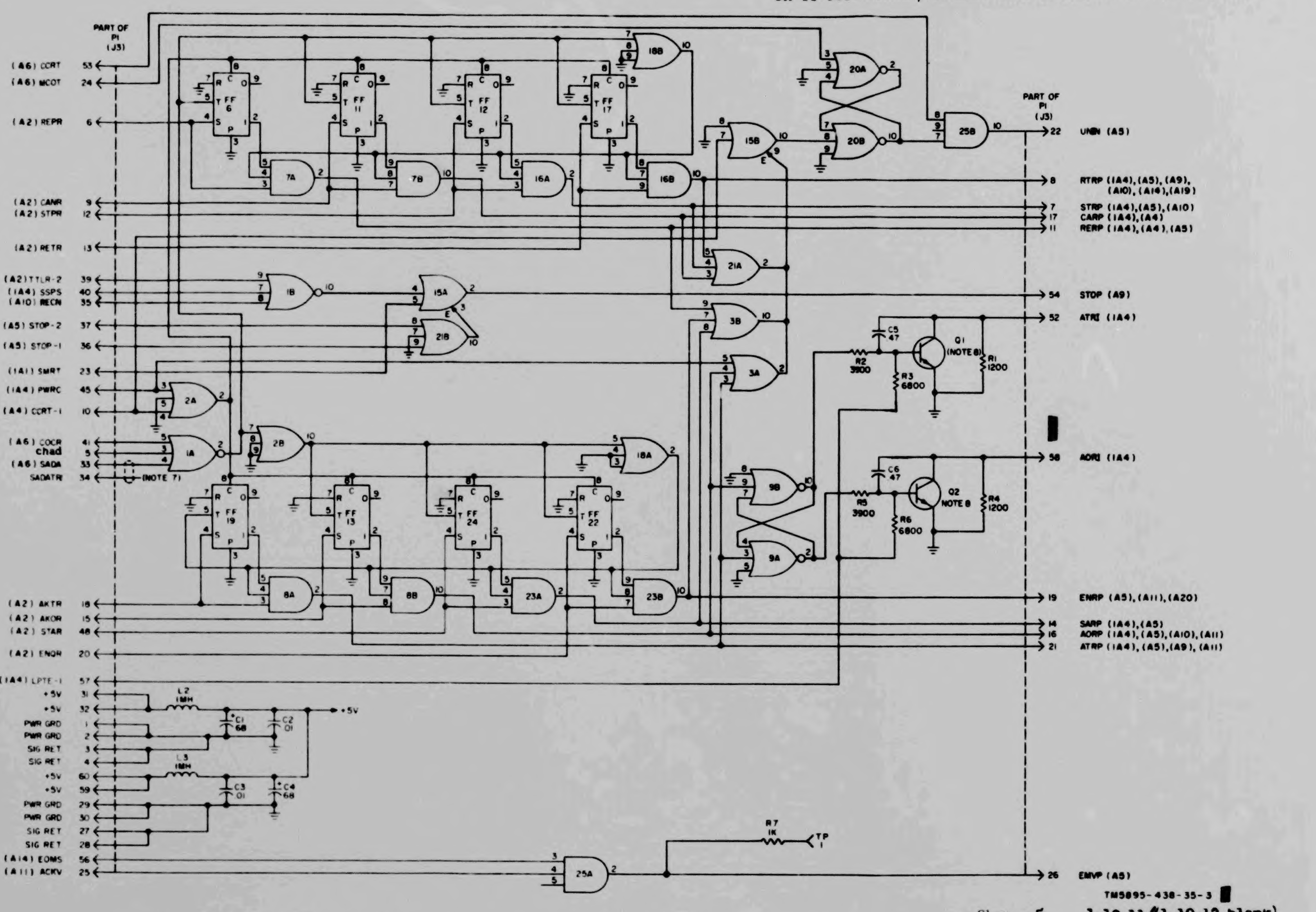

PART OF P1 (J3)
(A6) CCRT 53
(A6) MCOT 24
(A2) REPR 6
(A2) CANR 9
(A2) STPR 12
(A2) RETR 13
(A2) TTLR-2 39
(1A4) SSPS 40
(A10) RECN 35
(A5) STOP-2 37
(A5) STOP-1 36
(1A1) SMRT 23
(1A4) PWRC 45
(A4) CCRT-1 10
(A6) COCR 41
chad 5
(A6) SADA 33
SADATR 34
(NOTE 7)
(A2) AKTR 18
(A2) AKOR 15
(A2) STAR 48
(A2) ENQR 20
(1A4) LPTE-1 57
+5V 31
+5V 32
PWR GRD 1
PWR GRD 2
SIG RET 3
SIG RET 4
+5V 60
+5V 59
PWR GRD 29
PWR GRD 30
SIG RET 27
SIG RET 28
(A14) EOMS 56
(A11) ACKV 25
L2 1MH
L3 1MH
C1
C2
C3 .01
C4 68
+5V
FF 6
FF 11
FF 12
FF 17
FF 19
FF 13
FF 24
FF 22
7A
7B
16A
16B
18B
18A
15B
20A
20B
25B
21A
3B
3A
1B
15A
21B
2A
1A
2B
9B
9A
8A
8B
23A
23B
25A
C5 47
C6 47
R2 3900
R3 6800
R5 3900
R6 6800
Q1 (NOTE 8)
Q2 NOTE 8
R1 1200
R4 1200
R7 1K
TP 1
PART OF P1 (J3)
22 UNEN (A5)
8 RTRP (1A4), (A5), (A9), (A10), (A14), (A19)
7 STRP (1A4), (A5), (A10)
17 CARP (1A4), (A4)
11 RERP (1A4), (A4), (A5)
54 STOP (A9)
52 ATRI (1A4)
58 AORI (1A4)
19 ENRP (A5), (A11), (A20)
14 SARP (1A4), (A5)
16 AORP (1A4), (A5), (A10), (A11)
21 ATRP (1A4), (A5), (A9), (A11)
26 EMVP (A5)
TM5895-438-35-3

Figure 1-5. 1A2A3, Receive Control Sequences PL-1141/G, schematic diagram.

NOTES

1 UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UF

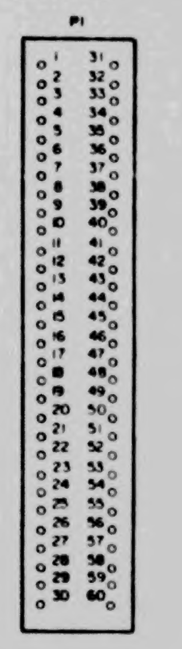
2 IDENTIFICATION NUMBERS SHOWN WITHIN LOGIC SYMBOLS ALSO ESTABLISH PHYSICAL LOCATION ON EACH PRINTED WIRING BOARD ASSEMBLY ALL PRINTED WIRING BOARD ASSEMBLIES LOCATE NUMBER 1 IN UPPER LEFT (CONTACT FINGER END) WITH NUMBER 25 IN LOWER RIGHT OF THE ITEM

3 LOGIC ELEMENT TERMINALS ARE NUMBERED COUNTERCLOCKWISE FROM 1 THROUGH 10 WHEN VIEWED FROM THE TOP TERMINAL 10 COINCIDES WITH THE KEY

4 TERMINAL 1 IS GROUND AND TERMINAL 6 IS +5VOLTS ON ALL LOGIC ELEMENTS

5 LOGIC CAN POSITIONS 10B, 15A, 15B, 21A, 21B, 22A, 22B, 23A, 23B, 24A, 24B 25A, 25B ARE NOT USED

6 RECEPTACLE VIEWED FROM PIN SIDE


P1
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30
31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60

7. SPRAGUE ELECTRIC, TYPE NUMBER TN-56.

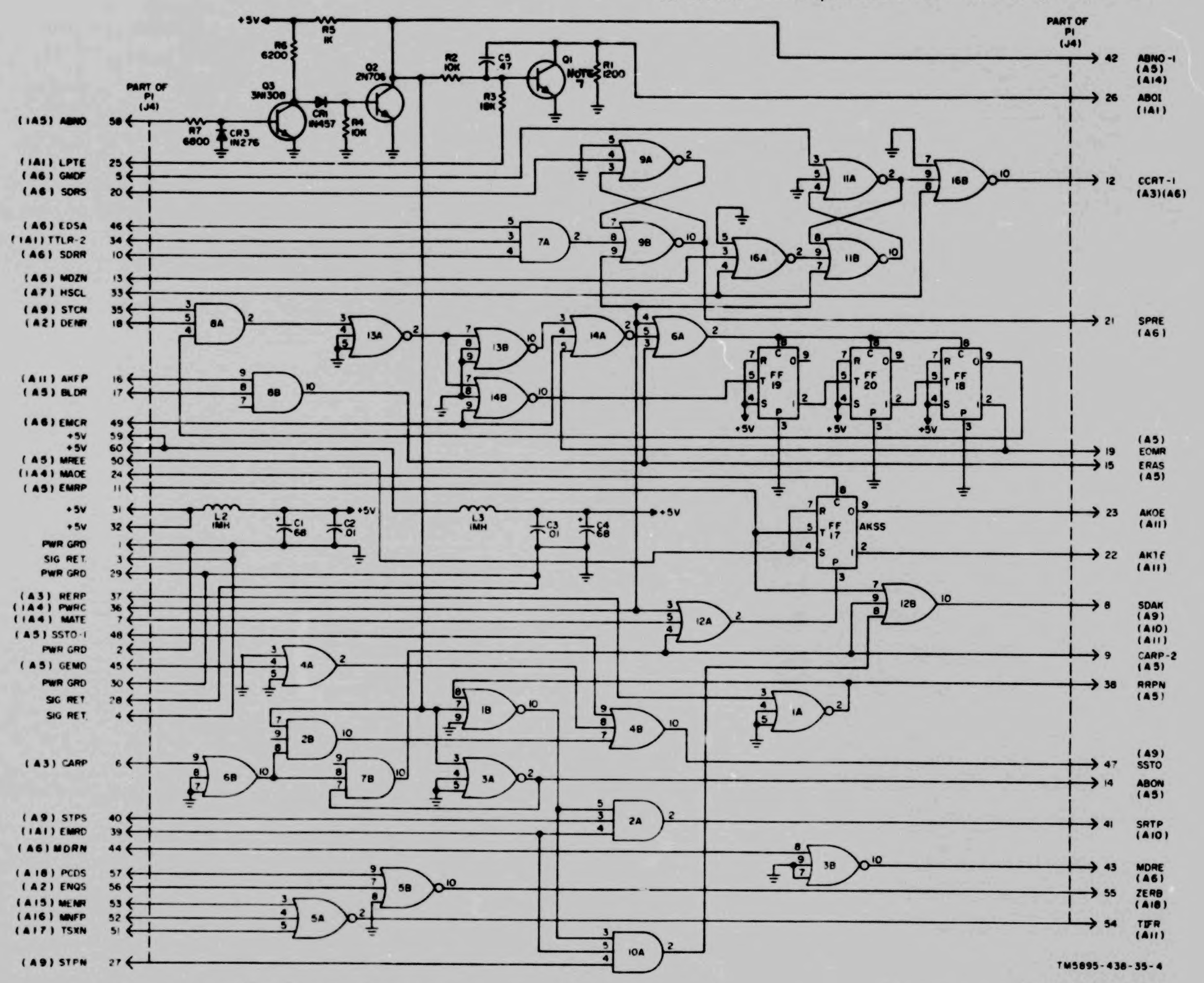
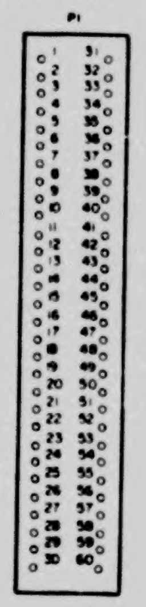

+5V
PART OF P1 (J4)
(A5) ABNO
(1A1) LPTE
(A6) GNDF
(A6) SDRS
(A6) EDSA
(1A1) TTLR-2
(A6) SDRN
(A6) MDZN
(A7) HSCL
(A9) STCN
(A2) DENR
(A11) AKFP
(A5) BLDR
(A6) EMCR
(A5) MREE
(1A4) MAOE
(A5) EMRP
PWR GRD
SIG RET
(A3) CARP
(A9) STPS
(1A1) EMRD
(A6) MDRN
(A18) PCDS
(A2) ENQS
(A15) MENR
(A16) MNFP
(A17) TSXN
(A9) STPN
ABNO-1 (A5) (A14)
ABOI (1A1)
CCRT-1 (A3)(A6)
SPRE (A6)
EDMR
ERAS (A5)
AKOE (A11)
AKTE (A11)
SDAK (A9) (A10) (A11)
CARP-2 (A5)
RRPN (A5)
SSTO
ABON (A5)
SRTP (A10)
MDRE (A6)
ZERB (A18)
TIFR (A11)
TM5895-438-35-4

Figure 1-6. 1A2A4, Receive End of Message PL-1142/G, schematic diagram.

NOTES

1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS. CAPACITANCES ARE IN UF
2. IDENTIFICATION NUMBERS SHOWN WITHIN LOGIC SYMBOLS ALSO ESTABLISH PHYSICAL LOCATION ON EACH PRINTED WIRING BOARD ASSEMBLY. ALL PRINTED WIRING BOARD ASSEMBLIES LOCATE NUMBER 1 IN UPPER LEFT (CONTACT FINGER END) WITH NUMBER 25 IN LOWER RIGHT OF THE ITEM
3. LOGIC ELEMENT TERMINALS ARE NUMBERED COUNTERCLOCKWISE FROM 1 THROUGH 10 WHEN VIEWED FROM THE TOP. TERMINAL 10 COINCIDES WITH THE KEY
4. TERMINAL 1 IS GROUND AND TERMINAL 6 IS +5VOLTS ON ALL LOGIC ELEMENTS
5. LOGIC CAN POSITIONS 3, 8, 21, 24 ARE NOT USED
6. RECEPTACLE VIEWED FROM PIN SIDE


P1
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
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31
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7. SPRAGUE ELECTRIC, TYPE NUMBER TN-56

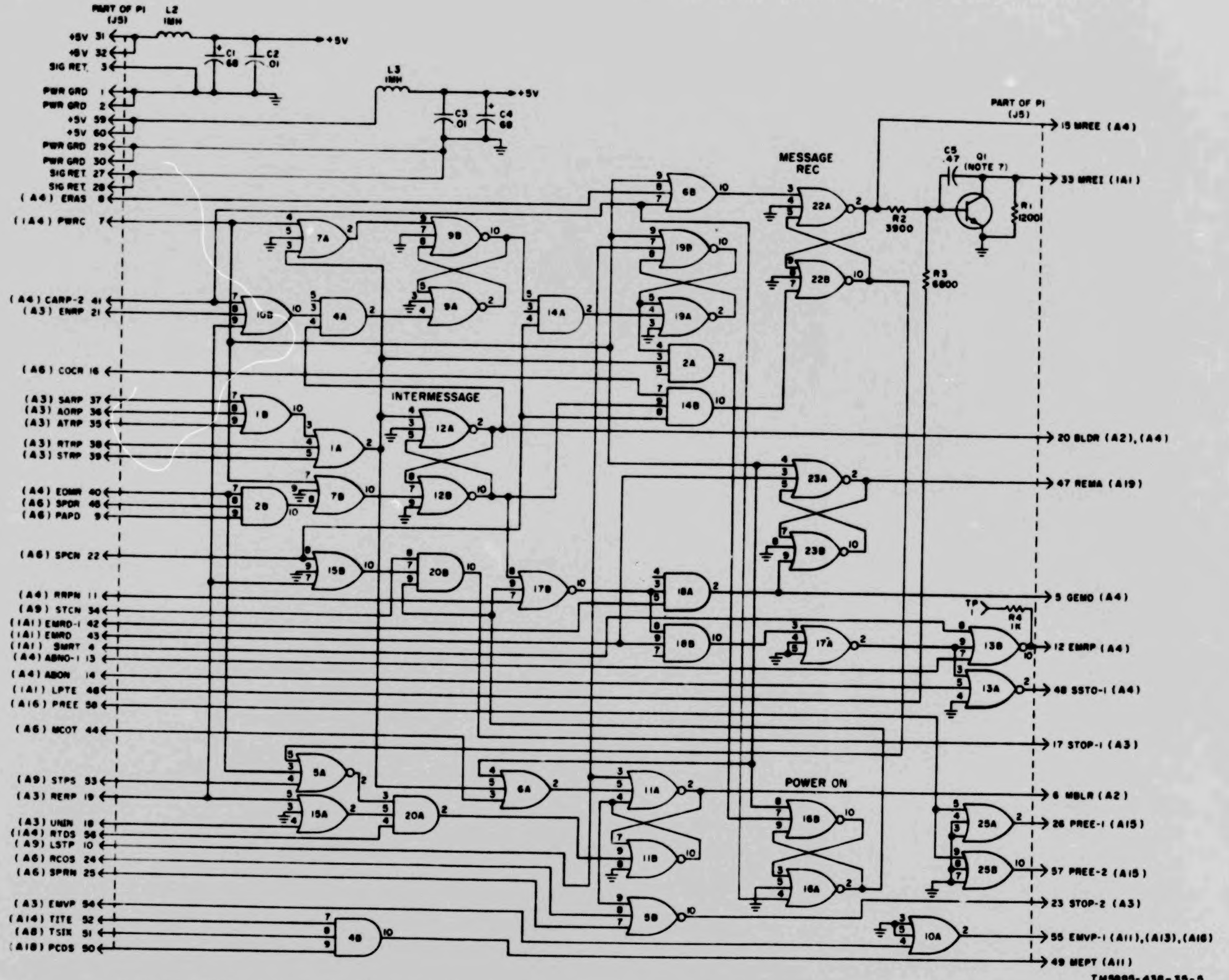
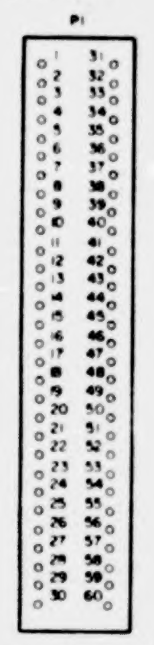

PART OF P1 (J5)
L2 1MH
L3 1MH
C1 68
C2 .01
C3 .01
C4 68
+5V
+5V 31
+5V 32
SIG RET 3
PWR GRD 1
PWR GRD 2
+5V 59
+5V 60
PWR GRD 29
PWR GRD 30
SIG RET 27
SIG RET 28
(A4) ERAS 8
(1A4) PWRC 7
(A4) CARP-2 41
(A3) ENRP 21
(A6) COCR 16
(A3) SARP 37
(A3) AORP 36
(A3) ATRP 35
(A3) RTRP 38
(A3) STRP 39
(A4) EOMR 40
(A6) SPOR 46
(A6) PAPD 9
(A6) SPCN 22
(A4) RRPN 11
(A9) STCN 34
(1A1) EMRO-1 42
(1A1) EMRO 43
(1A1) SMRT 4
(A4) ABNO-1 13
(A4) ABON 14
(1A1) LPTE 45
(A16) PREE 58
(A6) MCOT 44
(A9) STPS 53
(A3) RERP 19
(A3) UNIN 18
(1A4) RTDS 56
(A9) LSTP 10
(A6) RCOS 24
(A6) SPRN 25
(A3) EMVP 54
(A14) TITE 52
(A8) TSIX 51
(A18) PCDS 50
INTERMESSAGE
MESSAGE REC
POWER ON
7A
9B
9A
10B
4A
14A
1B
1A
12A
12B
2B
7B
15B
20B
17B
5A
15A
20A
6A
4B
6B
19B
19A
2A
14B
22A
22B
23A
23B
18A
18B
17A
13B
13A
11A
11B
16B
16A
5B
25A
25B
10A
C5 .47
Q1 (NOTE 7)
R1 1200
R2 3900
R3 6800
R4 1K
TP
15 MREE (A4)
33 MREI (1A1)
20 BLDR (A2),(A4)
47 REMA (A19)
5 GEMO (A4)
12 EMRP (A4)
48 SSTO-1 (A4)
17 STOP-1 (A3)
6 MBLR (A2)
26 PREE-1 (A15)
57 PREE-2 (A15)
23 STOP-2 (A3)
55 EMVP-1 (A11),(A13),(A16)
49 MEPT (A11)
TM5895-438-35-5

Figure 1-7. 1A2A5, Output Device Control PL-1157/G, schematic diagram.

NOTES

1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UF
2. IDENTIFICATION NUMBERS SHOWN WITHIN LOGIC SYMBOLS ALSO ESTABLISH PHYSICAL LOCATION ON EACH PRINTED WIRING BOARD ASSEMBLY. ALL PRINTED WIRING BOARD ASSEMBLIES LOCATE NUMBER 1 IN UPPER LEFT (CONTACT FINGER END) WITH NUMBER 25 IN LOWER RIGHT OF THE ITEM
3. LOGIC ELEMENT TERMINALS ARE NUMBERED COUNTERCLOCKWISE FROM 1 THROUGH 10 WHEN VIEWED FROM THE TOP. TERMINAL 10 COINCIDES WITH THE KEY
4. TERMINAL 1 IS GROUND AND TERMINAL 6 IS +5VOLTS ON ALL LOGIC ELEMENTS
5. LOGIC CAN POSITION 15B IS NOT USED
6. RECEPTACLE VIEWED FROM PIN SIDE


P1
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19
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7. GUARD CONDUCTOR NOT CONNECTED TO ANY CIRCUIT ELEMENTS

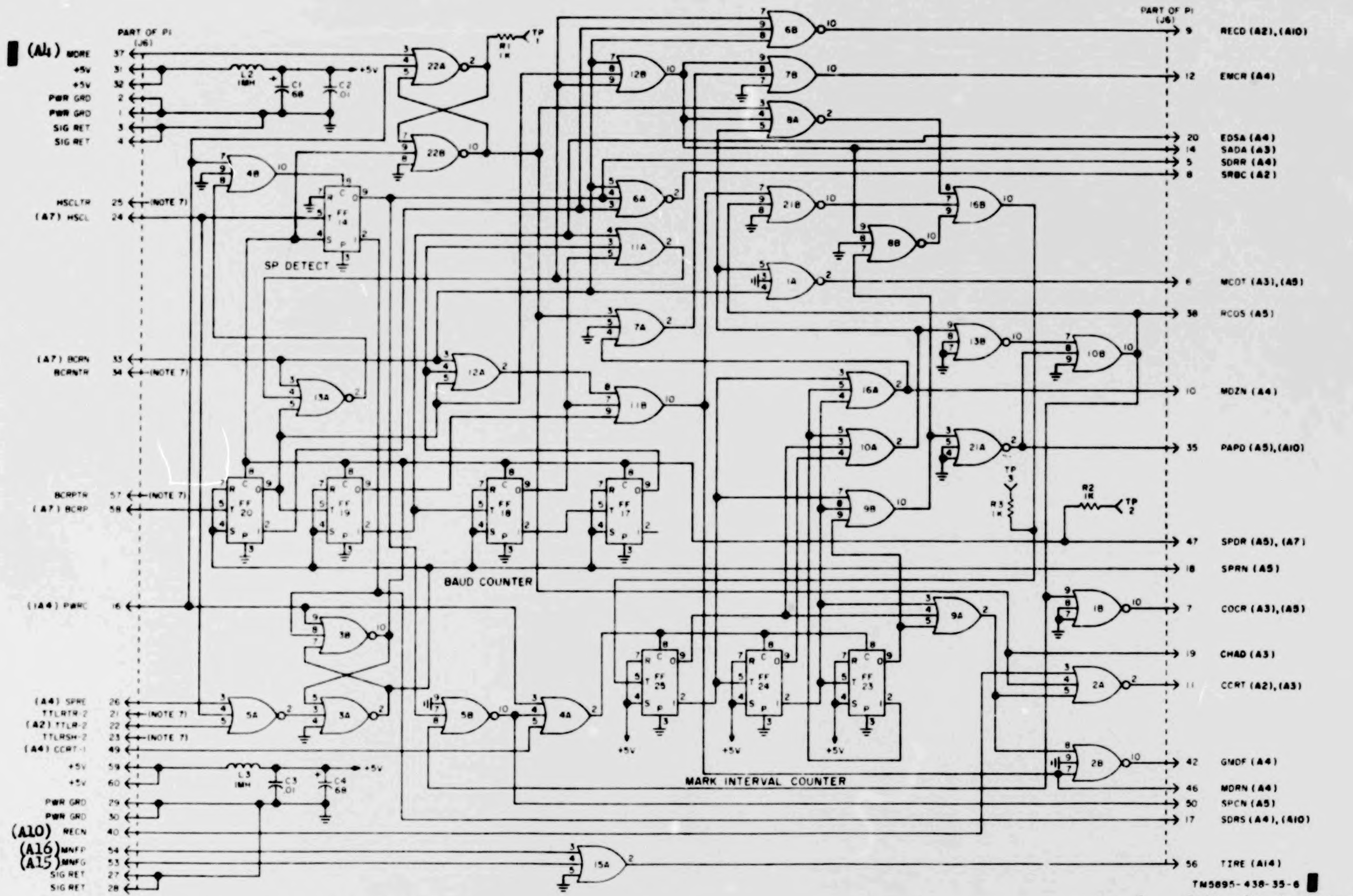
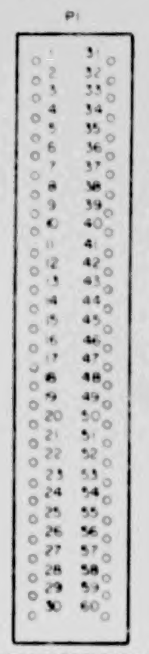

PART OF P1 (J6)
(A4) MDRE 37
+5V 31
+5V 32
PWR GRD 2
PWR GRD 1
SIG RET 3
SIG RET 4
HSCLTR 25 (NOTE 7)
(A7) HSCL 24
(A7) BCRN 33
BCRNTR 34 (NOTE 7)
BCRPTR 57 (NOTE 7)
(A7) BCRP 58
(1A4) PWRC 16
(A4) SPRE 26
TTLRTR-2 21 (NOTE 7)
(A2) TTLR-2 22
TTLRSH-2 23 (NOTE 7)
(A4) CCRT-1 49
+5V 59
+5V 60
PWR GRD 29
PWR GRD 30
(A10) RECN 40
(A16) MNFP 54
(A15) MNFG 53
SIG RET 27
SIG RET 28
L2 1MH
C1 68
C2 .01
L3 1MH
C3 .01
C4 68
+5V
R1 1K
TP 1
R2 1K
TP 2
R3 1K
TP 3
22A
22B
4B
FF 14
SP DETECT
13A
12A
FF 20
FF 19
FF 18
FF 17
BAUD COUNTER
3B
5A
3A
5B
4A
FF 25
FF 24
FF 23
MARK INTERVAL COUNTER
15A
6B
7B
8A
12B
6A
11A
7A
11B
21B
1A
8B
15B
13B
10B
16A
10A
9B
21A
9A
1B
2A
2B
PART OF P1 (J6)
9 RECD (A2),(A10)
12 EMCR (A4)
20 EDSA (A4)
14 SADA (A3)
5 SDRR (A4)
8 SRBC (A2)
6 MCOT (A3),(A5)
38 RCOS (A5)
10 MDZN (A4)
35 PAPD (A5),(A10)
47 SPDR (A5), (A7)
18 SPRN (A5)
7 COCR (A3),(A5)
19 CHAD (A3)
11 CCRT (A2),(A3)
42 GMDF (A4)
46 MDRN (A4)
50 SPCN (A5)
17 SDRS (A4),(A10)
56 TIRE (A14)
TM5895-438-35-6

Figure 1-8. 1A2A6, Receive Baud Counter PL-1140/G, schematic diagram.

NOTES

1. UNLESS OTHERWISE INDICATED RESISTANCES ARE IN OHMS CAPACITANCES ARE IN UF
2. IDENTIFICATION NUMBERS SHOWN WITHIN LOGIC SYMBOLS ALSO ESTABLISH PHYSICAL LOCATION ON EACH PRINTED WIRING BOARD ASSEMBLY ALL PRINTED WIRING BOARD ASSEMBLIES LOCATE NUMBER 1 IN UPPER LEFT (CONTACT FINGER END) WITH NUMBER 25 IN LOWER RIGHT OF THE ITEM
3. LOGIC ELEMENT TERMINALS ARE NUMBERED COUNTERCLOCKWISE FROM 1 THROUGH 10 WHEN VIEWED FROM THE TOP TERMINAL 10 COINCIDES WITH THE KEY
4. TERMINAL 1 IS GROUND AND TERMINAL 6 IS +5VOLTS ON ALL LOGIC ELEMENTS
5. LOGIC CAN POSITIONS 1 THRU 6 AND 8 THRU 25 ARE NOT USED
6. RECEPTACLE VIEWED FROM PIN SIDE


P1
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19
20
21
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44
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52
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54
55
56
57
58
59
60

7. GUARD CONNECTOR NOT CONNECTED TO ANY CIRCUIT ELEMENTS
8. THESE COMPONENTS ARE FOR EXPANSION FOR OTHER THAN PRESENT SYSTEM BAUD RATES, AND ARE NOT SUPPLIED.

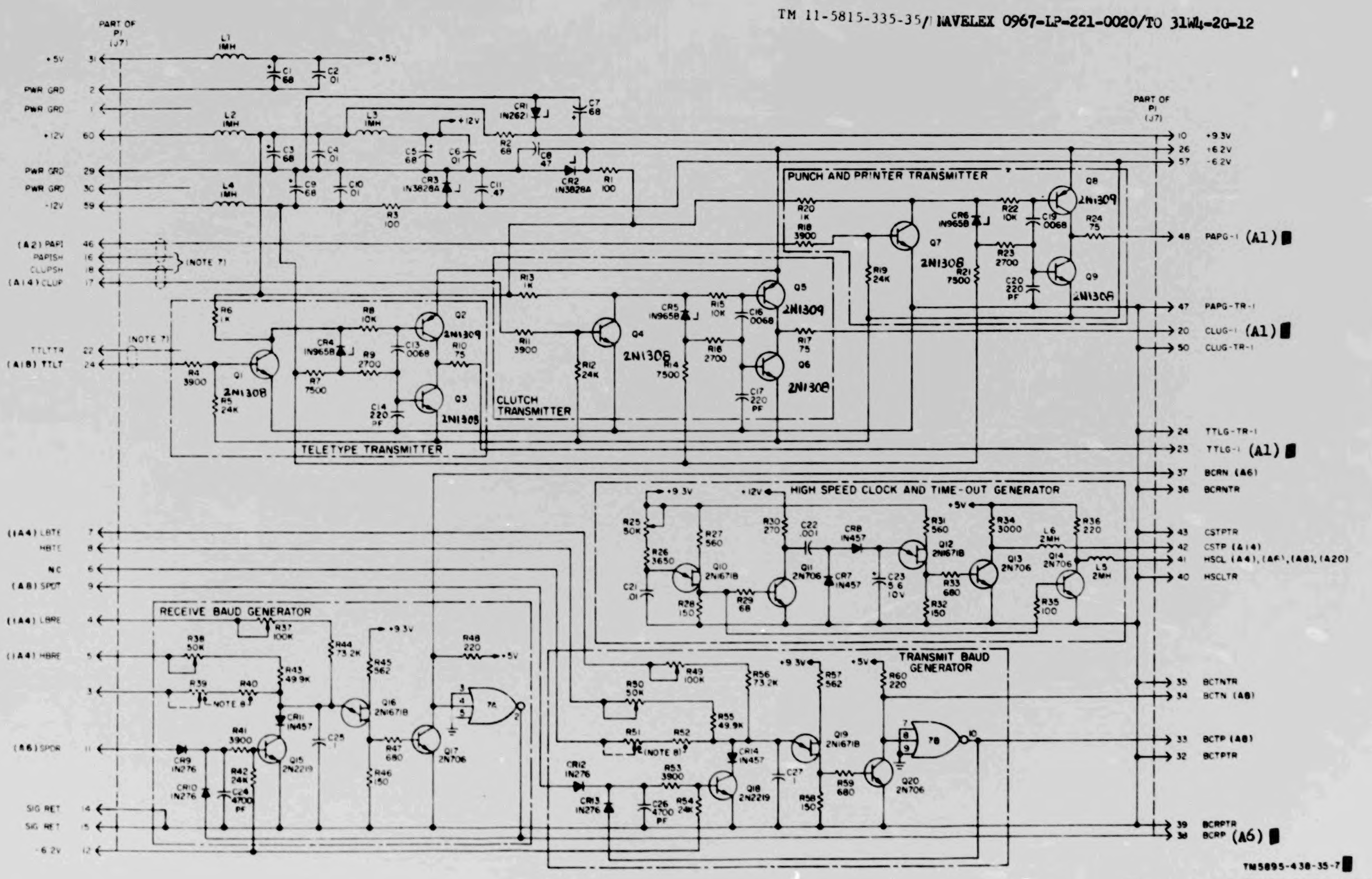
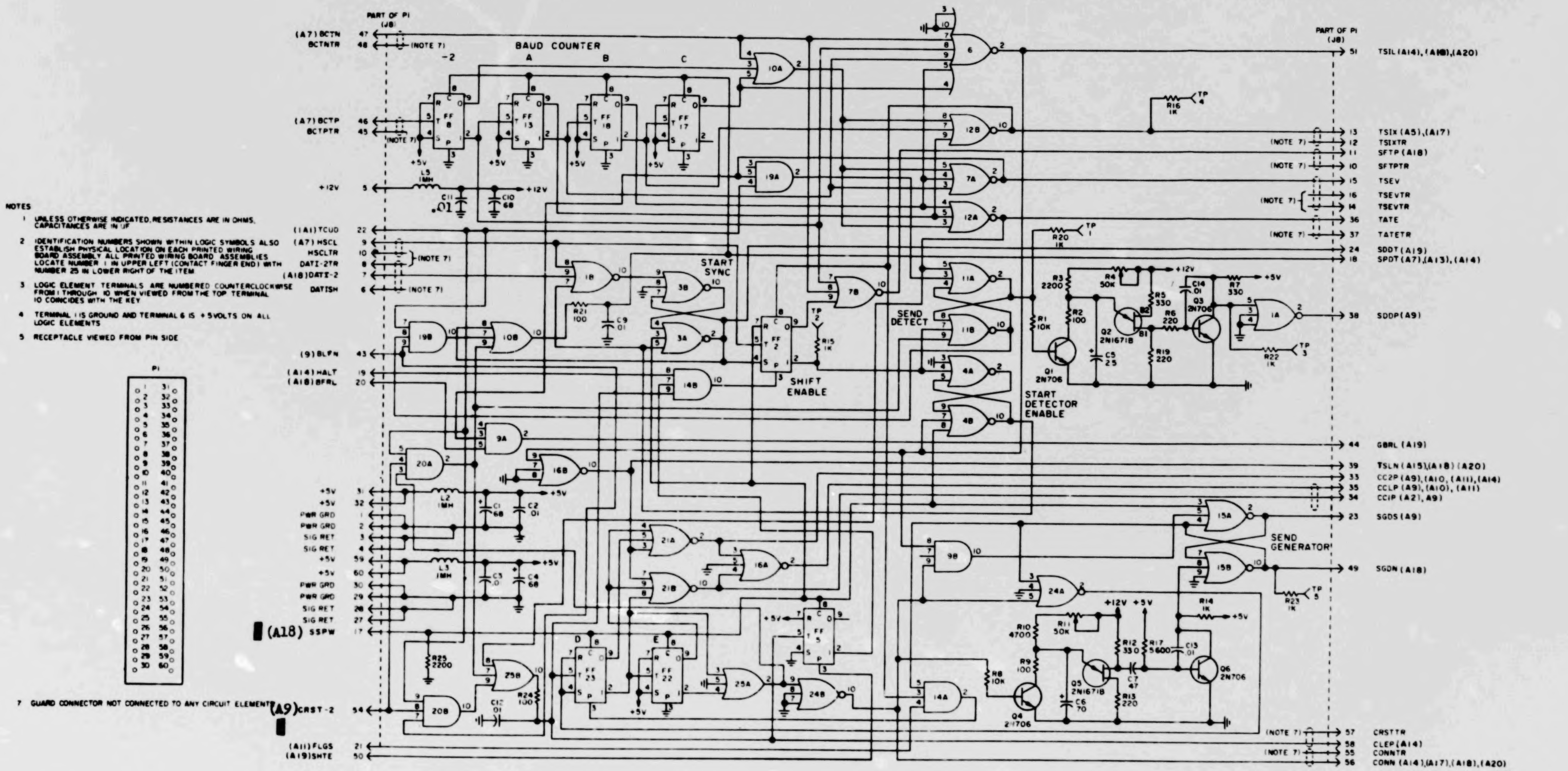

PART OF P1 (J7)
+5V 31
PWR GRD 2
PWR GRD 1
+12V 60
PWR GRD 29
PWR GRD 30
-12V 59
(A2) PAPI 46
PAPISH 16
CLUPSH 18
(A14) CLUP 17
(NOTE 7)
TTLTTR 22
(A18) TTLT 24
(1A4) LBTE 7
HBTE 8
NC 6
(A8) SPDT 9
(1A4) LBRE 4
(1A4) HBRE 5
3
(A6) SPDR 11
SIG RET 14
SIG RET 15
-6.2V 12
TELETYPE TRANSMITTER
CLUTCH TRANSMITTER
PUNCH AND PRINTER TRANSMITTER
HIGH SPEED CLOCK AND TIME-OUT GENERATOR
RECEIVE BAUD GENERATOR
TRANSMIT BAUD GENERATOR
PART OF P1 (J7)
10 +9.3V
26 +6.2V
57 -6.2V
48 PAPG-1 (A1)
47 PAPG-TR-1
20 CLUG-1 (A1)
50 CLUG-TR-1
24 TTLG-TR-1
23 TTLG-1 (A1)
37 BCRN (A6)
36 BCRNTR
43 CSTPTR
42 CSTP (A14)
41 HSCL (A4),(A6),(A8),(A20)
40 HSCLTR
35 BCTNTR
34 BCTN (A8)
33 BCTP (A8)
32 BCTPTR
39 BCRPTR
38 BCRP (A6)
TM5895-438-35-7

Figure 1-9. 1A2A7, Timing Generator PL-1143/G, schematic diagram.


PART OF P1 (J8)
BAUD COUNTER
-2
A
B
C
START SYNC
SEND DETECT
SHIFT ENABLE
START DETECTOR ENABLE
SEND GENERATOR
(A7) BCTN
BCTNTR
(A7) BCTP
BCTPTR
+12V
(1A1) TCUD
(A7) HSCL
HSCLTR
DATI-2TR
(A18) DATI-2
DATISH
(9) BLFN
(A14) HALT
(A18) BFRL
+5V
PWR GRD
SIG RET
(A18) SSPW
(A9) CRST-2
(A11) FLGS
(A9) SHTE
TSIL (A14), (A18), (A20)
TSIX (A5), (A17)
TSIXTR
SFTP (A18)
SFTPTR
TSEV
TSEVTR
TATE
TATETR
SDDT (A19)
SPDT (A7), (A15), (A14)
SDDP (A9)
GBRL (A19)
TSLN (A15), (A18), (A20)
CCLP (A9), (A10), (A11)
SGDS (A9)
SGDN (A18)
CRSTTR
CLEP (A14)
CONNTR
CONN (A14), (A17), (A18), (A20)
(NOTE 7)
P1
TM5895-438-35-8

NOTES

1 UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UF

2 IDENTIFICATION NUMBERS SHOWN WITHIN LOGIC SYMBOLS ALSO ESTABLISH PHYSICAL LOCATION ON EACH PRINTED WIRING BOARD ASSEMBLY. ALL PRINTED WIRING BOARD ASSEMBLIES LOCATE NUMBER 1 IN UPPER LEFT (CONTACT FINGER END) WITH NUMBER 25 IN LOWER RIGHT OF THE ITEM

3 LOGIC ELEMENT TERMINALS ARE NUMBERED COUNTERCLOCKWISE FROM 1 THROUGH 10 WHEN VIEWED FROM THE TOP. TERMINAL 10 COINCIDES WITH THE KEY

4 TERMINAL 1 IS GROUND AND TERMINAL 6 IS +5 VOLTS ON ALL LOGIC ELEMENTS

5 RECEPTACLE VIEWED FROM PIN SIDE

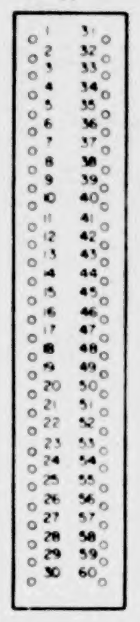
7 GUARD CONNECTOR NOT CONNECTED TO ANY CIRCUIT ELEMENT

Figure 1-10. 1A2A8, Transmit Baud Counter PL-1144/G, schematic diagram.

NOTES

1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UF
2. IDENTIFICATION NUMBERS SHOWN WITHIN LOGIC SYMBOLS ALSO ESTABLISH PHYSICAL LOCATION ON EACH PRINTED WIRING BOARD ASSEMBLY. ALL PRINTED WIRING BOARD ASSEMBLIES LOCATE NUMBER 1 IN UPPER LEFT (CONTACT FINGER END) WITH NUMBER 25 IN LOWER RIGHT OF THE ITEM
3. LOGIC ELEMENT TERMINALS ARE NUMBERED COUNTERCLOCKWISE FROM 1 THROUGH 10 WHEN VIEWED FROM THE TOP. TERMINAL 10 COINCIDES WITH THE KEY
4. TERMINAL 1 IS GROUND AND TERMINAL 6 IS +5 VOLTS ON ALL LOGIC ELEMENTS
5. LOGIC CAN POSITIONS 1, 2, 5, 16, 19, 20, 21, 22, 23, 24, 25 ARE NOT USED
6. RECEPTACLE VIEWED FROM PIN SIDE

P1


1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30
31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60

7. SPRAGUE ELECTRIC TYPE NO TN-56
8. GUARD CONNECTOR NOT CONNECTED TO ANY CIRCUIT ELEMENTS

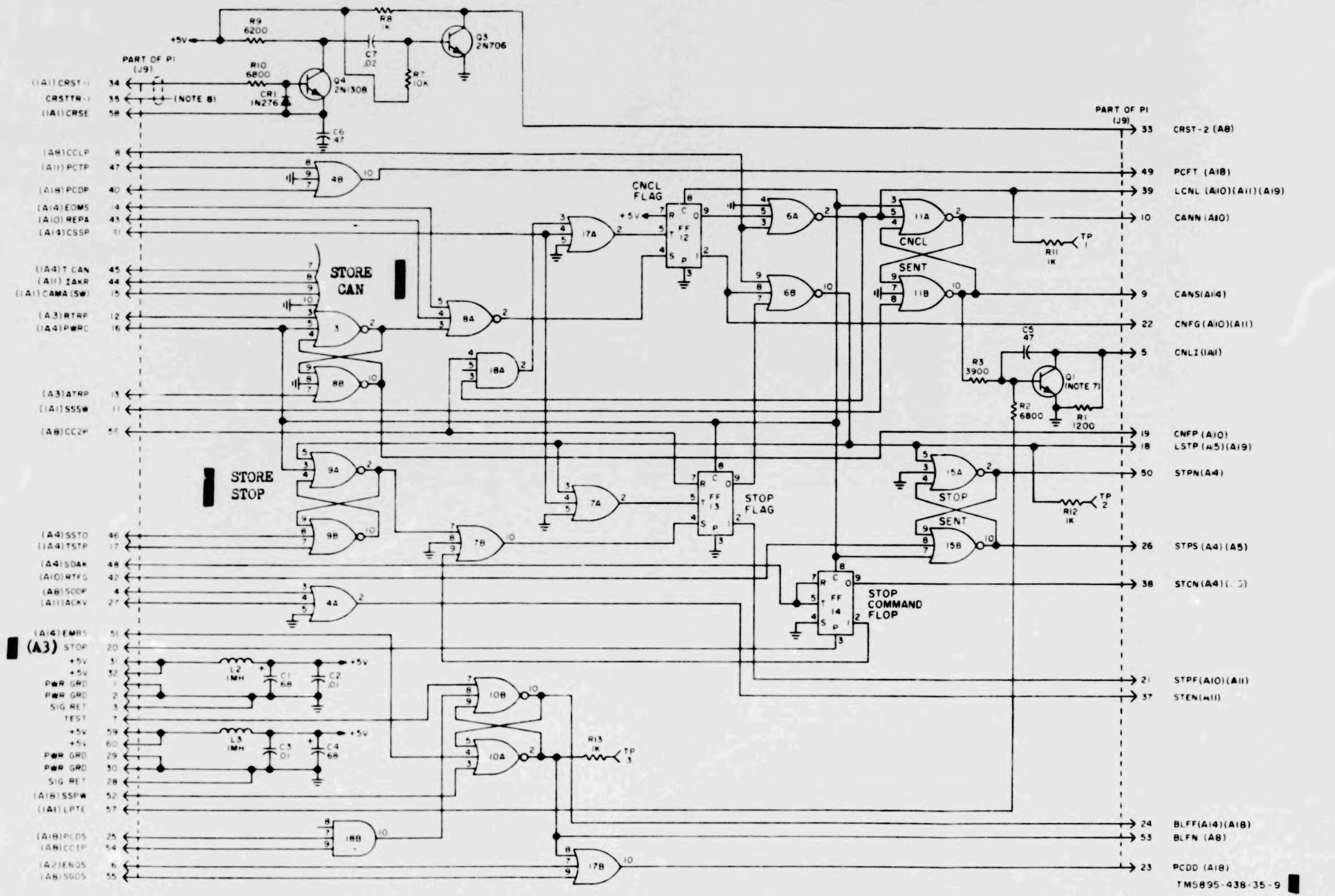

+5V
R9 6200
R8 1K
C7 .02
R7 10K
Q3 2N706
PART OF P1 (J9)
R10 6800
CR1 1N276
Q4 2N1308
C6 47
(1A1) CRST-1 34
CRSTTR-1 35
(NOTE 8)
(1A1) CRSE 58
(A8) CCLP 8
(A11) PCTP 47
(A18) PCDP 40
(A14) EOMS 14
(A10) REPA 43
(A14) CSSP 31
(1A4) T CAN 45
(A11) IAKR 44
(1A1) CAMA (SW) 15
(A3) RTRP 12
(1A4) PWRC 16
(A3) ATRP 13
(1A1) SSSW 11
(A8) CC2P 56
(A4) SSTO 46
(1A4) TSTP 17
(A4) SDAK 48
(A10) RTFG 42
(A8) SDDP 4
(A11) ACKV 27
(A14) EMBS 51
(A3) STOP 20
+5V 31
+5V 32
PWR GRD 1
PWR GRD 2
SIG RET 3
TEST 7
+5V 59
+5V 60
PWR GRD 29
PWR GRD 30
SIG RET 28
(A18) SSPW 52
(1A1) LPTE 57
(A18) PCDS 25
(A8) CC1P 54
(A2) ENDS 6
(A8) SGDS 55
L2 1MH
C1 68
C2 .01
L3 1MH
C3 .01
C4 68
STORE CAN
STORE STOP
4B
3
8A
8B
18A
9A
9B
7B
4A
10B
10A
18B
17B
7A
CNCL FLAG
FF 12
6A
6B
11A
CNCL SENT
11B
FF 13
STOP FLAG
15A
STOP SENT
15B
FF 14
STOP COMMAND FLOP
R13 1K
TP 3
R11 1K
TP 1
R12 1K
TP 2
C5 47
R3 3900
Q1 (NOTE 7)
R2 6800
R1 1200
PART OF P1 (J9)
33 CRST-2 (A8)
49 PCFT (A18)
39 LCNL (A10)(A11)(A19)
10 CANN (A10)
9 CANS (A14)
22 CNFG (A10)(A11)
5 CNLI (1A11)
19 CNFP (A10)
18 LSTP (A5)(A19)
50 STPN (A4)
26 STPS (A4)(A5)
38 STCN (A4)
21 STPF (A10)(A11)
37 STEN (A11)
24 BLFF (A14)(A18)
53 BLFN (A8)
23 PCDD (A18)

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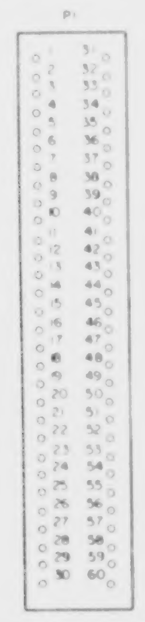
Figure 1-11. 1A2A9, Transmit Cancel-Stop Sequence PL-1145/G, schematic diagram.

NOTES

1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UF.
2. IDENTIFICATION NUMBERS SHOWN WITHIN LOGIC SYMBOLS ALSO ESTABLISH PHYSICAL LOCATION ON EACH PRINTED WIRING BOARD ASSEMBLY. ALL PRINTED WIRING BOARD ASSEMBLIES LOCATE NUMBER 1 IN UPPER LEFT (CONTACT FINGER END) WITH NUMBER 25 IN LOWER RIGHT OF THE ITEM.
3. LOGIC ELEMENT TERMINALS ARE NUMBERED COUNTERCLOCKWISE FROM 1 THROUGH 10 WHEN VIEWED FROM THE TOP. TERMINAL 10 COINCIDES WITH THE KEY.
4. TERMINAL 1 IS GROUND AND TERMINAL 6 IS +5 VOLTS ON ALL LOGIC ELEMENTS.
5. LOGIC CAN POSITIONS 4A, 5, 12, 17 ARE NOT USED.
6. RECEPTACLE VIEWED FROM PIN SIDE.


P1
1 31
2 32
3 33
4 34
5 35
6 36
7 37
8 38
9 39
10 40
11 41
12 42
13 43
14 44
15 45
16 46
17 47
18 48
19 49
20 50
21 51
22 52
23 53
24 54
25 55
26 56
27 57
28 58
29 59
30 60

7. GUARD CONNECTOR NOT CONNECTED TO ANY CIRCUIT ELEMENTS.
8. SPRAGUE ELECTRIC, TYPE NUMBER TN 56.

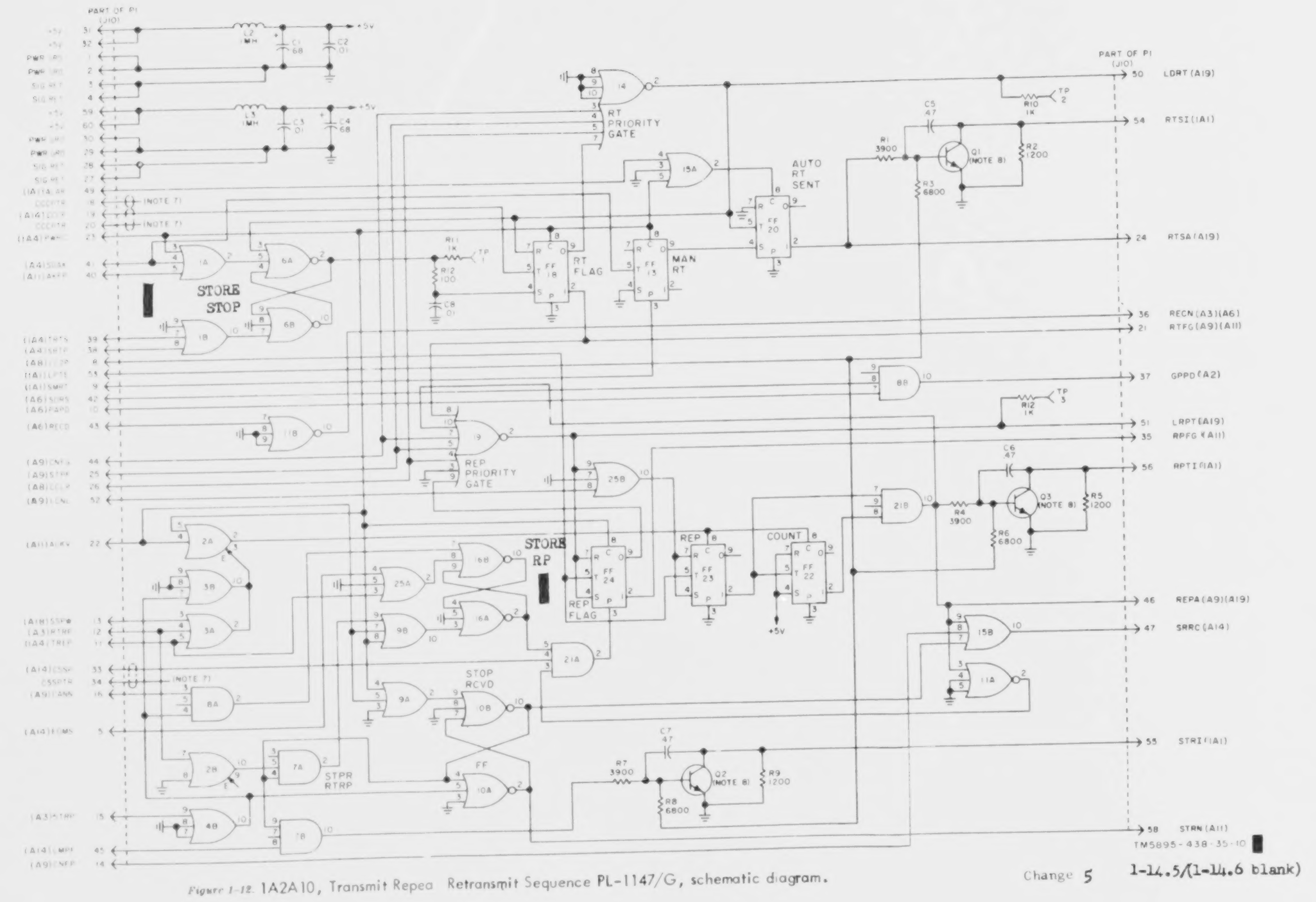
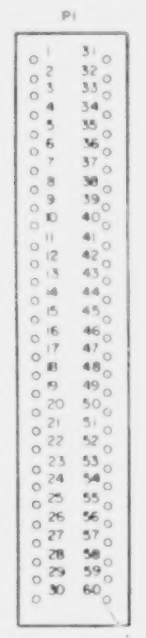

PART OF P1 (J10)
STORE STOP
STORE RP
RT PRIORITY GATE
AUTO RT SENT
RT FLAG
MAN RT
REP PRIORITY GATE
REP FLAG
REP
COUNT
STOP RCVD
FF
STPR RTRP
+5V
50 LDRT (A19)
54 RTSI (1A1)
24 RTSA (A19)
36 RECN (A3)(A6)
21 RTFG (A9)(A11)
37 GPPD (A2)
51 LRPT (A19)
35 RPFG (A11)
56 RPTI (1A1)
46 REPA (A9)(A19)
47 SRRC (A14)
55 STRI (1A1)
58 STRN (A11)
TP 2
TP 3
R10 1K
R7 3900
R8 6800
R9 1200
C7 47
Q2 (NOTE 8)
Q3 (NOTE 8)
R5 1200
TM5895-438-35-10

Figure 1-12. 1A2A10, Transmit Repea Retransmit Sequence PL-1147/G, schematic diagram.

NOTES

1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UF
2. IDENTIFICATION NUMBERS SHOWN WITHIN LOGIC SYMBOLS ALSO ESTABLISH PHYSICAL LOCATION ON EACH PRINTED WIRING BOARD ASSEMBLY. ALL PRINTED WIRING BOARD ASSEMBLIES LOCATE NUMBER 1 IN UPPER LEFT (CONTACT FINGER END) WITH NUMBER 25 IN LOWER RIGHT OF THE ITEM
3. LOGIC ELEMENT TERMINALS ARE NUMBERED COUNTERCLOCKWISE FROM 1 THROUGH 10 WHEN VIEWED FROM THE TOP. TERMINAL 10 COINCIDES WITH THE KEY
4. TERMINAL 1 IS GROUND AND TERMINAL 6 IS +5 VOLTS ON ALL LOGIC ELEMENTS
5. LOGIC CAN POSITIONS 1, 3, 5, 14, 16B ARE NOT USED
6. RECEPTACLE VIEWED FROM PIN SIDE


P1
1 31
2 32
3 33
4 34
5 35
6 36
7 37
8 38
9 39
10 40
11 41
12 42
13 43
14 44
15 45
16 46
17 47
18 48
19 49
20 50
21 51
22 52
23 53
24 54
25 55
26 56
27 57
28 58
29 59
30 60

7. SPRAGUE ELECTRIC, TYPE NUMBER TN-56

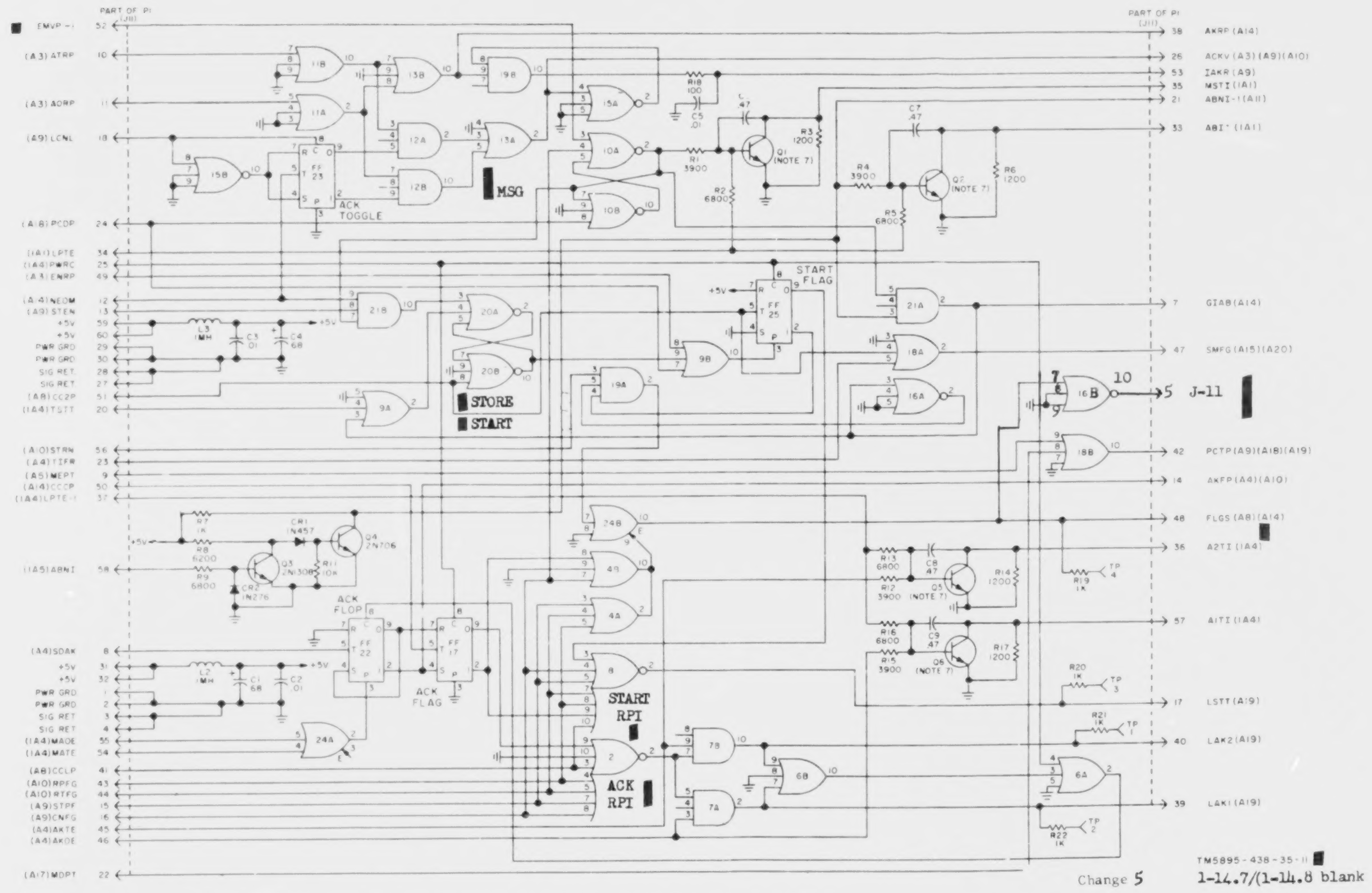
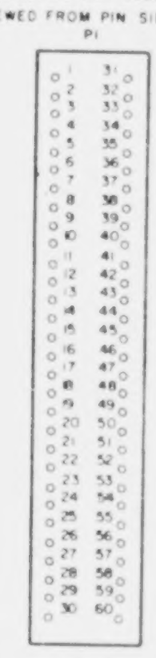

PART OF P1 (J11)
MSG
ACK TOGGLE
START FLAG
STORE
START
ACK FLOP
ACK FLAG
START RPT
ACK RPT
J-11
10
5
AKRP (A14)
ACKV (A3)(A9)(A10)
IAKR (A9)
MSTI (A1)
ABNI-1 (A11)
ABI' (A1)
LSTT (A19)
LAK2 (A19)
LAK1 (A19)

Figure 1-13. 1A2A11, Transmit Start-Acknowledge Sequence, PL-1146/G, schematic diagram.

NOTES

1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UF.
2. IDENTIFICATION NUMBERS SHOWN WITHIN LOGIC SYMBOLS ALSO ESTABLISH PHYSICAL LOCATION ON EACH PRINTED WIRING BOARD ASSEMBLY. ALL PRINTED WIRING BOARD ASSEMBLIES LOCATE NUMBER 1 IN UPPER LEFT (CONTACT FINGER END) WITH NUMBER 25 IN LOWER RIGHT OF THE ITEM.
3. LOGIC ELEMENT TERMINALS ARE NUMBERED COUNTERCLOCKWISE FROM 1 THROUGH 10 WHEN VIEWED FROM THE TOP. TERMINAL 10 COINCIDES WITH THE KEY.
4. TERMINAL 1 IS GROUND AND TERMINAL 6 IS +5VOLTS ON ALL LOGIC ELEMENTS.
5. LOGIC CAN POSITIONS 1,2,3,4,5,6,7,8,9,10,11A,12,13,14,15,17,18, 19,20,22,23,24,25, ARE NOT USED.
6. RECEPTACLE VIEWED FROM PIN SIDE.


P1
1 31
2 32
3 33
4 34
5 35
6 36
7 37
8 38
9 39
10 40
11 41
12 42
13 43
14 44
15 45
16 46
17 47
18 48
19 49
20 50
21 51
22 52
23 53
24 54
25 55
26 56
27 57
28 58
29 59
30 60

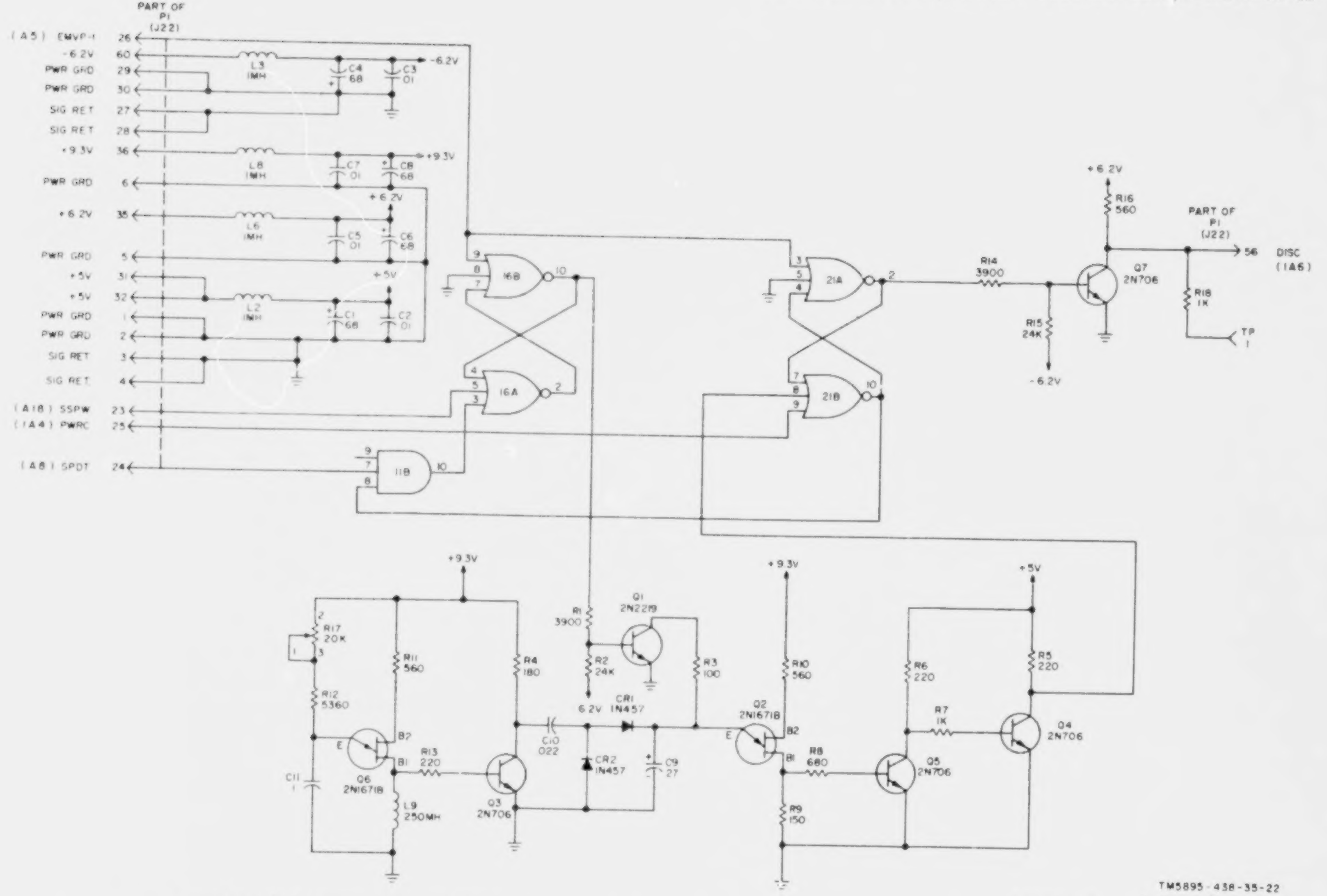

PART OF P1 (J22)
(A5) EMVP-1 26
-6.2V 60
PWR GRD 29
PWR GRD 30
SIG RET 27
SIG RET 28
+9.3V 36
PWR GRD 6
+6.2V 35
PWR GRD 5
+5V 31
+5V 32
PWR GRD 1
PWR GRD 2
SIG RET 3
SIG RET 4
(A18) SSPW 23
(1A4) PWRC 25
(A8) SPDT 24
L3 1MH
C4 68
C3 .01
-6.2V
L8 1MH
C7 .01
C8 68
+9.3V
+6.2V
L6 1MH
C5 .01
C6 68
+5V
L2 1MH
C1 68
C2 .01
16B
16A
11B
21A
21B
R14 3900
R15 24K
-6.2V
+6.2V
R16 560
Q7 2N706
PART OF P1 (J22)
56
DISC (1A6)
R18 1K
TP 1
+9.3V
R17 20K
R12 5360
R11 560
R4 180
Q6 2N1671B
C11 1
L9 250MH
R13 220
Q3 2N706
C10 .022
R1 3900
R2 24K
6.2V
Q1 2N2219
R3 100
CR1 1N457
CR2 1N457
C9 27
+9.3V
R10 560
Q2 2N1671B
R8 680
R9 150
R6 220
R7 1K
Q5 2N706
+5V
R5 220
Q4 2N706

Figure 1-14. 2A3, Disconnect Line PL-1154/G, schematic diagram.

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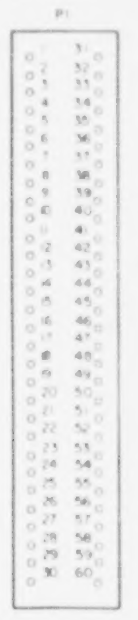
NOTES:

1. UNLESS OTHERWISE INDICATED RESISTANCES ARE IN OHMS. CAPACITANCES ARE IN UF.
2. IDENTIFICATION NUMBERS SHOWN WITHIN LOGIC SYMBOLS ALSO ESTABLISH PHYSICAL LOCATION ON EACH PRINTED WIRING BOARD ASSEMBLY. ALL PRINTED WIRING BOARD ASSEMBLIES LOCATE NUMBER 1 IN UPPER LEFT (CONTACT FINGER END) WITH NUMBER 25 IN LOWER RIGHT OF THE ITEM.
3. LOGIC ELEMENT TERMINALS ARE NUMBERED COUNTERCLOCKWISE FROM 1 THROUGH 10 WHEN VIEWED FROM THE TOP. TERMINAL 10 COINCIDES WITH THE KEY.
4. TERMINAL 1 IS GROUND AND TERMINAL 6 IS +5VOLTS ON ALL LOGIC ELEMENTS.
5. LOGIC CAN POSITIONS 1,5,19B,25 ARE NOT USED.
6. RECEPTACLE VIEWED FROM PIN SIDE.


P1
1
2
3
4
5
6
7
8
9
10
11
12
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14
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16
17
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19
20
21
22
23
24
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32
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7. GUARD CONNECTOR NOT CONNECTED TO ANY CIRCUIT ELEMENTS.
8. SPRAGUE ELECTRIC, TYPE NUMBER TN-56

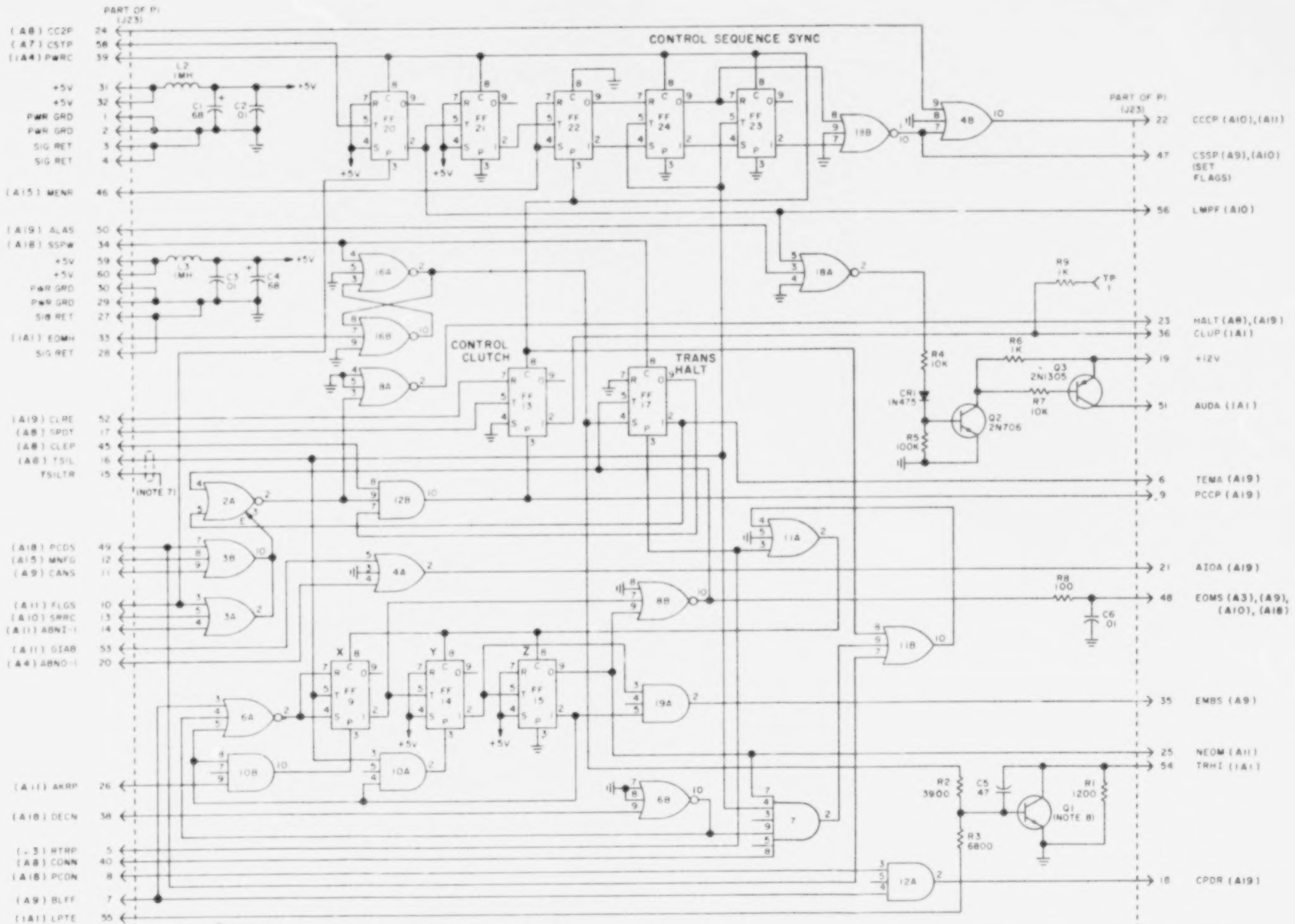

PART OF P1 (J23)
(A8) CC2P 24
(A7) CSYP 58
(1A4) PWRC 39
+5V 31
+5V 32
PWR GRD 1
PWR GRD 2
SIG RET 3
SIG RET 4
(A15) MENR 46
(A19) ALAS 50
(A18) SSPW 34
+5V 59
+5V 60
PWR GRD 30
PWR GRD 29
SIG RET 27
(1A1) EOMH 33
SIG RET 28
(A19) CLRE 52
(A8) SPDT 17
(A8) CLEP 45
(A8) TSIL 16
TSILTR 15
(NOTE 7)
(A18) PCDS 49
(A15) MNFG 12
(A9) CANS 11
(A11) FLGS 10
(A10) SRRC 13
(A11) ABNI-1 14
(A11) GIAB 53
(A4) ABNO-1 20
(A11) AKRP 26
(A18) DECN 38
(.3) RTRP 5
(A8) CONN 40
(A18) PCON 8
(A9) BLFF 7
(1A1) LPTE 55
(A6) TIRE 42
(1A4) MEND 43
L2 1MH
C1 68
C2 .01
L3 1MH
C3 .01
C4 68
+5V
CONTROL SEQUENCE SYNC
FF 20
FF 21
FF 22
FF 24
FF 23
19B
4B
16A
16B
8A
18A
CONTROL CLUTCH
FF 13
TRANS HALT
FF 17
2A
3B
3A
12B
4A
8B
11A
11B
X
Y
Z
FF 9
FF 14
FF 15
6A
10B
10A
19A
6B
7
12A
2B
R9 1K
TP 1
R4 10K
CR1 1N475
R5 100K
Q2 2N706
R6 1K
R7 10K
Q3 2N1305
R8 100
C6 .01
R2 3900
R3 6800
C5 47
R1 1200
Q1 (NOTE 8)
PART OF P1 (J23)
22 CCCP (A10),(A11)
47 CSSP (A9),(A10) (SET FLAGS)
56 LWPF (A10)
23 HALT (A8),(A19)
36 CLUP (1A1)
19 +12V
51 AUDA (1A1)
6 TEMA (A19)
9 PCCP (A19)
21 AIOA (A19)
48 EOMS (A3),(A9), (A10),(A18)
35 EMBS (A9)
25 NEOM (A11)
54 TRHI (1A1)
18 CPDR (A19)
41 TITE (A5)
TM5895-438-35-23

Figure 1-15. 1A2A14, Input Device Control PL-1152/G schematic diagram.

NOTES

1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UF.
2. IDENTIFICATION NUMBERS SHOWN WITHIN LOGIC SYMBOLS ALSO ESTABLISH PHYSICAL LOCATION ON EACH PRINTED WIRING BOARD ASSEMBLY. ALL PRINTED WIRING BOARD ASSEMBLIES LOCATE NUMBER 1 IN UPPER LEFT (CONTACT FINGER END) WITH NUMBER 25 IN LOWER RIGHT OF THE ITEM.
3. LOGIC ELEMENT TERMINALS ARE NUMBERED COUNTERCLOCKWISE FROM 1 THROUGH 10 WHEN VIEWED FROM THE TOP. TERMINAL 10 COINCIDES WITH THE KEY.
4. TERMINAL 1 IS GROUND AND TERMINAL 6 IS +5 VOLTS ON ALL LOGIC ELEMENTS.
5. ALL LOGIC CAN POSITIONS ARE USED.
6. RECEPTACLE VIEWED FROM PIN SIDE.

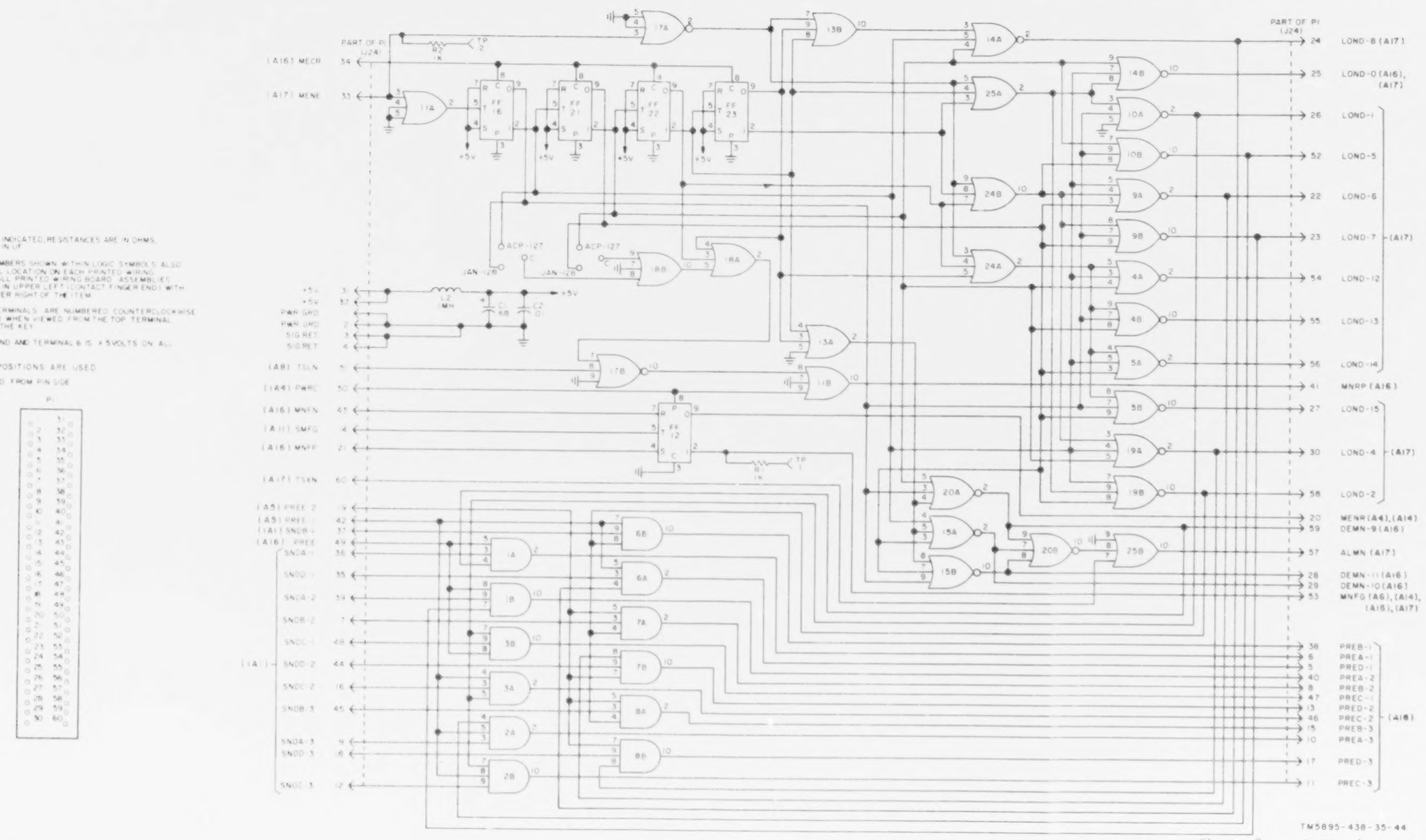
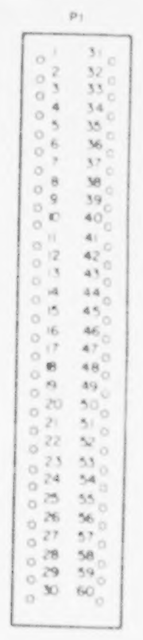

P1
PART OF P1 (J24)
(A18) MBCR
(A17) MCNI
(A8) TLLN
(A4) PWRC
(A18) MNFN
(A17) SNFS
(A18) MNFF
(A17) TSYN
(A5) PREE-2
(A5) PREE
(A17) SNDR-1
(A18) PREE
+5V
PWR GND
SIGRET
ACP-127
JAN-128
FF 18
FF 21
FF 22
FF 23
FF 12
LOND-8 (A17)
LOND-0 (A18), (A17)
LOND-1
LOND-5
LOND-6
LOND-7
LOND-12
LOND-13
LOND-14
MNRP (A18)
LOND-15
LOND-4
LOND-2
MENF (A4), (A14)
DEMN-8 (A18)
ALMN (A17)
DEMN-11 (A18)
DEMN-10 (A18)
MNFG (A8), (A14), (A18), (A17)
PREB-1
PREA-1
PRED-1
PREA-2
PREB-2
PREC-1
PRED-2
PREC-2
PREB-3
PREA-3
PRED-3
PREC-3
(A18)
TM5895-438-35-44

Figure 1-16. 1A2A15, Message Identifier Sequence Generator PL-1151/G schematic diagram.

NOTES

1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UF
2. IDENTIFICATION NUMBERS SHOWN WITHIN LOGIC SYMBOLS ALSO ESTABLISH PHYSICAL LOCATION ON EACH PRINTED WIRING BOARD ASSEMBLY. ALL PRINTED WIRING BOARD ASSEMBLIES LOCATE NUMBER 1 IN UPPER LEFT (CONTACT FINGER END) WITH NUMBER 25 IN LOWER RIGHT OF THE ITEM.
3. LOGIC ELEMENT TERMINALS ARE NUMBERED COUNTERCLOCKWISE FROM 1 THROUGH 10 WHEN VIEWED FROM THE TOP. TERMINAL 10 COINCIDES WITH THE KEY.
4. TERMINAL 1 IS GROUND AND TERMINAL 6 IS +5 VOLTS ON ALL LOGIC ELEMENTS.
5. ALL LOGIC CAN POSITIONS ARE USED.
6. RECEPTACLE VIEWED FROM PIN SIDE.



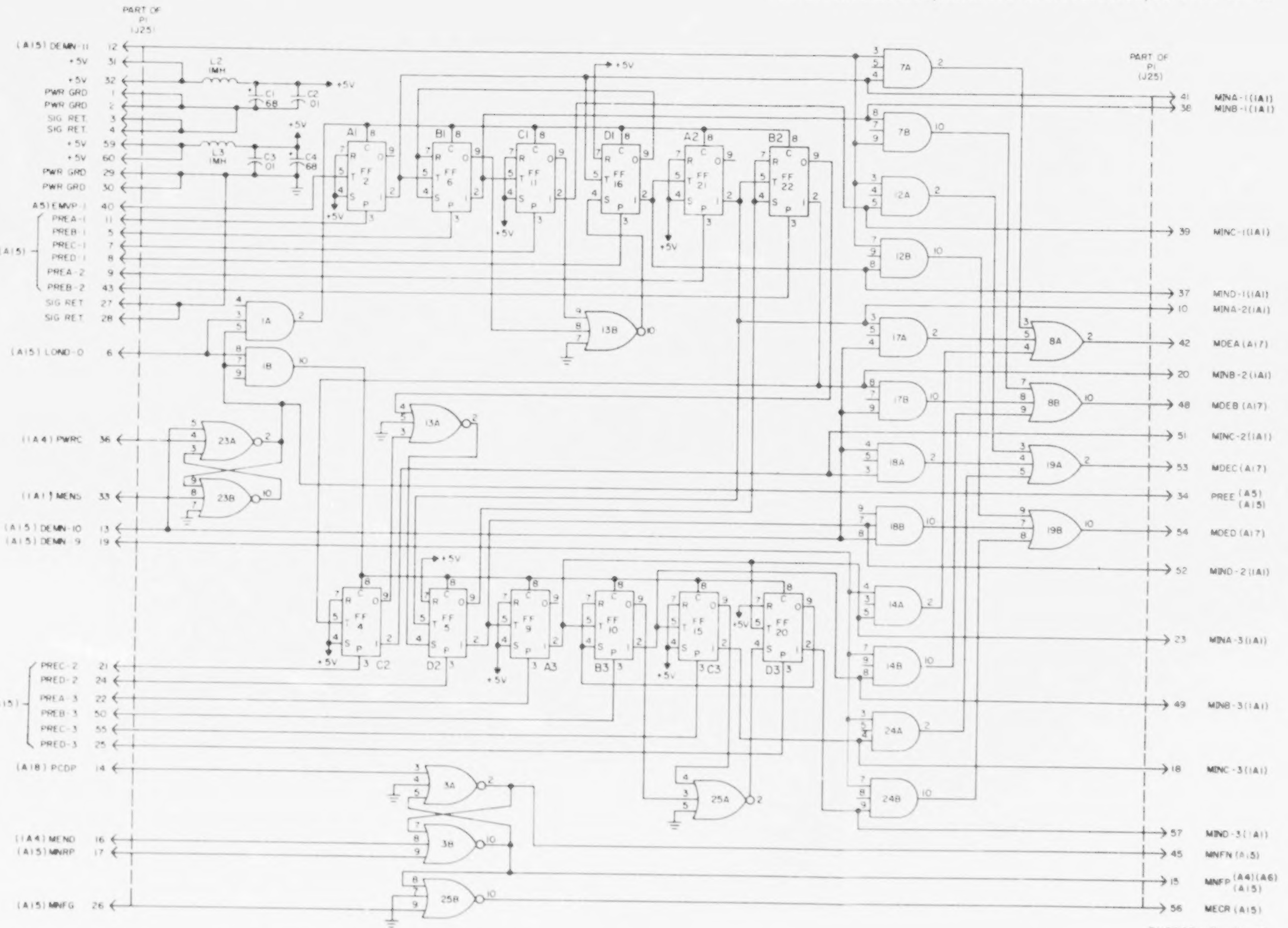
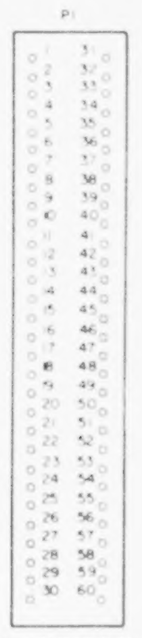


Figure 1-17. 1A2A16, Message Identifier PL-1150/G Decimal Counter, schematic diagram.

NOTES

1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UF.
2. IDENTIFICATION NUMBERS SHOWN WITHIN LOGIC SYMBOLS ALSO ESTABLISH PHYSICAL LOCATION ON EACH PRINTED WIRING BOARD ASSEMBLY. ALL PRINTED WIRING BOARD ASSEMBLIES LOCATE NUMBER 1 IN UPPER LEFT (CONTACT FINGER END) WITH NUMBER 25 IN LOWER RIGHT OF THE ITEM.
3. LOGIC ELEMENT TERMINALS ARE NUMBERED COUNTERCLOCKWISE FROM 1 THROUGH 10 WHEN VIEWED FROM THE TOP. TERMINAL 10 COINCIDES WITH THE KEY.
4. TERMINAL 1 IS GROUND AND TERMINAL 6 IS +5 VOLTS ON ALL LOGIC ELEMENTS.
5. LOGIC CAN POSITIONS 5, 13, 25 ARE NOT USED.
6. RECEPTACLE VIEWED FROM PIN SIDE.

P1


1 31
2 32
3 33
4 34
5 35
6 36
7 37
8 38
9 39
10 40
11 41
12 42
13 43
14 44
15 45
16 46
17 47
18 48
19 49
20 50
21 51
22 52
23 53
24 54
25 55
26 56
27 57
28 58
29 59
30 60

7. GUARD CONDUCTOR NOT CONNECTED TO ANY CIRCUIT ELEMENTS.

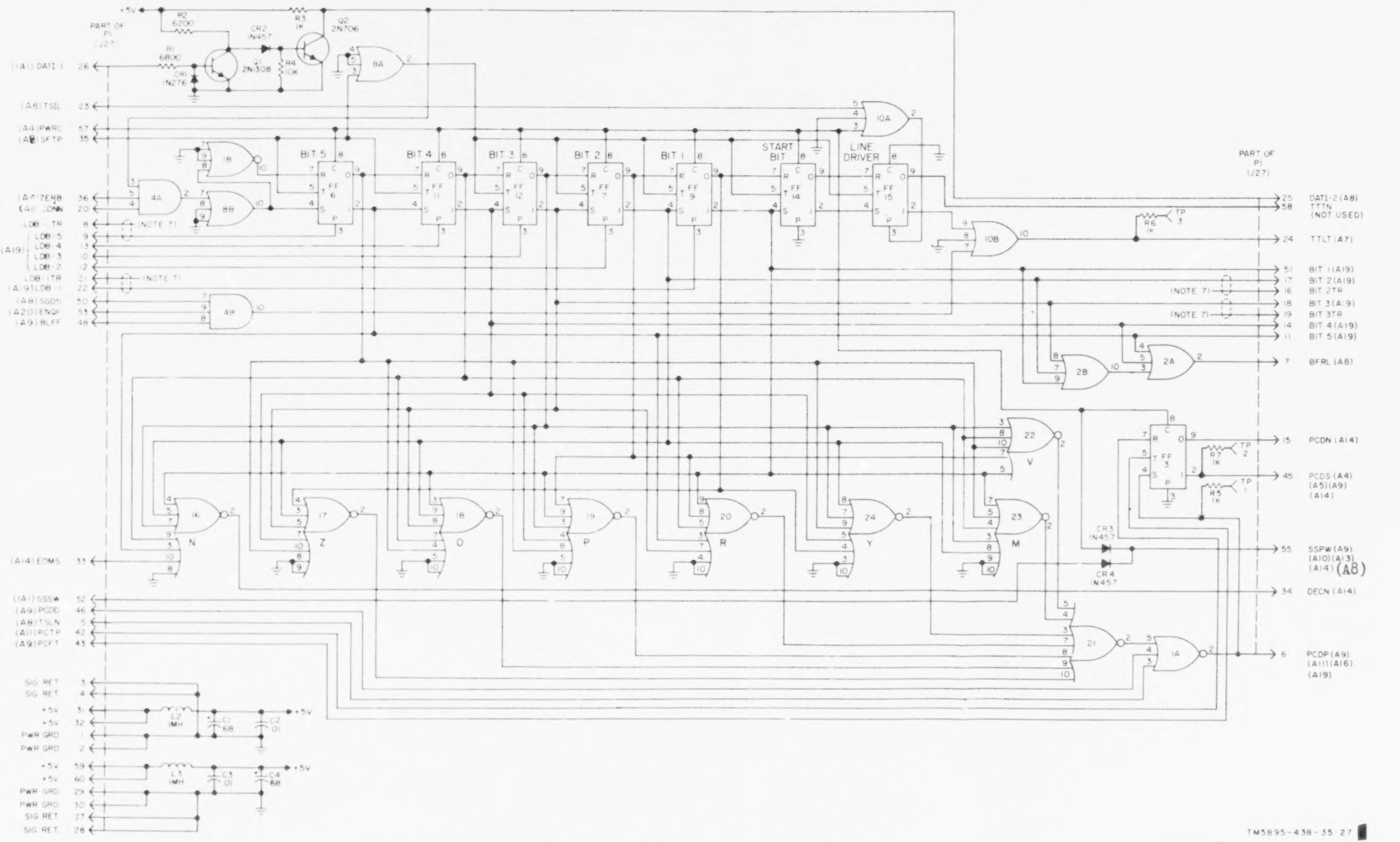

+5V
PART OF P1 (J27)
R2 6200
R1 6800
CR1 1N276
Q1 2N1308
CR2 1N457
R4 10K
R3 1K
Q2 2N706
8A
(1A1) DATI-1 26
(A8) TSIL 23
(A4) PWRC 57
(A8) SFTP 35
(A4) ZERB 36
(A8) CONN 20
LDB - TR 8
(A19) LDB-5 9
LDB-4 13
LDB-3 10
LDB-2 12
LDB-1TR 21
(A19) LDB-1 22
(A8) SGDN 50
(A20) ENQF 53
(A9) BLFF 48
(NOTE 7)
1B
4A
8B
4B
BIT 5
FF 6
BIT 4
FF 11
BIT 3
FF 12
BIT 2
FF 7
BIT 1
FF 9
START BIT
FF 14
LINE DRIVER
FF 15
10A
10B
2A
2B
22
V
FF 3
16
N
17
Z
18
O
19
P
20
R
24
Y
23
M
21
1A
CR3 1N457
CR4 1N457
R6 1K
TP 3
R7 1K
TP 2
R5 1K
TP 1
(A14) EOMS 33
(1A1) SSSW 52
(A9) PCDD 46
(A8) TSLN 5
(A11) PCTP 42
(A9) PCFT 43
SIG RET 3
SIG RET 4
+5V 31
+5V 32
PWR GRD 1
PWR GRD 2
L2 1MH
C1 68
C2 .01
+5V 59
+5V 60
PWR GRD 29
PWR GRD 30
SIG RET 27
SIG RET 28
L3 1MH
C3 .01
C4 68
PART OF P1 (J27)
25 DATI-2 (A8)
58 TTTN (NOT USED)
24 TTLT (A7)
51 BIT 1 (A19)
17 BIT 2 (A19)
16 BIT 2TR
18 BIT 3 (A19)
19 BIT 3TR
14 BIT 4 (A19)
11 BIT 5 (A19)
7 BFRL (A8)
15 PCDN (A14)
45 PCDS (A4) (A5) (A9) (A14)
55 SSPW (A9) (A10) (A13) (A14) (A8)
34 DECN (A14)
6 PCDP (A9) (A11) (A16) (A19)

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Figure 1-18. 1A2A18, Transmit Buffer-Decoder PL-1148/G, schematic diagram.

NOTES

1 UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS. CAPACITANCES ARE IN UF

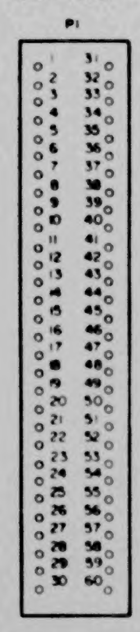
2 IDENTIFICATION NUMBERS SHOWN WITHIN LOGIC SYMBOLS ALSO ESTABLISH PHYSICAL LOCATION ON EACH PRINTED WIRING BOARD ASSEMBLY ALL PRINTED WIRING BOARD ASSEMBLIES LOCATE NUMBER 1 IN UPPER LEFT (CONTACT FINGER END) WITH NUMBER 25 IN LOWER RIGHT OF THE ITEM

3 LOGIC ELEMENT TERMINALS ARE NUMBERED COUNTERCLOCKWISE FROM 1 THROUGH 10 WHEN VIEWED FROM THE TOP TERMINAL 10 COINCIDES WITH THE KEY

4 TERMINAL 1 IS GROUND AND TERMINAL 6 IS +5VOLTS ON ALL LOGIC ELEMENTS

5 LOGIC CAN POSITIONS 3A, 3B, 5A, 5B, 10A, 10B, 20A, 20B ARE NOT USED

6 RECEPTACLE VIEWED FROM PIN SIDE


P1
1 31
2 32
3 33
4 34
5 35
6 36
7 37
8 38
9 39
10 40
11 41
12 42
13 43
14 44
15 45
16 46
17 47
18 48
19 49
20 50
21 51
22 52
23 53
24 54
25 55
26 56
27 57
28 58
29 59
30 60

7 SPRAGUE ELECTRIC, TYPE NUMBER TN-56

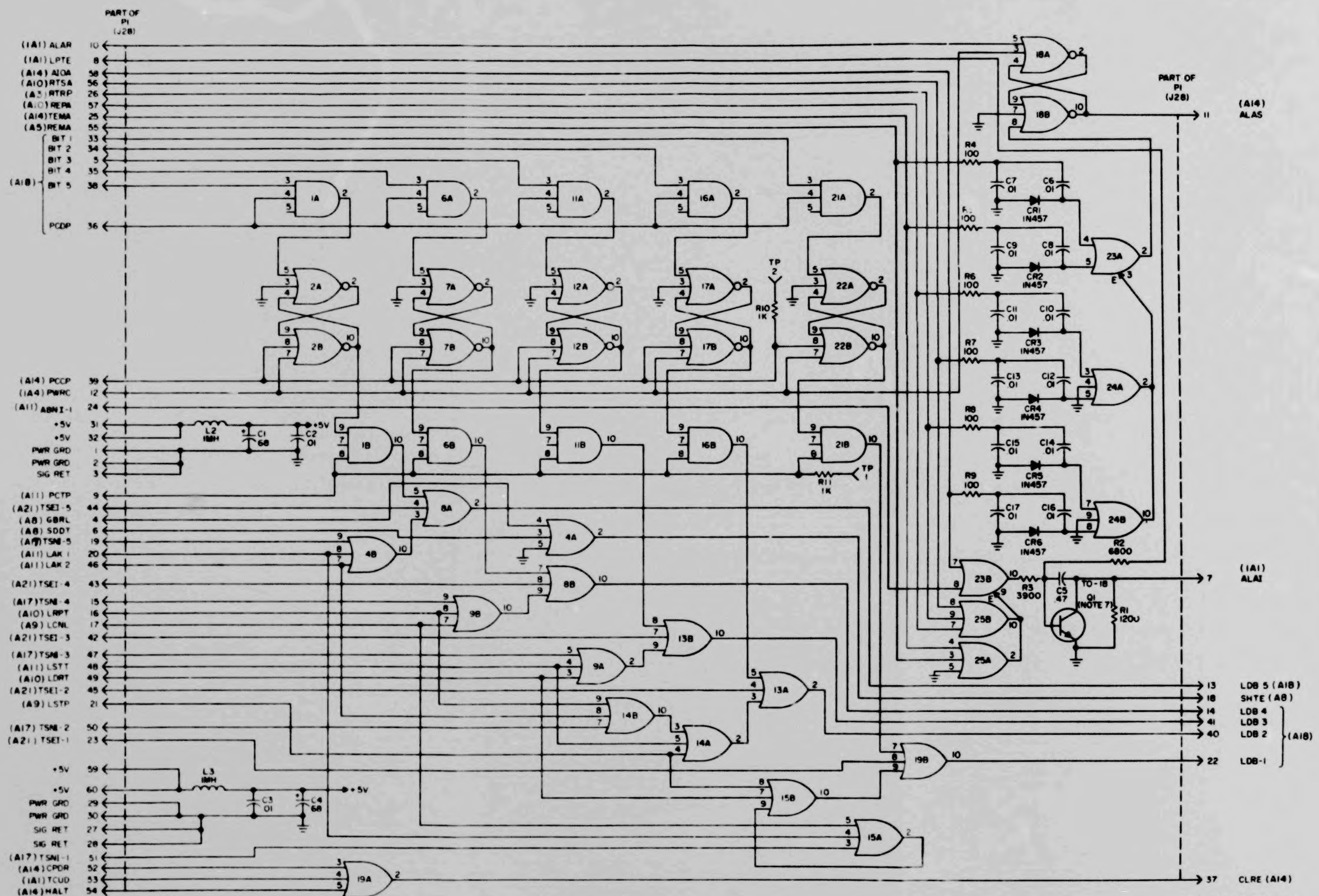
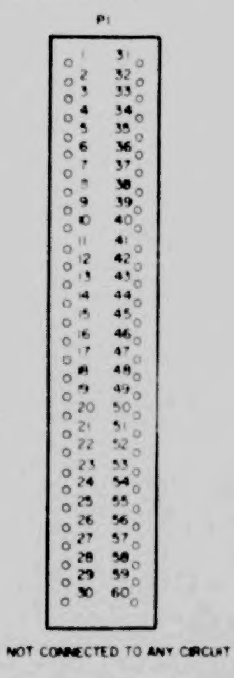

PART OF P1 (J28)
(1A1) ALAR 10
(1A1) LPTE 8
(A14) AIOA 58
(A10) RTSA 56
(A3) RTRP 26
(A10) REPA 57
(A14) TEMA 25
(A5) REMA 55
BIT 1 33
BIT 2 34
BIT 3 5
BIT 4 35
(A18) BIT 5 38
PCDP 36
(A14) PCCP 39
(1A4) PWRC 12
(A11) ABNI-1 24
+5V 31
+5V 32
PWR GRD 1
PWR GRD 2
SIG RET 3
(A11) PCTP 9
(A21) TSEI-5 44
(A8) GBRL 4
(A8) SDDT 6
(A17) TSNI-5 19
(A11) LAK 1 20
(A11) LAK 2 46
(A21) TSEI-4 43
(A17) TSNI-4 15
(A10) LRPT 16
(A9) LCNL 17
(A21) TSEI-3 42
(A17) TSNI-3 47
(A11) LSTT 48
(A10) LDRT 49
(A21) TSEI-2 45
(A9) LSTP 21
(A17) TSNI-2 50
(A21) TSEI-1 23
+5V 59
+5V 60
PWR GRD 29
PWR GRD 30
SIG RET 27
SIG RET 28
(A17) TSNI-1 51
(A14) CPDR 52
(1A1) TCUD 53
(A14) HALT 54
L2 1MH
L3 1MH
C3 .01
C4 68
+5V
1A 6A 11A 16A 21A
2A 7A 12A 17A 22A
2B 7B 12B 17B 22B
1B 6B 11B 16B 21B
8A 4B 4A 8B 9B 13B 9A 13A 14B 14A 15B 15A 19B 19A
18A 18B
23A 24A 24B 23B 25B 25A
TP 1
R10 1K
R11 1K
R4 100
R5 100
R6 100
R7 100
R8 100
R9 100
CR1 1N457
CR2 1N457
CR3 1N457
CR4 1N457
CR5 1N457
CR6 1N457
R2 6800
R3 3900
TO-18
Q1 (NOTE 7)
R1 120U
PART OF P1 (J28)
11 (A14) ALAS
7 (1A1) ALAI
13 LDB 5 (A18)
18 SHTE (A8)
14 LDB 4
41 LDB 3
40 LDB 2
22 LDB-1
(A18)
37 CLRE (A14)
TM5895-438-35-28)

Figure 1-19. 1A2A19, Transmit Character Encoder P1-1156/G, schematic diagram.

NOTES

1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS. CAPACITANCES ARE IN UF
2. IDENTIFICATION NUMBERS SHOWN WITHIN LOGIC SYMBOLS ALSO ESTABLISH PHYSICAL LOCATION ON EACH PRINTED WIRING BOARD ASSEMBLY ALL PRINTED WIRING BOARD ASSEMBLIES LOCATE NUMBER 1 IN UPPER LEFT (CONTACT FINGER END) WITH NUMBER 25 IN LOWER RIGHT OF THE ITEM
3. LOGIC ELEMENT TERMINALS ARE NUMBERED COUNTERCLOCKWISE FROM 1 THROUGH 10 WHEN VIEWED FROM THE TOP TERMINAL 10 COINCIDES WITH THE KEY
4. TERMINAL 1 IS GROUND AND TERMINAL 6 IS +5 VOLTS ON ALL LOGIC ELEMENTS
5. LOGIC CAN POSITIONS 1B, 5, 11, 12B ARE NOT USED
6. RECEPTACLE VIEWED FROM PIN SIDE


P1
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60

7. GUARD CONNECTOR NOT CONNECTED TO ANY CIRCUIT ELEMENTS

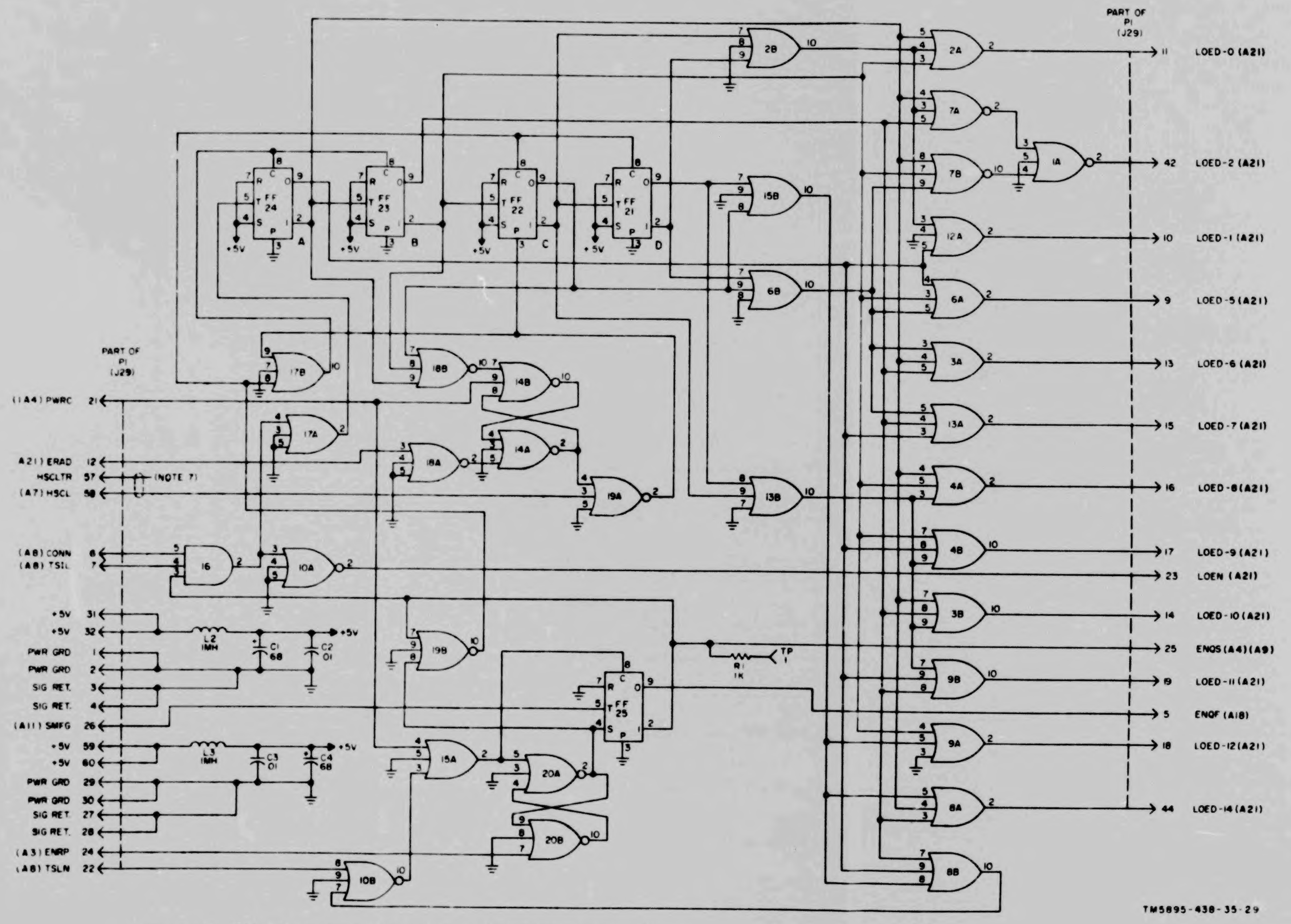

PART OF
P1
(J29)
(1A4) PWRC 21
A21) ERAD 12
HSCLTR 57
(NOTE 7)
(A7) HSCL 58
(A8) CONN 6
(A8) TSIL 7
+5V 31
+5V 32
PWR GRD 1
PWR GRD 2
SIG RET. 3
SIG RET. 4
(A11) SMFG 26
+5V 59
+5V 60
PWR GRD 29
PWR GRD 30
SIG RET. 27
SIG RET. 28
(A3) ENRP 24
(A8) TSLN 22
L2
1MH
L3
1MH
C1
68
C2
.01
C3
.01
C4
68
FF 24
FF 21
FF 22
FF 21
FF 25
A
B
C
D
+5V
R1
1K
TP
17B
17A
18B
18A
14B
14A
19A
16
10A
19B
15A
20A
20B
10B
2B
15B
6B
13B
2A
7A
7B
1A
12A
6A
3A
13A
4A
4B
3B
9B
9A
8A
8B
PART OF
P1
(J29)
11 LOED-0 (A21)
42 LOED-2 (A21)
10 LOED-1 (A21)
9 LOED-5 (A21)
13 LOED-6 (A21)
15 LOED-7 (A21)
16 LOED-8 (A21)
17 LOED-9 (A21)
23 LOEN (A21)
14 LOED-10 (A21)
25 ENQS (A4)(A9)
19 LOED-11 (A21)
5 ENQF (A18)
18 LOED-12 (A21)
44 LOED-14 (A21)
TM5895-438-35-29

Figure 1-20. 2A1, Enquiry Response Sequence Generator PL-1153/G schematic diagram.

NOTES:
1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UF.
2. NO LOGIC CANS USED.
3. RECEPTACLE VIEWED FROM PIN SIDE.

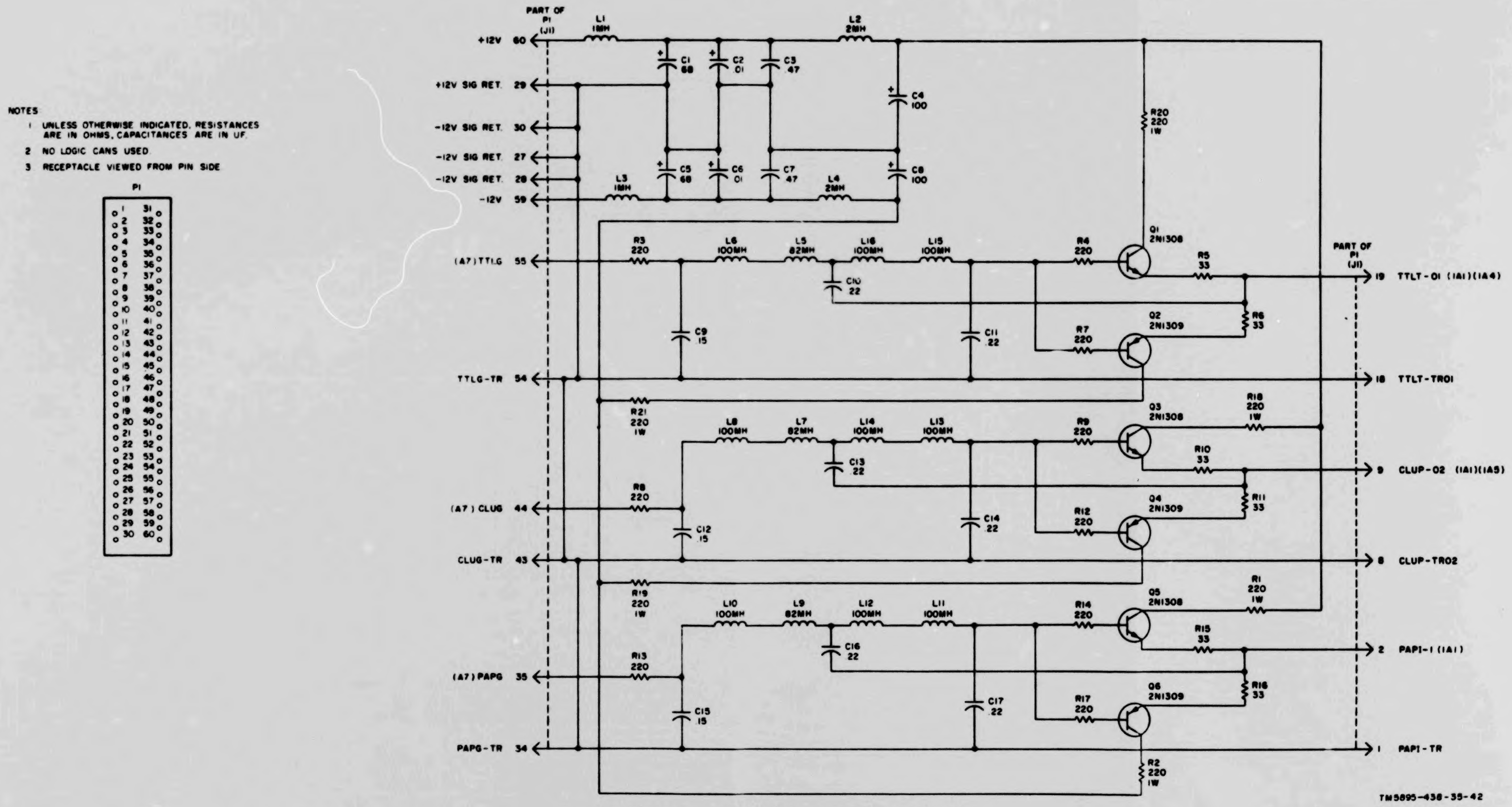

P1
PART OF P1 (J1)
+12V 60
+12V SIG RET. 29
-12V SIG RET. 30
-12V SIG RET. 27
-12V SIG RET. 28
-12V 59
(A7) TTLG 55
TTLG-TR 54
(A7) CLUG 44
CLUG-TR 43
(A7) PAPG 35
PAPG-TR 34
L1 1MH
L2 2MH
L3 1MH
L4 2MH
C1 68
C2 .01
C3 .47
C4 100
C5 68
C6 .01
C7 .47
C8 100
R3 220
L6 100MH
L5 82MH
L16 100MH
L15 100MH
C10 22
C9 .15
C11 .22
R21 220 1W
L8 100MH
L7 82MH
L14 100MH
L13 100MH
C13 .22
R8 220
C12 .15
C14 .22
R19 220 1W
L10 100MH
L9 82MH
L12 100MH
L11 100MH
C16 22
R13 220
C15 .15
C17 .22
R20 220 1W
Q1 2N1308
R4 220
R5 33
R6 33
Q2 2N1309
R7 220
Q3 2N1308
R9 220
R18 220 1W
R10 33
R11 33
Q4 2N1309
R12 220
Q5 2N1308
R14 220
R1 220 1W
R15 33
R16 33
Q6 2N1309
R17 220
R2 220 1W
19 TTLT-01 (1A1)(1A4)
18 TTLT-TR01
9 CLUP-02 (1A1)(1A5)
8 CLUP-TR02
2 PAPI-1 (1A1)
1 PAPI-TR
TM5895-438-35-42

Figure 1-81. 1A2A1, Transmit Line Filter Driver, schematic diagram.

NOTES

1 UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS. CAPACITANCES ARE IN UF

2 IDENTIFICATION NUMBERS SHOWN WITHIN LOGIC SYMBOLS ALSO ESTABLISH PHYSICAL LOCATION ON EACH PRINTED WIRING BOARD ASSEMBLY. ALL PRINTED WIRING BOARD ASSEMBLIES LOCATE NUMBER 1 IN UPPER LEFT (CONTACT FINGER END) WITH NUMBER 25 IN LOWER RIGHT OF THE ITEM

3 LOGIC ELEMENT TERMINALS ARE NUMBERED COUNTERCLOCKWISE FROM 1 THROUGH 10 WHEN VIEWED FROM THE TOP. TERMINAL 10 COINCIDES WITH THE KEY

4 TERMINAL 1 IS GROUND AND TERMINAL 6 IS +5VOLTS ON ALL LOGIC ELEMENTS

5 RECEPTACLE VIEWED FROM PIN SIDE

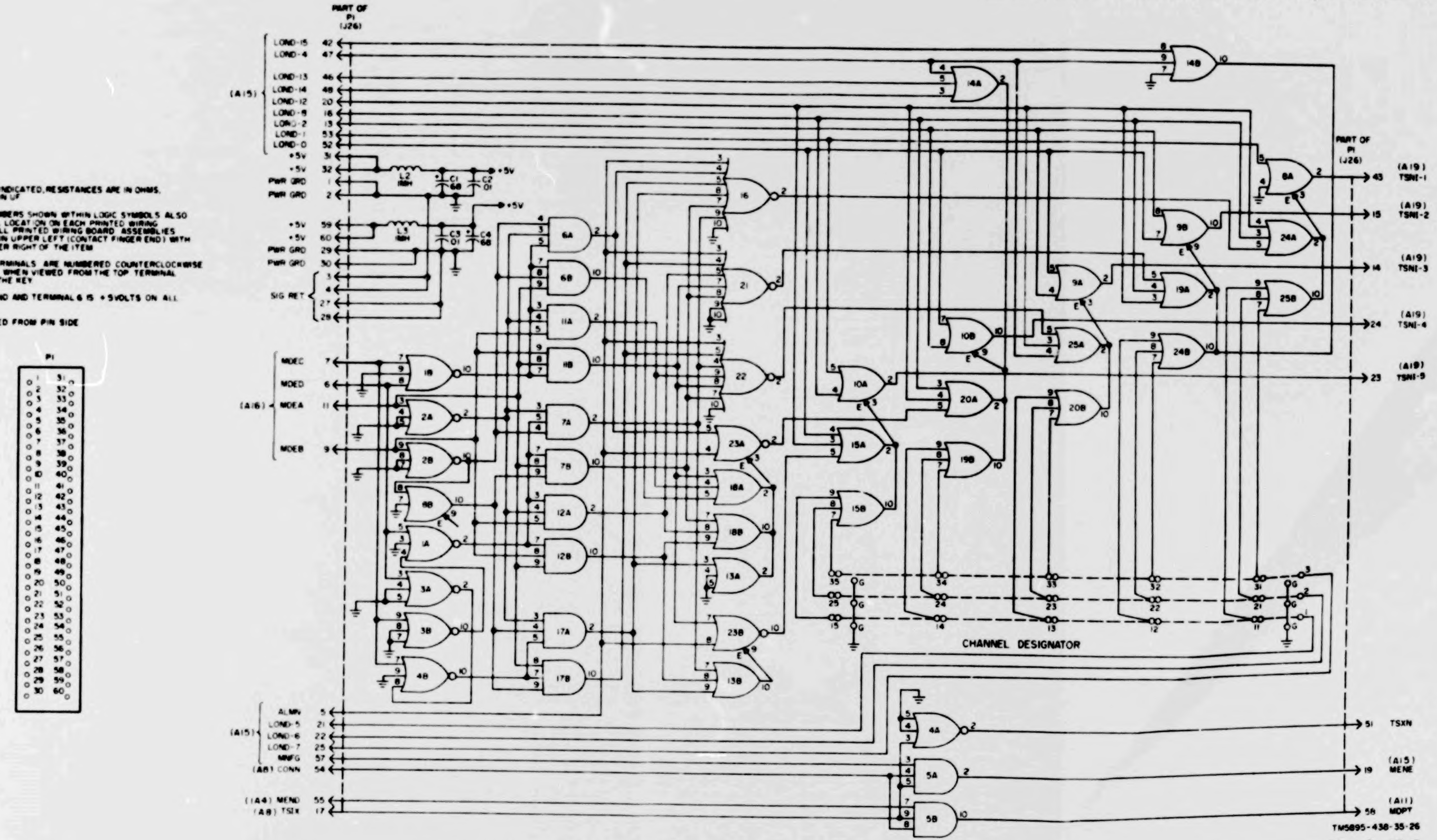
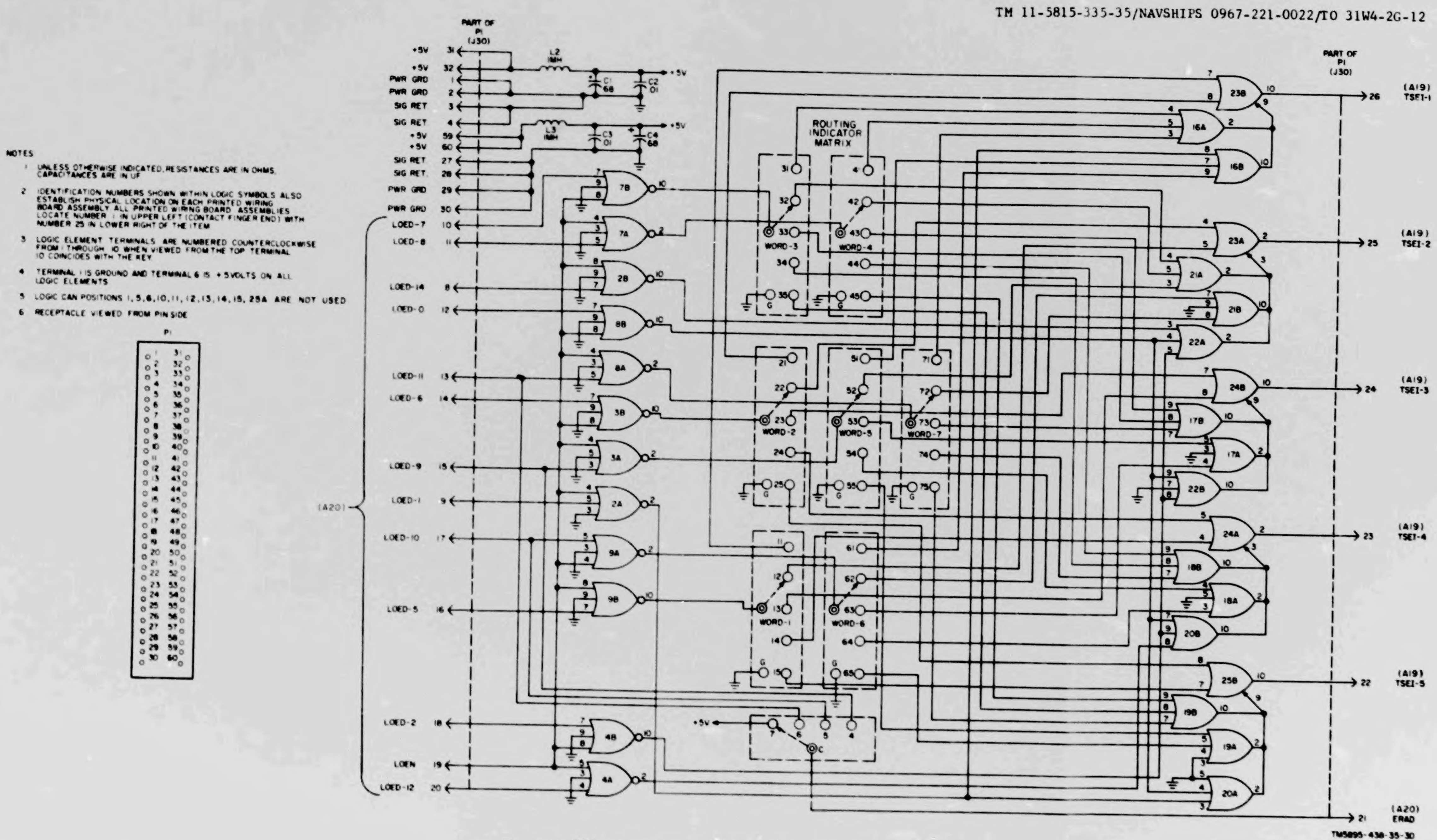

P1
PART OF P1 (J26)
(A15)
LOND-15
LOND-4
LOND-13
LOND-14
LOND-12
LOND-9
LOND-2
LOND-1
LOND-0
+5V
PWR GRD
SIG RET
(A16)
MOEC
MOED
MOEA
MOEB
CHANNEL DESIGNATOR
(A19) TSNE-1
(A19) TSNE-2
(A19) TSNE-3
(A19) TSNE-4
(A19) TSNE-5
ALMN
(A8) CONN
(A4) MENE
(A8) TSXN
51 TSXN
(A15) 19 MENE
(A11) 58 MOPT
TM5895-438-35-26

Figure 1-22. 1A2A17, Message Identifier, Binary-Baudot PL-1149/G, schematic diagram.


PART OF P1 (J30)
+5V 31
+5V 32
PWR GRD 1
PWR GRD 2
SIG RET 3
SIG RET 4
+5V 59
+5V 60
SIG RET 27
SIG RET 28
PWR GRD 29
PWR GRD 30
LOED-7 10
LOED-8 11
LOED-14 8
LOED-0 12
LOED-11 13
LOED-6 14
LOED-9 15
LOED-1 9
LOED-10 17
LOED-5 16
LOED-2 18
LOEN 19
LOED-12 20
(A20)
L2
L3
C1 68
C2 .01
C3 .01
C4 68
+5V
ROUTING INDICATOR MATRIX
WORD-1
WORD-2
WORD-3
WORD-4
WORD-5
WORD-6
WORD-7
7B
7A
2B
8B
6A
3B
3A
2A
9A
9B
4B
4A
23B
16A
16B
25A
21A
21B
22A
24B
17B
17A
22B
24A
18B
18A
20B
25B
19B
19A
20A
PART OF P1 (J30)
26 (A19) TSEI-1
25 (A19) TSEI-2
24 (A19) TSEI-3
23 (A19) TSEI-4
22 (A19) TSEI-5
21 (A20) ERAD
P1

NOTES

1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS. CAPACITANCES ARE IN UF.
2. IDENTIFICATION NUMBERS SHOWN WITHIN LOGIC SYMBOLS ALSO ESTABLISH PHYSICAL LOCATION ON EACH PRINTED WIRING BOARD ASSEMBLY. ALL PRINTED WIRING BOARD ASSEMBLIES LOCATE NUMBER 1 IN UPPER LEFT (CONTACT FINGER END) WITH NUMBER 25 IN LOWER RIGHT OF THE ITEM.
3. LOGIC ELEMENT TERMINALS ARE NUMBERED COUNTERCLOCKWISE FROM 1 THROUGH 10 WHEN VIEWED FROM THE TOP. TERMINAL 10 COINCIDES WITH THE KEY.
4. TERMINAL 1 IS GROUND AND TERMINAL 6 IS +5VOLTS ON ALL LOGIC ELEMENTS.
5. LOGIC CAN POSITIONS 1, 5, 6, 10, 11, 12, 13, 14, 15, 25A ARE NOT USED.
6. RECEPTACLE VIEWED FROM PIN SIDE.

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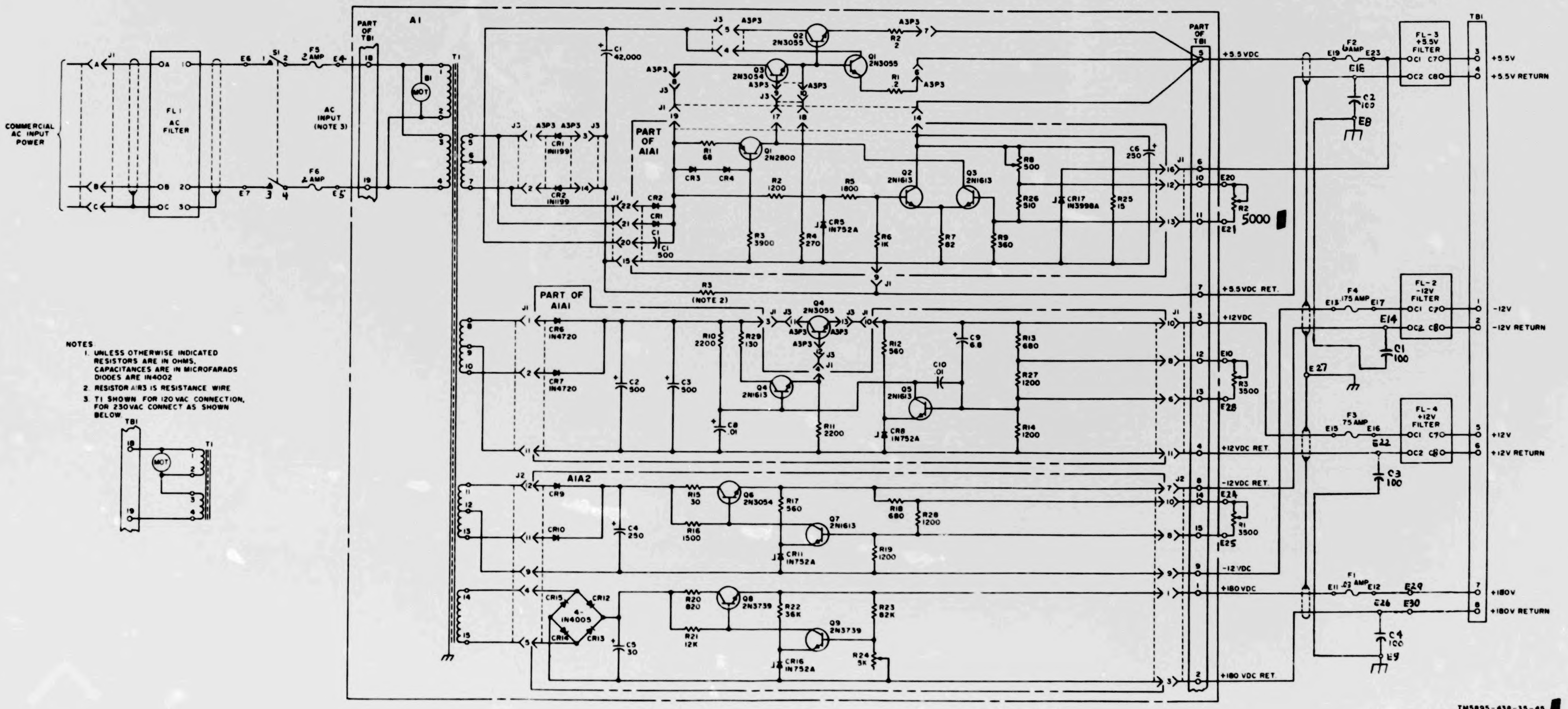
Figure 1-23. 2A2, Enquiry Response Encoder PL-1155/G, schematic diagram.


COMMERCIAL AC INPUT POWER
J1
A
B
C
FL1 AC FILTER
E6
E7
S1
F5 2 AMP
F6 2 AMP
E4
E5
AC INPUT (NOTE 3)
PART OF TB1
18
19
A1
B1 MOT
T1
C1 42,000
J3
A3P3
CR1 1N1199
CR2 1N1199
PART OF A1A1
R1 68
Q1 2N2800
CR3
CR4
R2 1200
R5 1800
R3 3900
R4 270
CR5 1N752A
R6 1K
Q2 2N1613
Q3 2N1613
R7 82
R8 500
R26 510
CR17 1N3998A
R25 15
R9 360
C6 250
C1 500
Q2 2N3055
Q1 2N3055
Q3 2N3054
R2 2
R1 .2
R3 (NOTE 2)
PART OF A1A1
CR6 1N4720
CR7 1N4720
C2 500
C3 500
R10 2200
R29 130
Q4 2N3055
Q4 2N1613
C8 .01
R11 2200
R12 560
C9 6.8
C10 .01
Q5 2N1613
CR8 1N752A
R13 680
R27 1200
R14 1200
A1A2
J2
CR9
CR10
C4 250
R15 30
R16 1500
Q6 2N3054
R17 560
Q7 2N1613
CR11 1N752A
R18 680
R28 1200
R19 1200
CR15
CR12
CR14
CR13
4-1N4005
C5 30
R20 820
R21 12K
Q8 2N3739
R22 36K
Q9 2N3739
CR16 1N752A
R23 82K
R24 5K
PART OF TB1
+5.5 VDC
+5.5VDC RET.
+12VDC
+12VDC RET.
-12VDC RET.
-12 VDC
+180 VDC
+180 VDC RET.
E20
R2 5000
E21
E10
R3 3500
E28
E24
R1 3500
E25
F2 6AMP
E19
E23
E16
C2 100
E8
FL-3 +5.5V FILTER
C1 C7
C2 C8
F4 .175 AMP
E13
E17
E14
C1 100
E27
FL-2 -12V FILTER
F3 .75 AMP
E15
E16
E22
C3 100
FL-4 +12V FILTER
F1 .03 AMP
E11
E12
E29
E26
E30
C4 100
E9
TB1
+5.5V
+5.5V RETURN
-12V
-12V RETURN
+12V
+12V RETURN
+180V
+180V RETURN
TB1
MOT
T1

NOTES

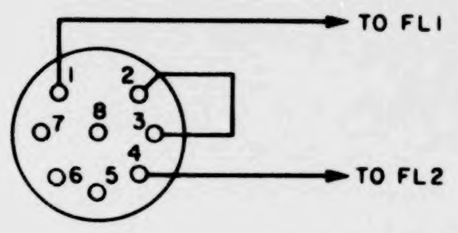
1. UNLESS OTHERWISE INDICATED RESISTORS ARE IN OHMS. CAPACITANCES ARE IN MICROFARADS DIODES ARE IN4002
2. RESISTOR A1R3 IS RESISTANCE WIRE
3. T1 SHOWN FOR 120 VAC CONNECTION, FOR 230VAC CONNECT AS SHOWN BELOW

Figure 1-24. [A3] Power supply and filter assembly, schematic diagram.

TM5895-438-35-45

NOTES:

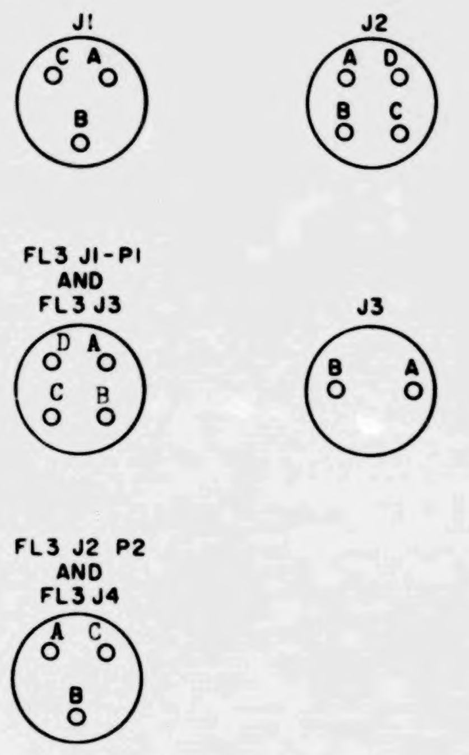
1. (a) POVER SUPPLY SHOWN WIRED FOR 120V OPERATION.
   (b) FOR 230V OPERATION WIRE AS SHOWN BELOW FOR AFFECTED TERMINALS 1,2, 3 AND 4. ALL REMAINING TERMINALS STAY AS BEFORE.



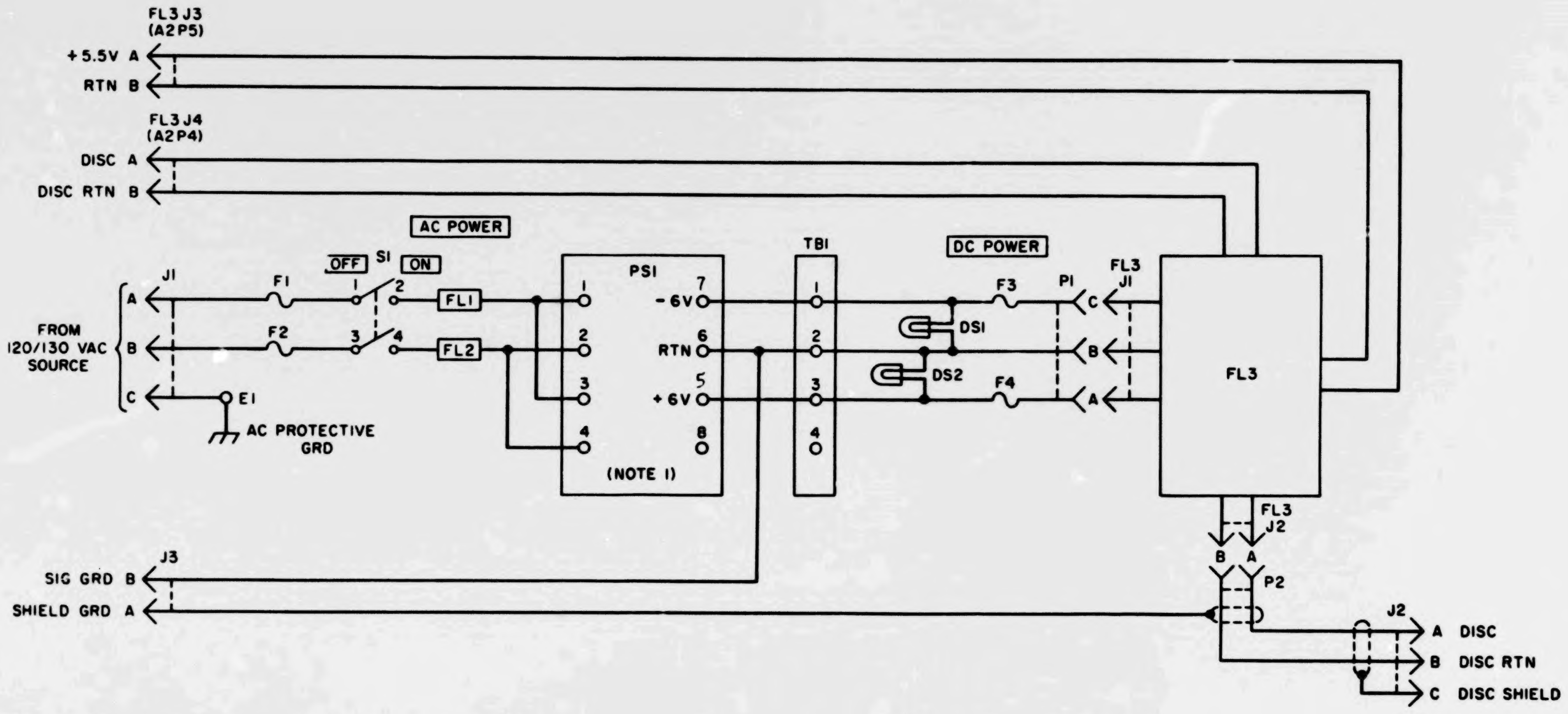
TO FL1
1
2
7
8
3
4
6
5
TO FL2

   (c) FOR 120V OPERATION F1 AND F2 ARE .125 AMP FUSES. FOR 230V OPERATION F1 AND F2 ARE .062 AMP FUSES

2. NUMBERING OF CONNECTORS SHOWN BELOW.



J1
C A
B
J2
A D
B C
FL3 J1-P1 AND FL3 J3
D A
C B
J3
B A
FL3 J2 P2 AND FL3 J4
A C
B



FL3 J3 (A2P5)
+5.5V A
RTN B
FL3 J4 (A2P4)
DISC A
DISC RTN B
AC POWER
OFF
S1
ON
FROM 120/130 VAC SOURCE
J1
A
B
C
F1
F2
1
2
3
4
FL1
FL2
E1
AC PROTECTIVE GRD
PS1
1
2
3
4
7
-6V
6
RTN
5
+6V
8
(NOTE 1)
TB1
1
2
3
4
DC POWER
DS1
DS2
F3
F4
P1
FL3 J1
C
B
A
FL3
FL3 J2
B
A
P2
J3
SIG GRD B
SHIELD GRD A
J2
A DISC
B DISC RTN
C DISC SHIELD

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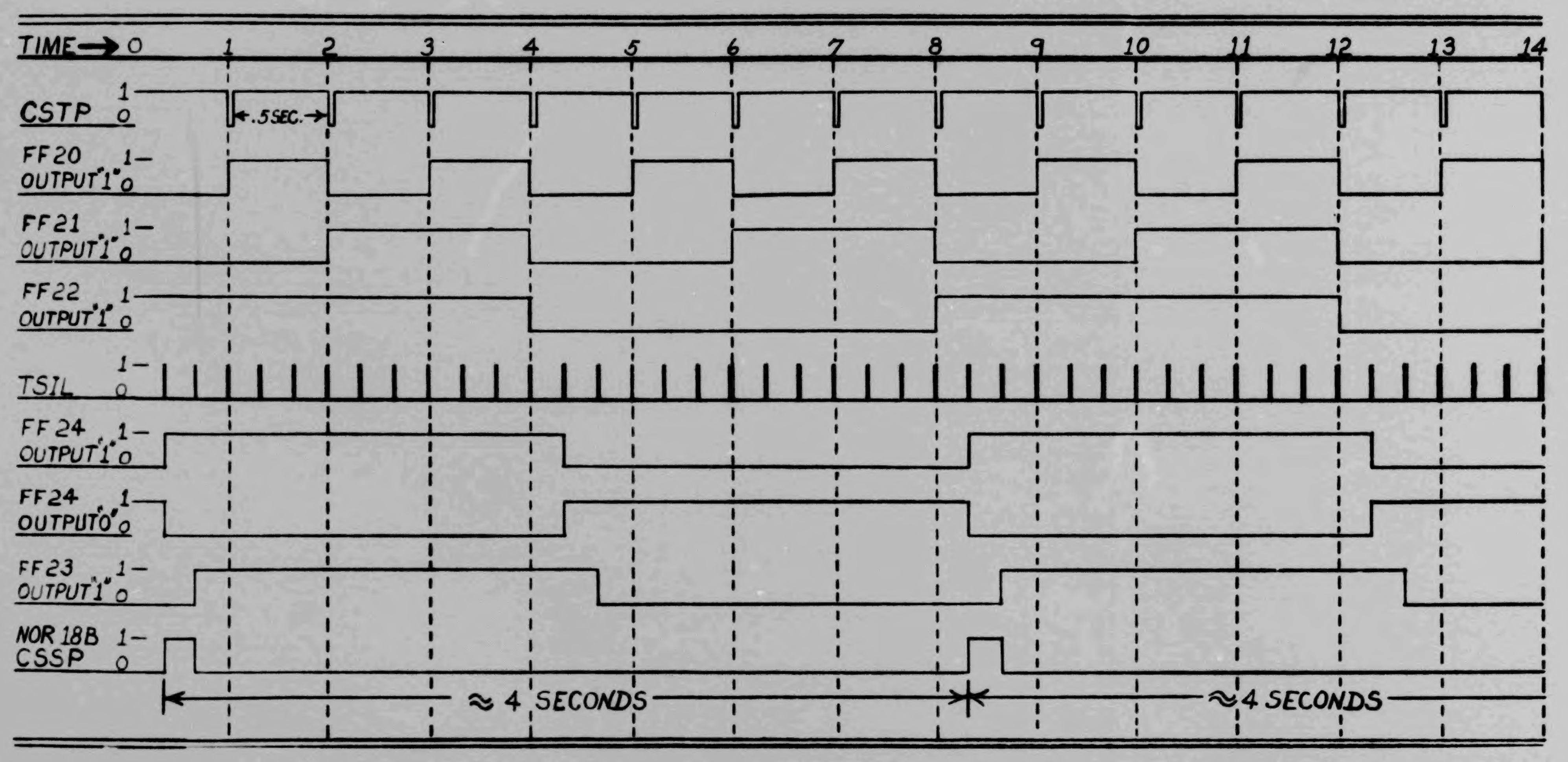
Figure 1-25. Isolator Assembly 2A6, schematic diagram.


TIME → 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14
CSTP 1 0
← .5 SEC. →
FF20 OUTPUT "1" 1 0
FF21 OUTPUT "1" 1 0
FF22 OUTPUT "1" 1 0
TSIL 1 0
FF24 OUTPUT "1" 1 0
FF24 OUTPUT "0" 1 0
FF23 OUTPUT "1" 1 0
NOR 18B CSSP 1 0
≈ 4 SECONDS
≈ 4 SECONDS

NOTES:

1. PREREQUISITES FOR CSSP GENERATION ARE FLGS (0) AND MENR (1); (NO FLAG SET/NO MSG HEADER SET).

2. CSSP SAMPLES THE "TOGGLE" INPUT OF THOSE FLIP FLOPS THAT ARE ASSOCIATED WITH THE GENERATION OF A "CONTROL CHARACTER SEQUENCE FLAG". IF A LOGIC "1" IS PRESENT ON THE "SET" INPUT OF A PARTICULAR FLIP FLOP, CSSP WILL TOGGLE THAT FLIP FLOP TO THE SET STATE. ONCE ANY FLAG IS SET, IT WILL BE ACTED UPON IN ACCORDANCE WITH THE INTERNAL PRIORITY OF THE TCU.

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Figure 1-27. Control sequence synchronization pulse (CSSP) timing chart.

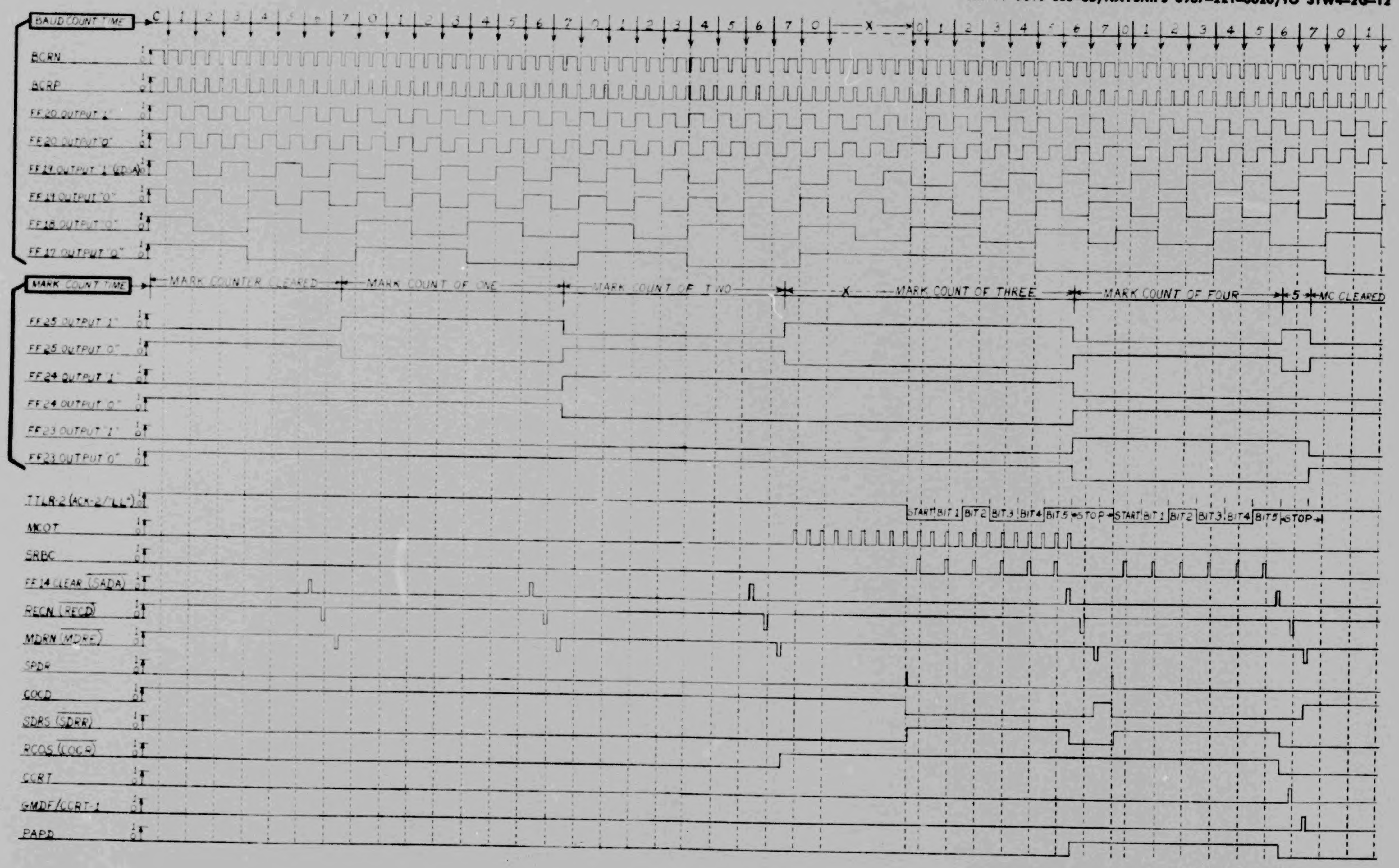
BAUD COUNT TIME
BCRN
BCRP
FF 20 OUTPUT "1"
FF 20 OUTPUT "0"
FF 19 OUTPUT "1" (EDSA)
FF 19 OUTPUT "0"
FF 18 OUTPUT "0"
FF 17 OUTPUT "0"
MARK COUNT TIME
MARK COUNTER CLEARED
MARK COUNT OF ONE
MARK COUNT OF TWO
X
MARK COUNT OF THREE
MARK COUNT OF FOUR
5
MC CLEARED
FF 25 OUTPUT "1"
FF 25 OUTPUT "0"
FF 24 OUTPUT "1"
FF 24 OUTPUT "0"
FF 23 OUTPUT "1"
FF 23 OUTPUT "0"
TTLR-2 (ACK-2/"LL")
MCOT
SRBC
FF 14 CLEAR (SADA)
RECN (RECD)
MDRN (MDRE)
SPDR
COCD
SDRS (SDRR)
RCOS (COCR)
CCRT
GMDF/CCRT-1
PAPD
START
BIT 1
BIT 2
BIT 3
BIT 4
BIT 5
STOP
1
0

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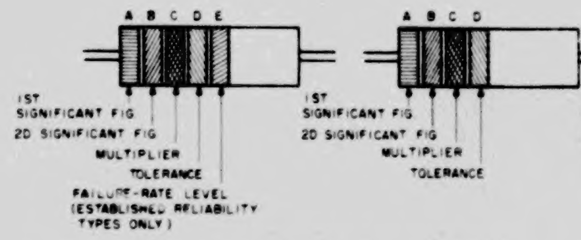
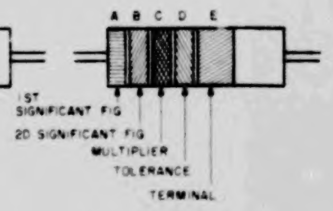
Figure 1-28. Receive baud counter/mark interval timing chart.


A B C D E
1ST SIGNIFICANT FIG
2D SIGNIFICANT FIG
MULTIPLIER
TOLERANCE
FAILURE-RATE LEVEL (ESTABLISHED RELIABILITY TYPES ONLY)
A B C D
1ST SIGNIFICANT FIG
2D SIGNIFICANT FIG
MULTIPLIER
TOLERANCE

COLOR CODE MARKING FOR COMPOSITION TYPE RESISTORS


A B C D E
1ST SIGNIFICANT FIG
2D SIGNIFICANT FIG
MULTIPLIER
TOLERANCE
TERMINAL

COLOR-CODE MARKING FOR FILM-TYPE RESISTORS

TABLE 1
COLOR CODE FOR COMPOSITION TYPE AND FILM TYPE RESISTORS

BAND A		BAND B		BAND C		BAND D		BAND E		
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)	COLOR	FAILURE RATE LEVEL	TERM
BLACK	0	BLACK	0	BLACK	1			BROWN	W=1.0	
BROWN	1	BROWN	1	BROWN	10			RED	P=0.1	
RED	2	RED	2	RED	100			ORANGE	R=0.01	
ORANGE	3	ORANGE	3	ORANGE	1,000			YELLOW	S=0.001	
YELLOW	4	YELLOW	4	YELLOW	10,000	SILVER	±10 (COMP TYPE ONLY)	WHITE		SOLDERABLE
GREEN	5	GREEN	5	GREEN	100,000	GOLD	±5			
BLUE	6	BLUE	6	BLUE	1,000,000	RED	±2 (NOT APPLICABLE TO ESTABLISHED RELIABILITY)			
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7							
GRAY	8	GRAY	8	SILVER	0.01					
WHITE	9	WHITE	9	GOLD	0.1					

BAND A — THE FIRST SIGNIFICANT FIGURE OF THE RESISTANCE VALUE (BANDS A THRU D SHALL BE OF EQUAL WIDTH)

BAND B — THE SECOND SIGNIFICANT FIGURE OF THE RESISTANCE VALUE

BAND C — THE MULTIPLIER (THE MULTIPLIER IS THE FACTOR BY WHICH THE TWO SIGNIFICANT FIGURES ARE MULTIPLIED TO YIELD THE NOMINAL RESISTANCE VALUE)

BAND D — THE RESISTANCE TOLERANCE

BAND E — WHEN USED ON COMPOSITION RESISTORS, BAND E INDICATES ESTABLISHED RELIABILITY FAILURE-RATE LEVEL (PERCENT FAILURE PER 1,000 HOURS) ON FILM RESISTORS, THIS BAND SHALL BE APPROXIMATELY 1-1/2 TIMES THE WIDTH OF OTHER BANDS, AND INDICATES TYPE OF TERMINAL

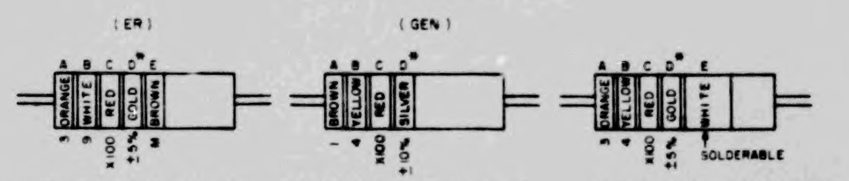
RESISTANCES IDENTIFIED BY NUMBERS AND LETTERS
(THESE ARE NOT COLOR CODED)

SOME RESISTORS ARE IDENTIFIED BY THREE OR FOUR DIGIT ALPHA NUMERIC DESIGNATORS. THE LETTER R IS USED IN PLACE OF A DECIMAL POINT WHEN FRACTIONAL VALUES OF AN OHM ARE EXPRESSED. FOR EXAMPLE

2R7 = 2.7 OHMS   10R0 = 10.0 OHMS

FOR WIRE-WOUND-TYPE RESISTORS COLOR CODING IS NOT USED. IDENTIFICATION MARKING IS SPECIFIED IN EACH OF THE APPLICABLE SPECIFICATIONS

EXAMPLES OF COLOR CODING


(ER)
(GEN)
A B C D* E
ORANGE
WHITE
RED
GOLD
BROWN
3
9
x100
±5%
M
A B C D*
BROWN
YELLOW
RED
SILVER
1
4
x100
±10%
A B C D* E
ORANGE
YELLOW
RED
GOLD
WHITE
3
4
x100
±5%
SOLDERABLE

NOMINAL RESISTANCE 3,900 OHMS
RESISTANCE TOLERANCE ±5%
FAILURE RATE LEVEL M

NOMINAL RESISTANCE 1,400 OHMS
RESISTANCE TOLERANCE ±10%

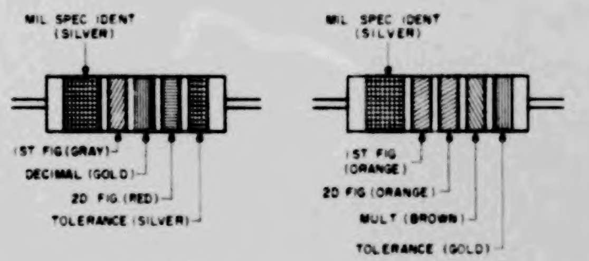
NOMINAL RESISTANCE 3,400 OHMS
RESISTANCE TOLERANCE ±5%
TERMINAL SOLDERABLE

COMPOSITION-TYPE RESISTORS

FILM-TYPE RESISTORS

* IF BAND D IS OMITTED, THE RESISTOR TOLERANCE IS ±20%, AND THE RESISTOR IS NOT MIL-STD

A. COLOR CODE MARKING FOR MILITARY STANDARD RESISTORS


MIL SPEC IDENT (SILVER)
1ST FIG (GRAY)
DECIMAL (GOLD)
2D FIG (RED)
TOLERANCE (SILVER)
MIL SPEC IDENT (SILVER)
1ST FIG (ORANGE)
2D FIG (ORANGE)
MULT (BROWN)
TOLERANCE (GOLD)

(A) 8.2UH ±10%   (B) 330UH ±5%

COLOR CODING FOR TUBULAR ENCAPSULATED RF CHOKES. AT A, AN EXAMPLE OF OF THE CODING FOR AN 8.2UH CHOKE IS GIVEN. AT B, THE COLOR BANDS FOR A 330UH INDUCTOR ARE ILLUSTRATED

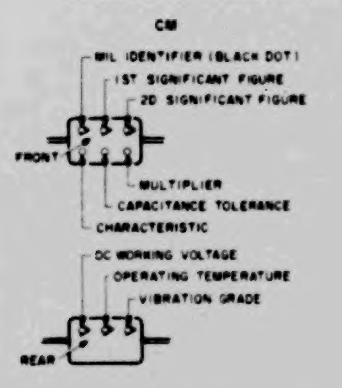
TABLE 2
COLOR CODING FOR TUBULAR ENCAPSULATED RF CHOKES

COLOR	SIGNIFICANT FIGURE	MULTIPLIER	INDUCTANCE TOLERANCE (PERCENT)
BLACK	0	1	
BROWN	1	10	1
RED	2	100	2
ORANGE	3	1,000	3
YELLOW	4		
GREEN	5		
BLUE	6		
VIOLET	7		
GRAY	8		
WHITE	9		
NONE			20
SILVER			10
GOLD	DECIMAL POINT		5

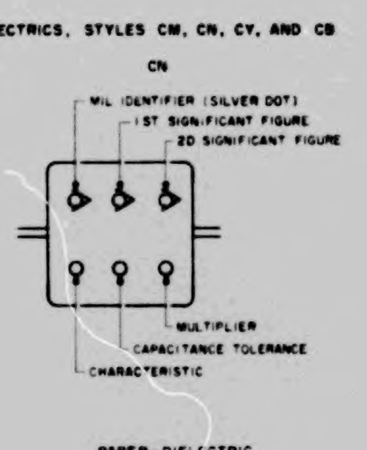
MULTIPLIER IS THE FACTOR BY WHICH THE TWO COLOR FIGURES ARE MULTIPLIED TO OBTAIN THE INDUCTANCE VALUE OF THE CHOKE COIL

B. COLOR CODE MARKING FOR MILITARY STANDARD INDUCTORS

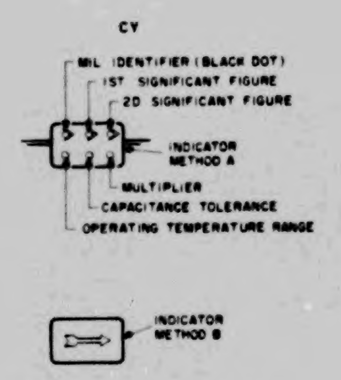
CAPACITORS, FIXED, VARIOUS-DIELECTRICS, STYLES CM, CN, CY, AND CB


CM
MIL IDENTIFIER (BLACK DOT)
1ST SIGNIFICANT FIGURE
2D SIGNIFICANT FIGURE
FRONT
MULTIPLIER
CAPACITANCE TOLERANCE
CHARACTERISTIC
DC WORKING VOLTAGE
OPERATING TEMPERATURE
VIBRATION GRADE
REAR

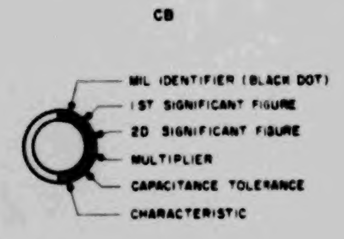
MICA-DIELECTRIC


CN
MIL IDENTIFIER (SILVER DOT)
1ST SIGNIFICANT FIGURE
2D SIGNIFICANT FIGURE
MULTIPLIER
CAPACITANCE TOLERANCE
CHARACTERISTIC

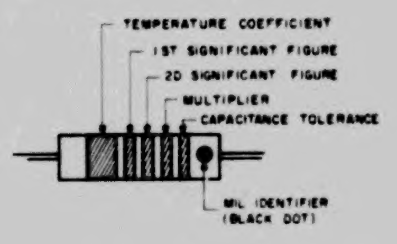
PAPER-DIELECTRIC


CY
MIL IDENTIFIER (BLACK DOT)
1ST SIGNIFICANT FIGURE
2D SIGNIFICANT FIGURE
INDICATOR METHOD A
MULTIPLIER
CAPACITANCE TOLERANCE
OPERATING TEMPERATURE RANGE
INDICATOR METHOD B

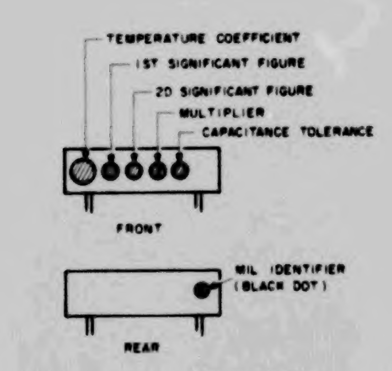
GLASS-DIELECTRIC, GLASS CASE


CB
MIL IDENTIFIER (BLACK DOT)
1ST SIGNIFICANT FIGURE
2D SIGNIFICANT FIGURE
MULTIPLIER
CAPACITANCE TOLERANCE
CHARACTERISTIC

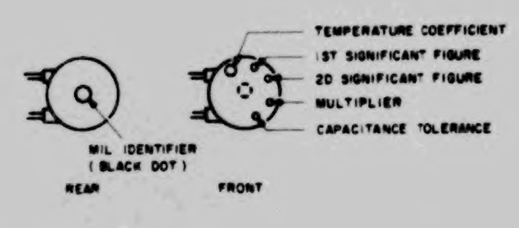
MICA, BUTTON TYPE


TEMPERATURE COEFFICIENT
1ST SIGNIFICANT FIGURE
2D SIGNIFICANT FIGURE
MULTIPLIER
CAPACITANCE TOLERANCE
MIL IDENTIFIER (BLACK DOT)

AXIAL LEAD


TEMPERATURE COEFFICIENT
1ST SIGNIFICANT FIGURE
2D SIGNIFICANT FIGURE
MULTIPLIER
CAPACITANCE TOLERANCE
FRONT
MIL IDENTIFIER (BLACK DOT)
REAR

RADIAL LEAD


TEMPERATURE COEFFICIENT
1ST SIGNIFICANT FIGURE
2D SIGNIFICANT FIGURE
MULTIPLIER
CAPACITANCE TOLERANCE
MIL IDENTIFIER (BLACK DOT)
REAR
FRONT

DISK-TYPE

TABLE 3 — FOR USE WITH STYLES CM, CN, CY AND CB

COLOR	MIL ID	1ST SIG FIG	2D SIG FIG	MULTIPLIER[1]	CAPACITANCE TOLERANCE				CHARACTERISTIC[2]			DC WORKING VOLTAGE	OPERATING TEMP RANGE	VIBRATION GRADE
					CM	CN	CY	CB	CM	CN	CB	CM	CY, CM	CM
BLACK	CM, CY CB	0	0	1			±20%	±20%		A			-55° TO +70°C	10-55 HZ
BROWN		1	1	10					B	E	B			
RED		2	2	100	±2%		±2%	±2%	C				-55° TO +85°C	
ORANGE		3	3	1,000		±30%			D		D	300		
YELLOW		4	4	10,000					E				-55° TO +125°C	10-2,000 HZ
GREEN		5	5		±5%				F			500		
BLUE		6	6										-55° TO +150°C	
PURPLE (VIOLET)		7	7											
GRAY		8	8											
WHITE		9	9											
GOLD				0.1			±5%	±5%						
SILVER	CN			0.01	±10%	±10%	±10%	±10%						

TABLE 4 — TEMPERATURE COMPENSATING, STYLE CC

COLOR	TEMPERATURE COEFFICIENT[4]	1ST SIG FIG	2D SIG FIG	MULTIPLIER[1]	CAPACITANCE TOLERANCE		MIL ID
					CAPACITANCES OVER 10 UUF	CAPACITANCES 10 UUF OR LESS	
BLACK	0	0	0	1		±2.0 UUF	CC
BROWN	-30	1	1	10	±1%		
RED	-80	2	2	100	±2%	±0.25 UUF	
ORANGE	-150	3	3	1,000			
YELLOW	-220	4	4				
GREEN	-330	5	5		±5%	±0.5 UUF	
BLUE	-470	6	6				
PURPLE (VIOLET)	-750	7	7				
GRAY		8	8	0.01*			
WHITE		9	9	0.1*	±10%		
GOLD	+100			0.1		±1.0 UUF	
SILVER				0.01			

1 THE MULTIPLIER IS THE NUMBER BY WHICH THE TWO SIGNIFICANT (SIG) FIGURES ARE MULTIPLIED TO OBTAIN THE CAPACITANCE IN UUF

2 LETTERS INDICATE THE CHARACTERISTICS DESIGNATED IN APPLICABLE SPECIFICATIONS MIL-C-5, MIL-C-25D, MIL-C-11272B, AND MIL-C-10950C RESPECTIVELY

3 LETTERS INDICATE THE TEMPERATURE RANGE AND VOLTAGE-TEMPERATURE LIMITS DESIGNATED IN MIL-C-11015D

4 TEMPERATURE COEFFICIENT IN PARTS PER MILLION PER DEGREE CENTIGRADE

* OPTIONAL CODING WHERE METALLIC PIGMENTS ARE UNDESIRABLE.

C. COLOR CODE MARKING FOR MILITARY STANDARD CAPACITORS

ESC-FM 913-73

Figure 2-1. Color code markings for MIL STD resistors, inductors, and capacitors.

NOTES:

1. WIRING SHOWN AS SEEN FROM WIRING SIDE.
2. FER INDICATES FERRULE.
3. WIRE DESTINATIONS LIST STATION NUMBER FOLLOWED BY TERMINAL NUMBER IN PARENTHESIS.

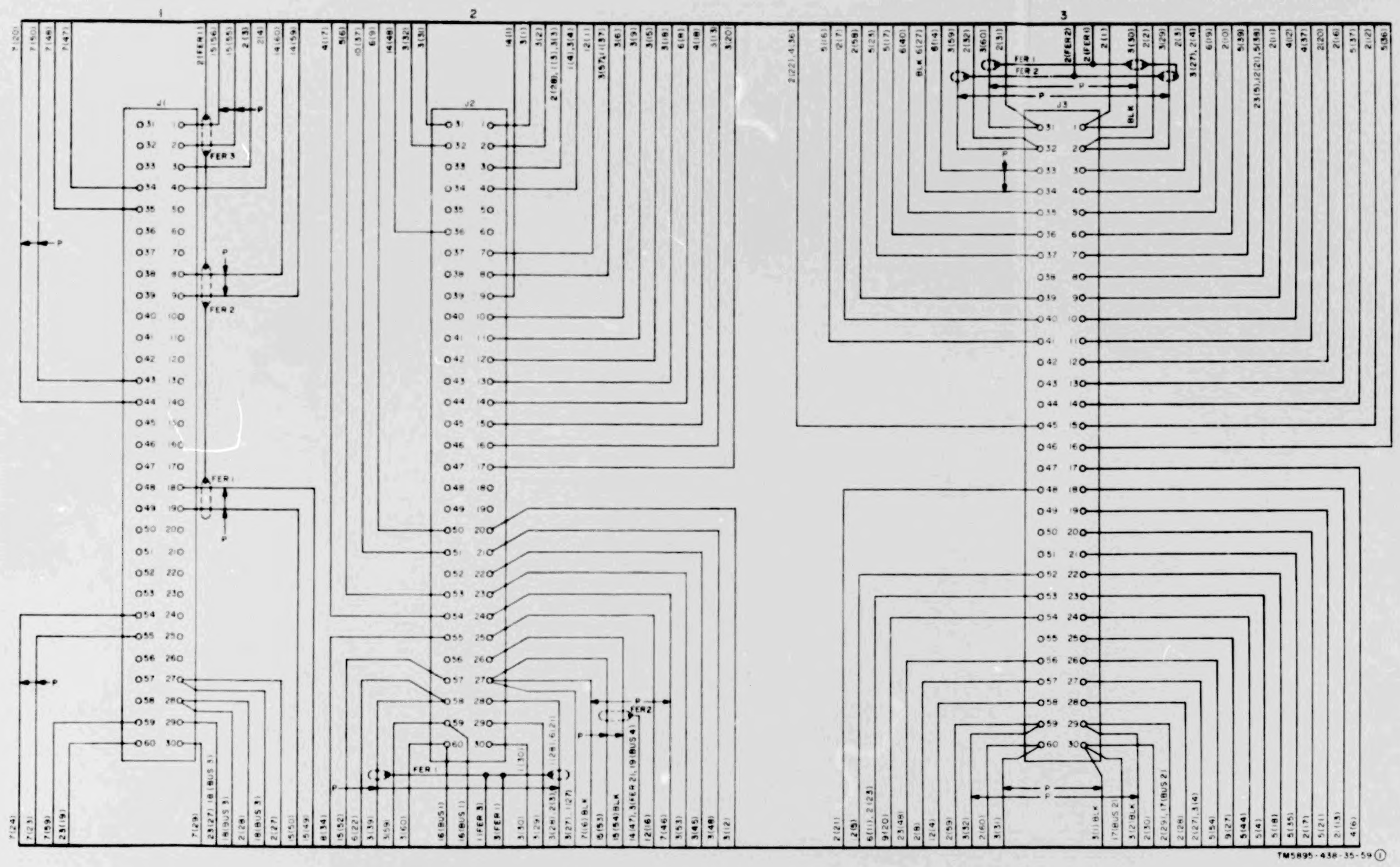

1
2
3
J1
J2
J3
FER 1
FER 2
FER 3
P
BLK
TM5895-438-35-59①

Figure 2-3①. Logic Rack Assembly A2, wiring diagram (part 1 of 8).

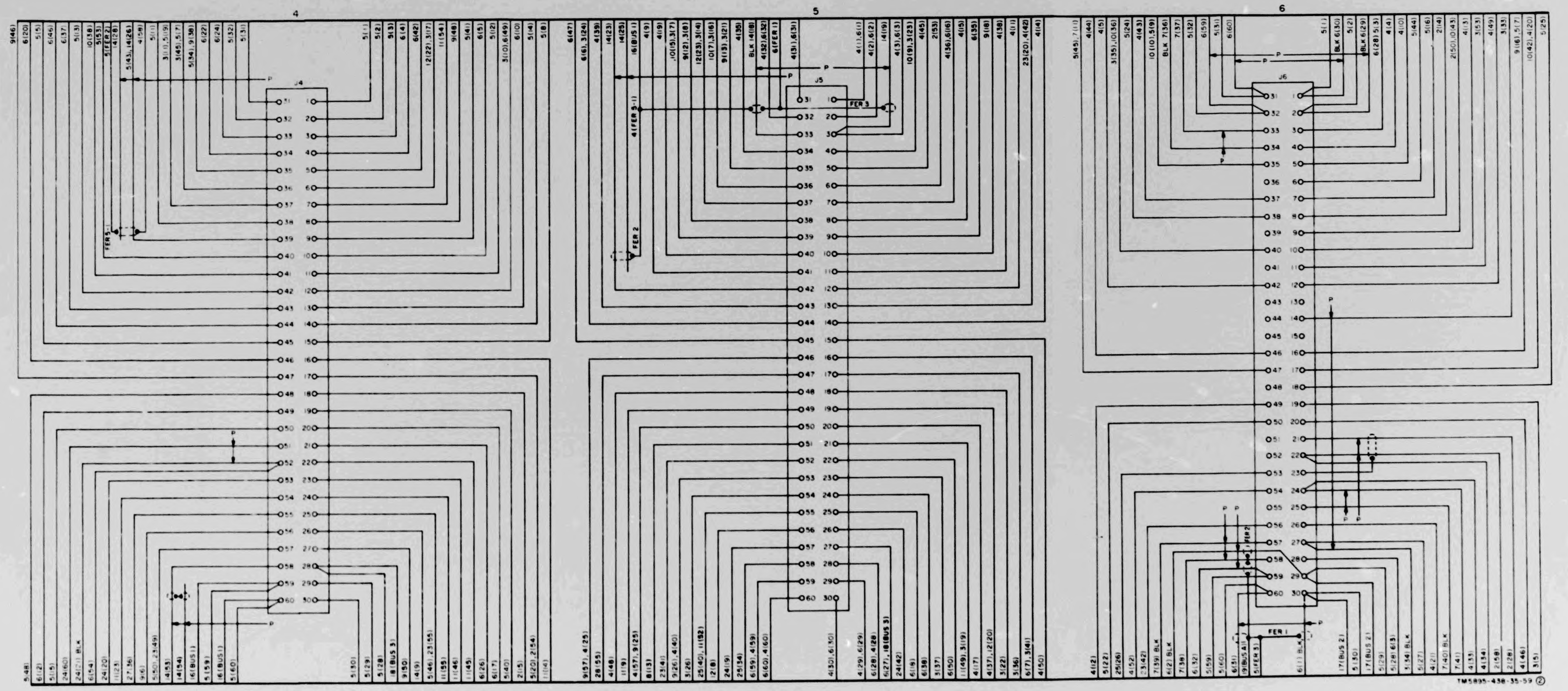

4
5
6
J4
J5
J6
P
FER 1
FER 2
FER 3
BLK
TM5835-438-35-59 ②

Figure 2-3②. Logic Rack Assembly A2, wiring diagram (part 2 of 8).

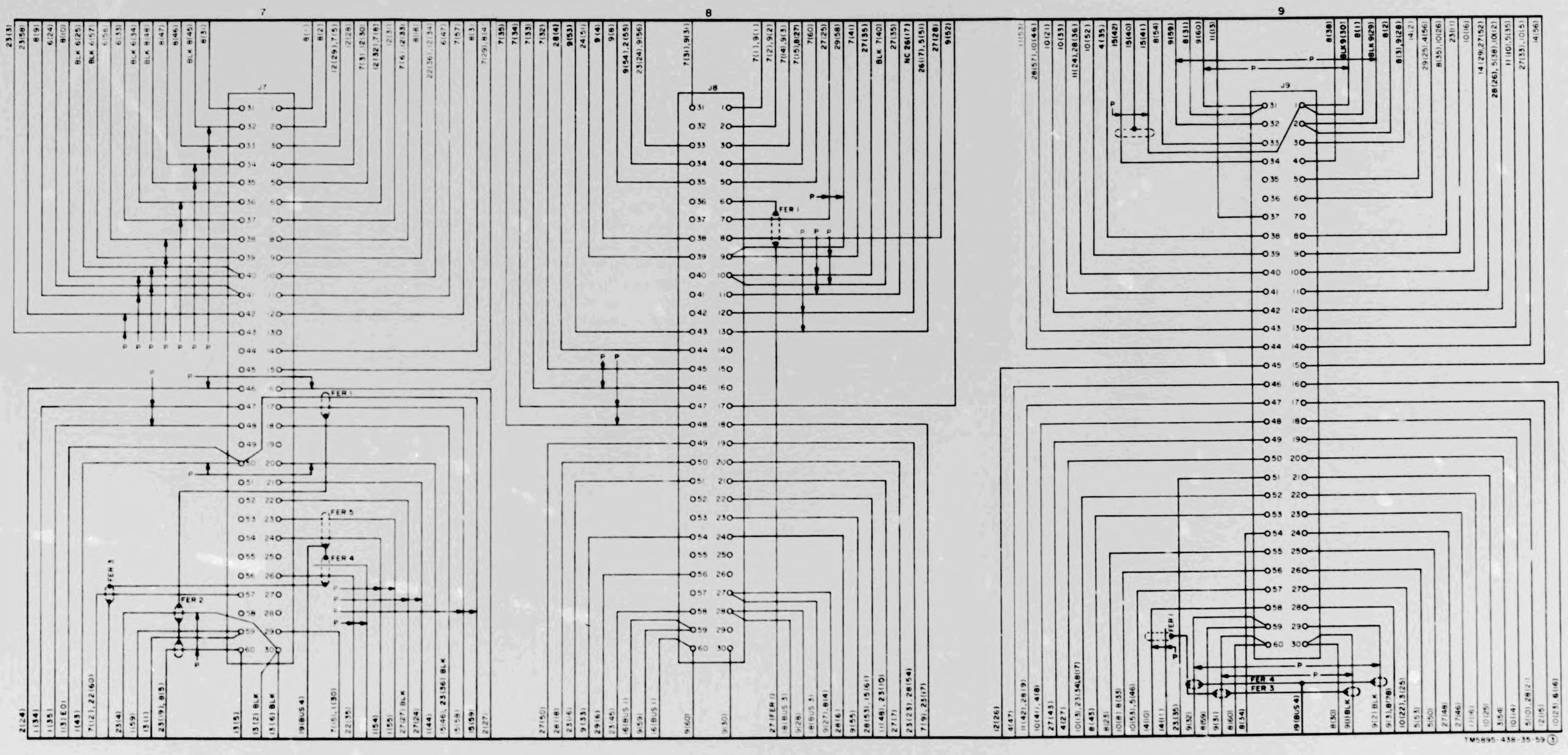

7
8
9
J7
J8
J9
FER 1
FER 2
FER 3
FER 4
FER 5
P
BLK
TM5895-438-35-59 ③

Figure 2-3③. Logic Rack Assembly A2, wiring diagram (part 3 of 8).

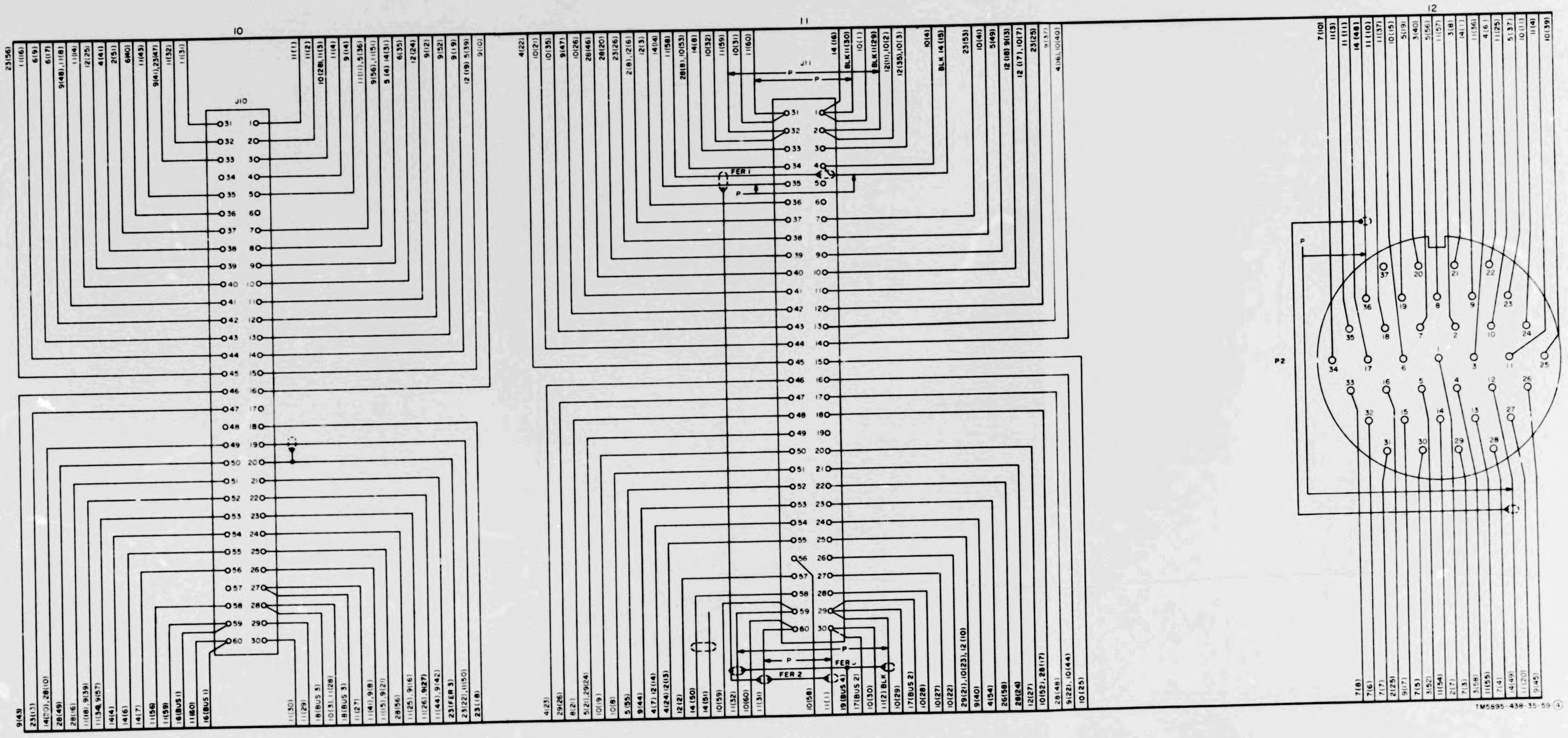

10
11
12
J10
J11
P2
FER 1
FER 2
P
TM5895-438-35-59④

Figure 2-3④. Logic Rack Assembly A2, wiring diagram (part 4 of 8).

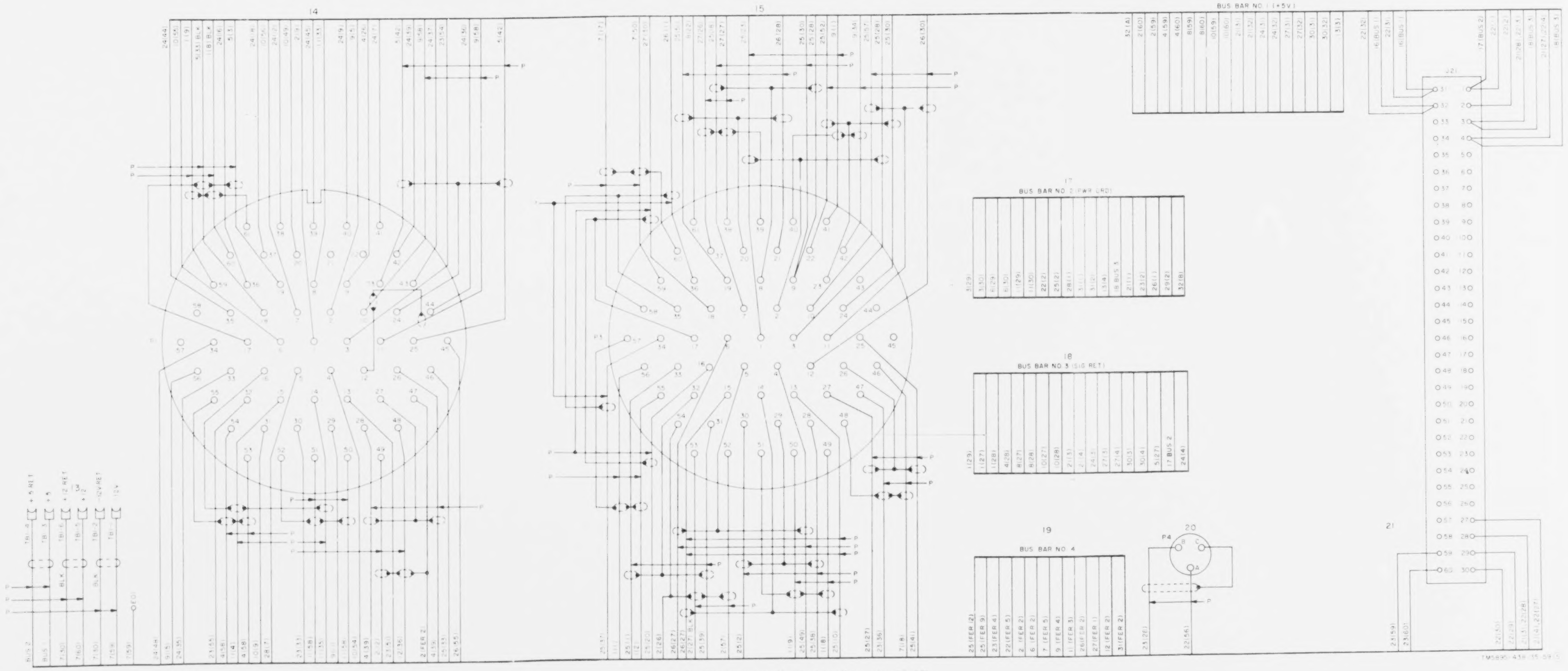

14
15
16
BUS BAR NO. 1 (+5V)
17
BUS BAR NO 2 (PWR GRD)
18
BUS BAR NO 3 (SIG RET)
19
BUS BAR NO. 4
20
P4
21
P

Figure 2-3⑤. Logic Rack Assembly A2, wiring diagram (part 5 of 8).

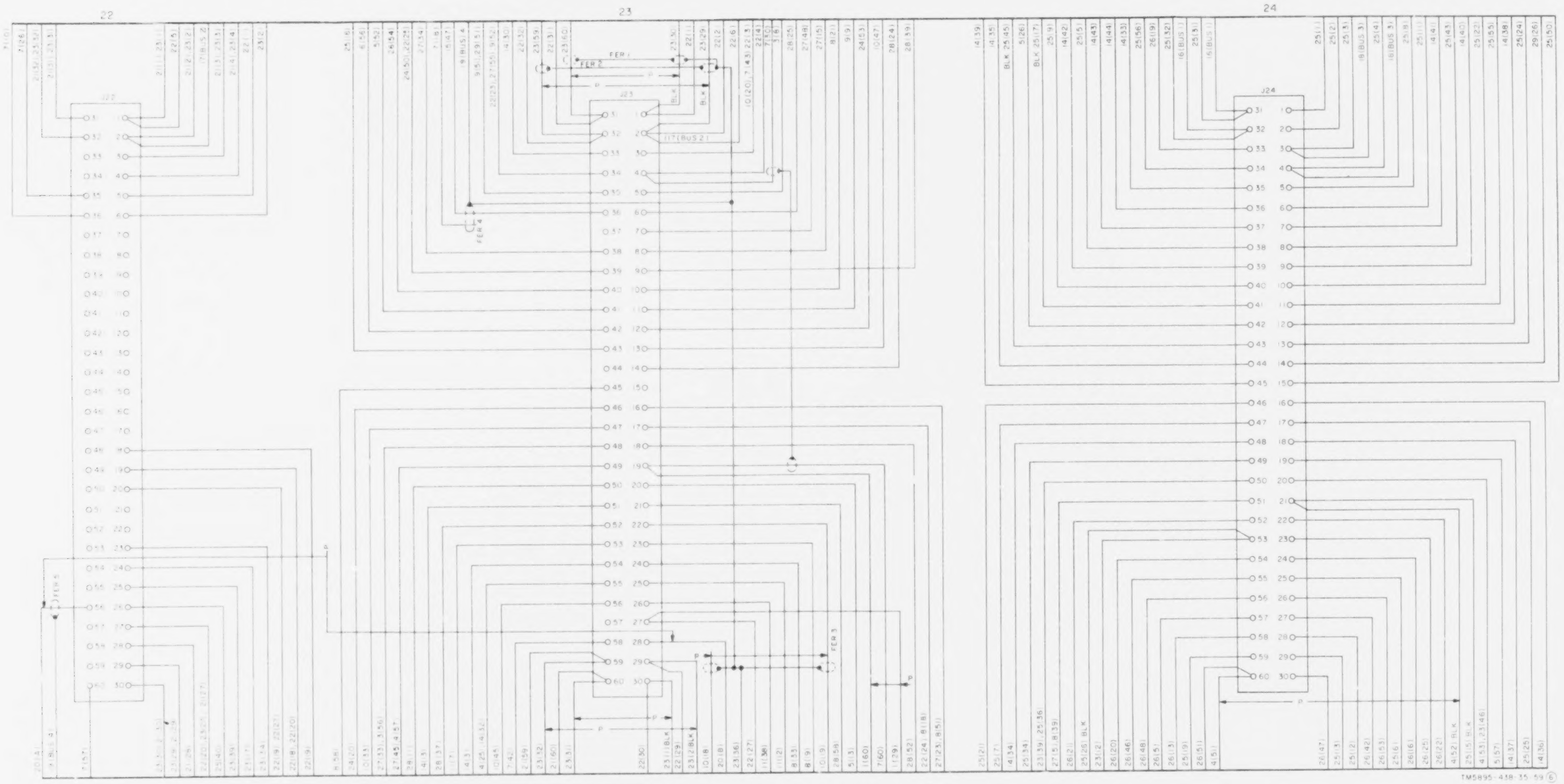

22
23
24
J22
J23
J24
FER 1
FER 2
FER 3
FER 4
FER 5
17 (BUS 2)
P
TM5895-438-35-59⑥

Figure 2-3⑥. Logic Rack Assembly A2, wiring diagram (part 6 of 8).

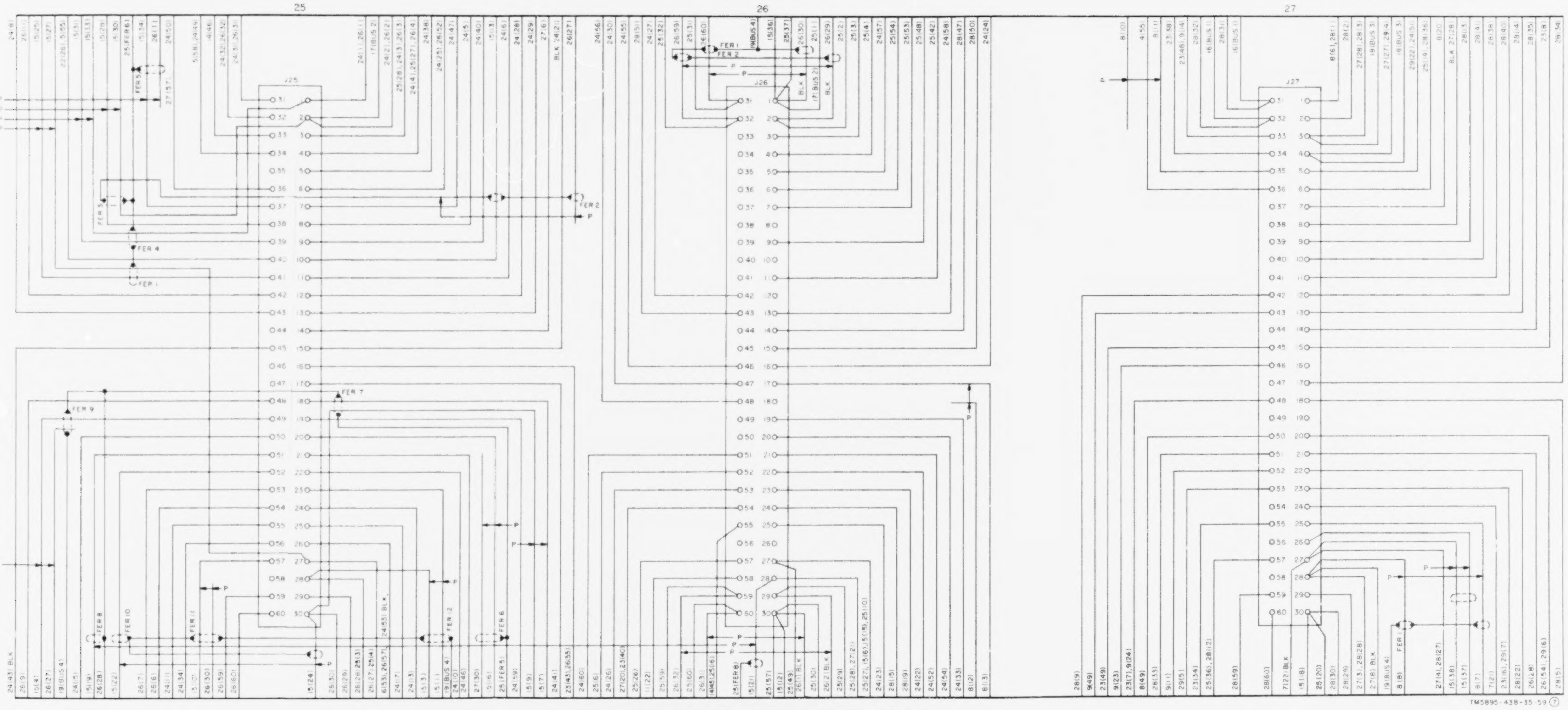

25
26
27
J25
J26
J27
FER 1
FER 2
FER 3
FER 4
FER 5
FER 6
FER 7
FER 8
FER 9
FER 10
FER 11
FER 12
P
BLK

Figure 2-3⑦. Logic Rack Assembly A2, wiring diagram (part 7 of 8).

TM5895-438-35-59 ⑦

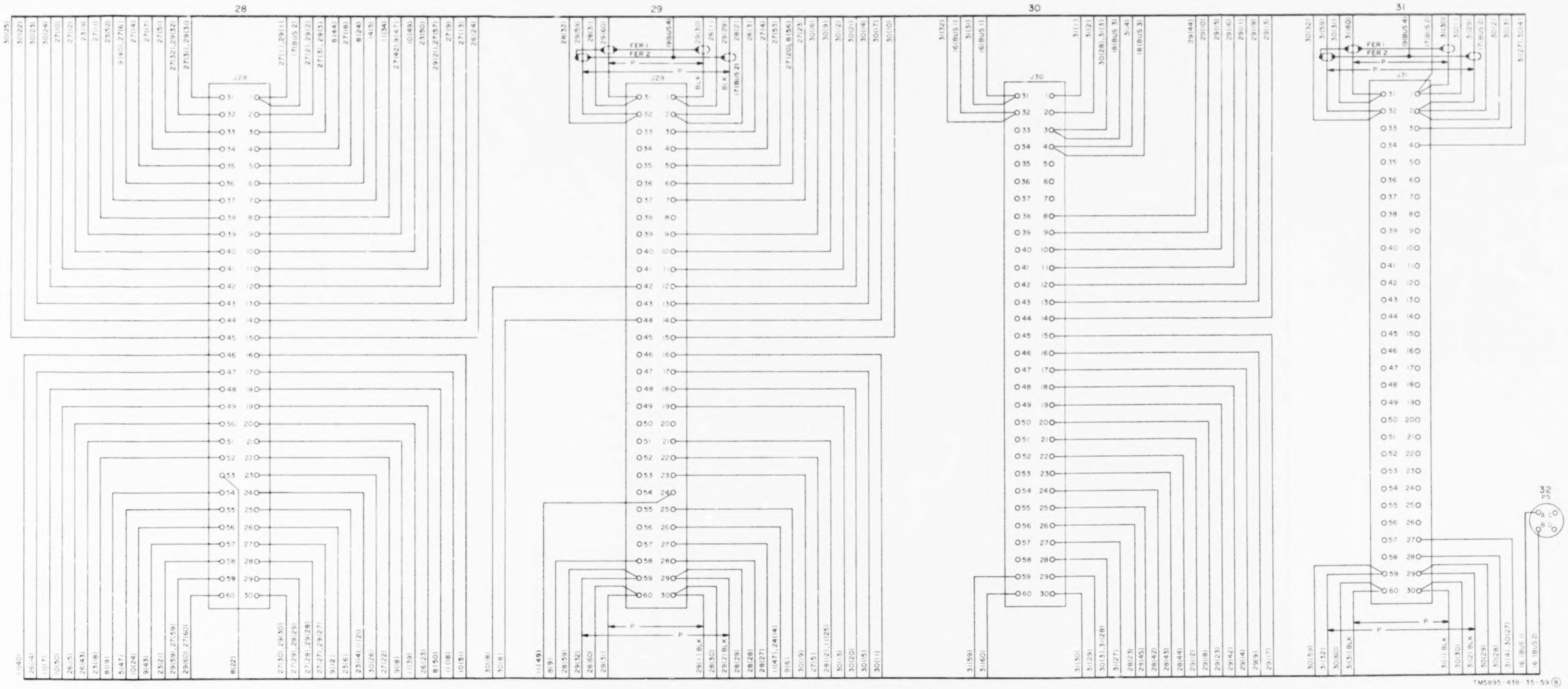
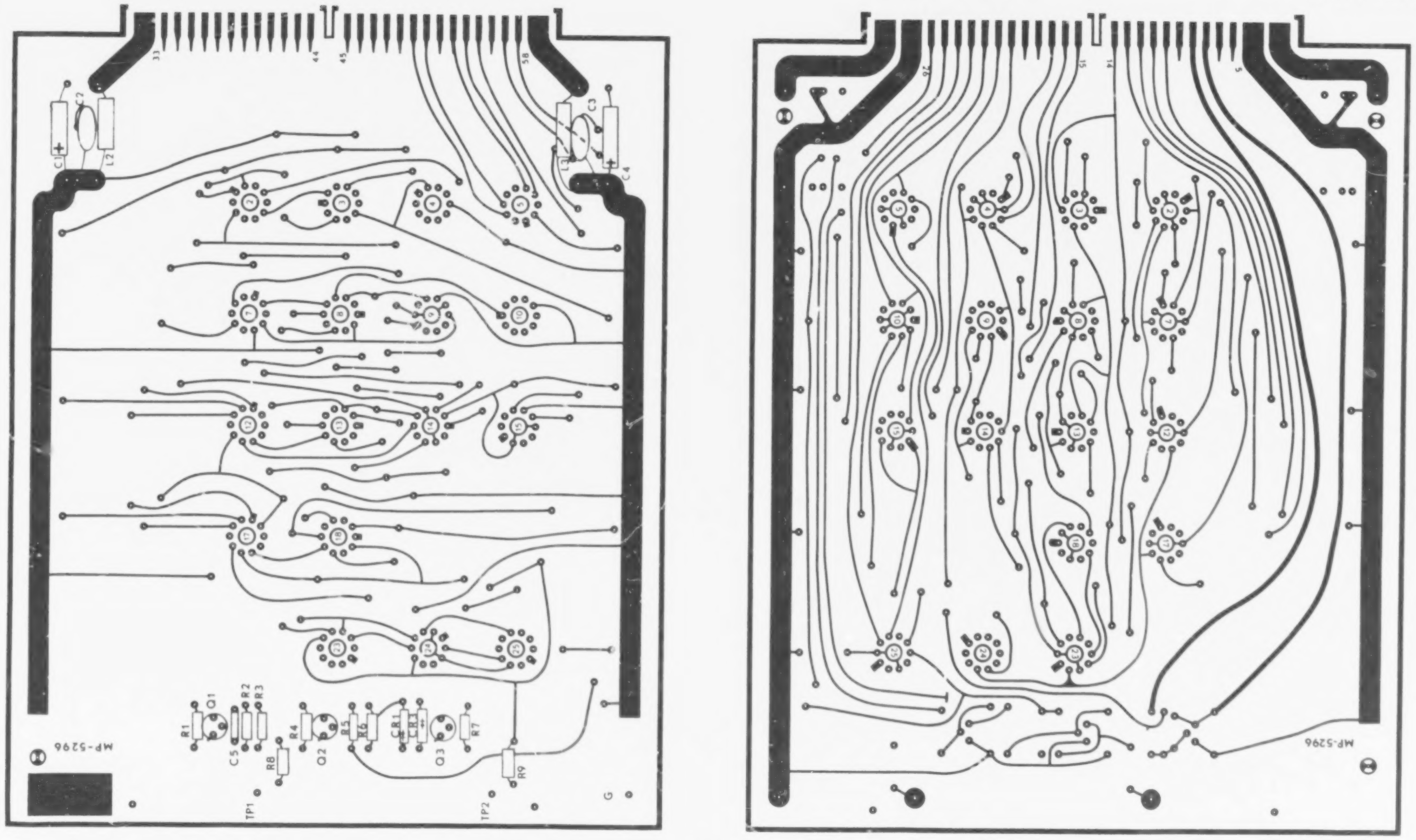

28
29
30
31
32
J28
J29
J30
J31
FER 1
FER 2
P
BLK
TM5895-438-35-59 (8)

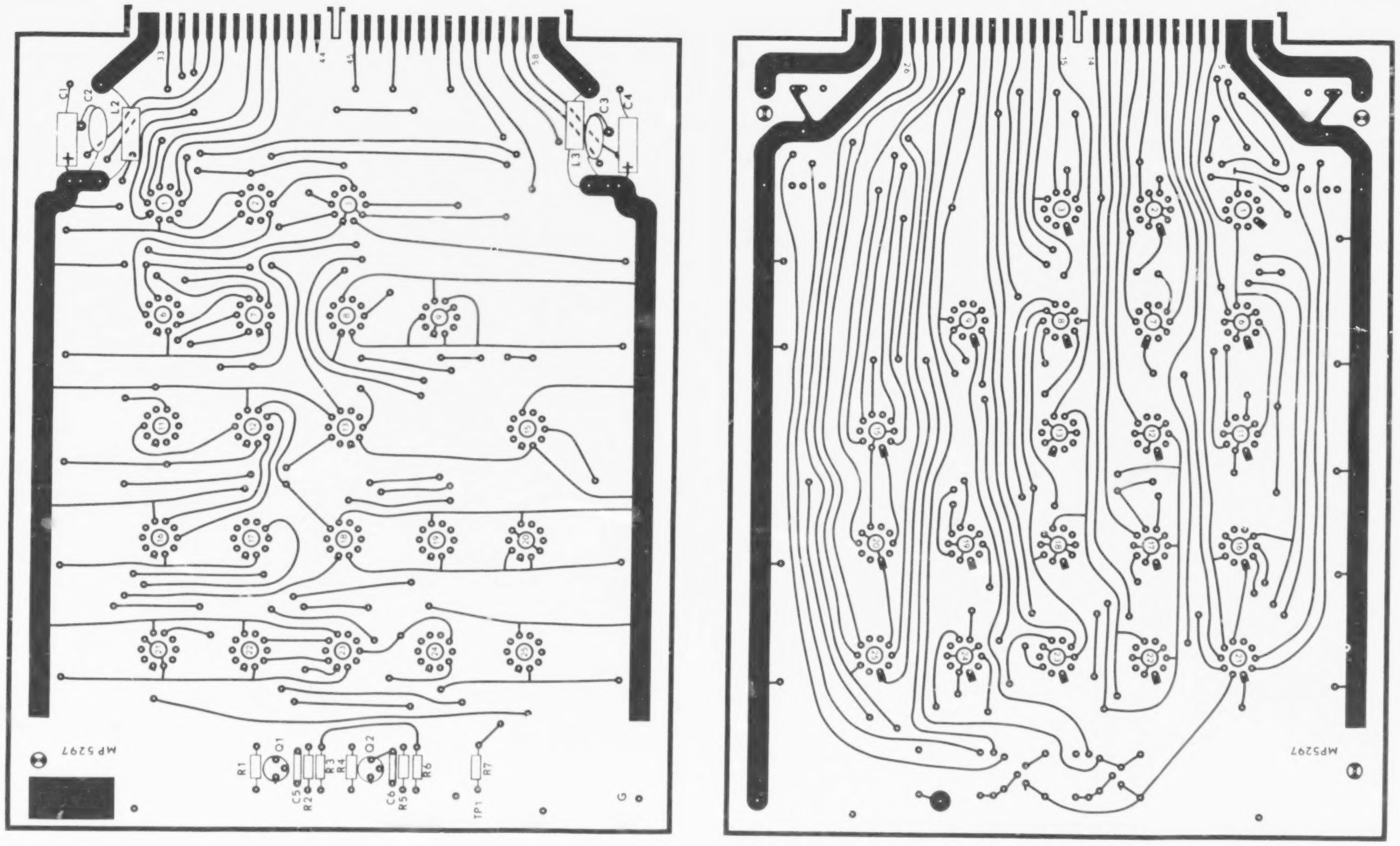
Figure 2-3⑧. Logic Rack Assembly A2, wiring diagram (part 8 of 8).


33
44
45
58
C1
C2
L2
L1
C3
C4
MP-5296
R1
Q1
R2
R3
C5
R8
R4
Q2
CR1
Q3
R7
R9
TP1
TP2
G
26
15
14
5
MP-5296

POSITION NO	INTEGRATED CIRCUIT MODULE
1	NOT EQUIPPED
2	C7976K
3	C7974K
4	C7972K
5	C7976K
6	NOT EQUIPPED
7	C7976K
8	C7974K
9	C7972K
10	C7976K
11	NOT EQUIPPED
12	C7972K
13	C7974K
14	C7972K
15	C7972K
16	NOT EQUIPPED
17	C7972K
18	C7974K
19	NOT EQUIPPED
20	NOT EQUIPPED
21	NOT EQUIPPED
22	NOT EQUIPPED
23	C7974K
24	C7974K
25	C7974K

TM5895-438-35-60

Figure 2-4. Logic Card 1A2A2 wiring and parts location diagram.


33
44
45
58
C1
C2
L2
C3
L3
C4
MP5297
R1
Q1
C5
R2
R3
R4
Q2
C6
R5
R6
R7
TP1
G
26
14
5
MP5297

POSITION NO	INTEGRATED CIRCUIT MODULE
1	C7972K
2	C7976K
3	C7968K
4	NOT EQUIPPED
5	NOT EQUIPPED
6	C7974K
7	C7970K
8	C7970K
9	C7972K
10	NOT EQUIPPED
11	C7974K
12	C7974K
13	C7974K
14	NOT EQUIPPED
15	C7975K
16	C7970K
17	C7974K
18	C7976K
19	C7974K
20	C7972K
21	C7968K
22	C7974K
23	C7970K
24	C7974K
25	C7970K

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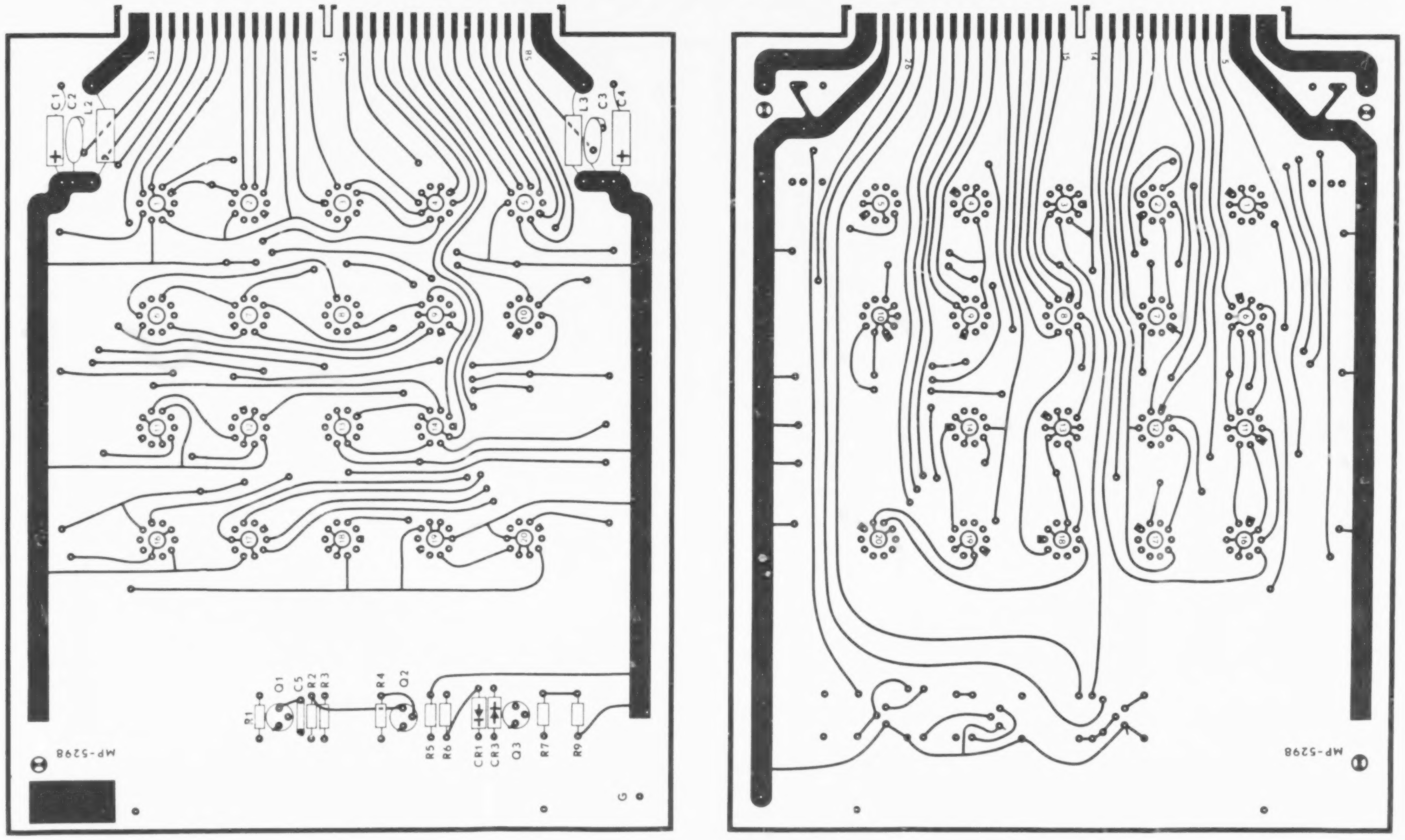
Figure 2-5. Logic Card 1A2A3 wiring and parts location diagram.


C1
C2
L2
L3
C3
C4
R1
Q1
C5
R2
R3
R4
Q2
R5
R6
CR1
CR3
Q3
R7
R9
MP-5298
G
MP-5298

POSITION NO	INTEGRATED CIRCUIT MODULE
1	C7972K
2	C7970K
3	C7972K
4	C7976K
5	C7972K
6	C7976K
7	C7970K
8	C7970K
9	C7972K
10	C7972K
11	C7972K
12	C7976K
13	C7972K
14	C7972K
15	NOT EQUIPPED
16	C7972K
17	C7974K
18	C7974K
19	C7974K
20	C7974K
21	NOT EQUIPPED
22	NOT EQUIPPED
23	NOT EQUIPPED
24	NOT EQUIPPED
25	NOT EQUIPPED

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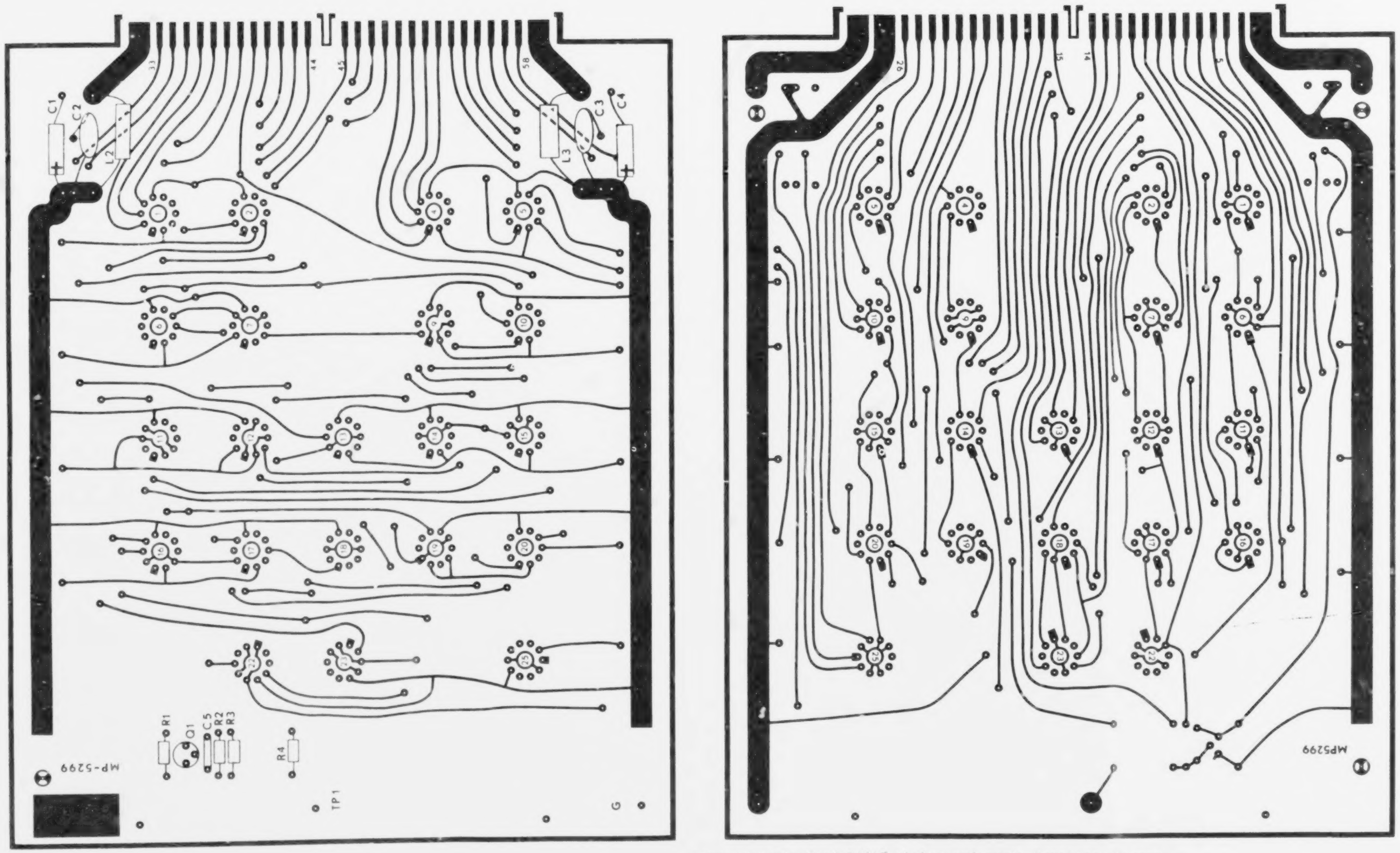
Figure 2-6. Logic Card 1A2A4 wiring and parts location diagram.


33
44
45
58
C1
C2
L2
L3
C3
C4
R1
Q1
C5
R2
R3
R4
TP1
G
MP-5299
26
15
14
5
MP5299

POSITION NO.	INTEGRATED CIRCUIT MODULE
1	C7976K
2	C7970K
3	NOT EQUIPPED
4	C7970K
5	C7972K
6	C7976K
7	C7976K
8	NOT EQUIPPED
9	C7972K
10	C7976K
11	C7972K
12	C7972K
13	C7972K
14	C7970K
15	C7976K
16	C7972K
17	C7972K
18	C7970K
19	C7972K
20	C7970K
21	NOT EQUIPPED
22	C7972K
23	C7972K
24	NOT EQUIPPED
25	C7976K

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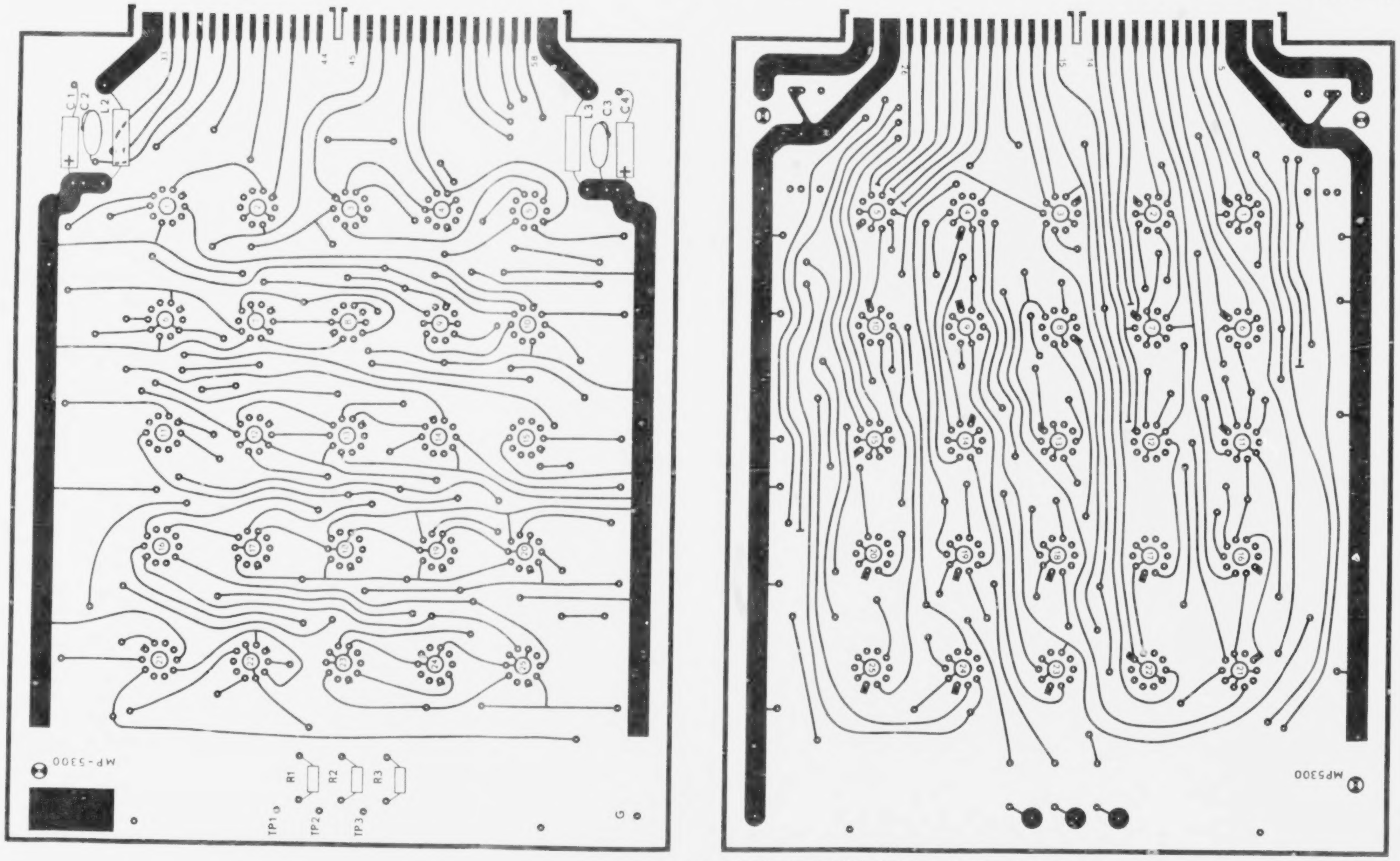
Figure 2-7. Logic Card 1A2A5 wiring and parts location diagram.


33
44
45
58
C1
C2
L2
L3
C3
C4
+
R1
R2
R3
TP1
TP2
TP3
G
MP-5300
26
15
14
5
MP5300

POSITION NO	INTEGRATED CIRCUIT MODULE
1	C7972K
2	C7972K
3	C7972K
4	C7976K
5	C7972K
6	C7972K
7	C7976K
8	C7972K
9	C7976K
10	C7976K
11	C7976K
12	C7976K
13	C7972K
14	C7974K
15	C7976K
16	C7976K
17	C7974K
18	C7974K
19	C7974K
20	C7974K
21	C7972K
22	C7972K
23	C7974K
24	C7974K
25	C7974K

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Figure 2-8. Logic Card 1A2A6 wiring and parts location diagram.

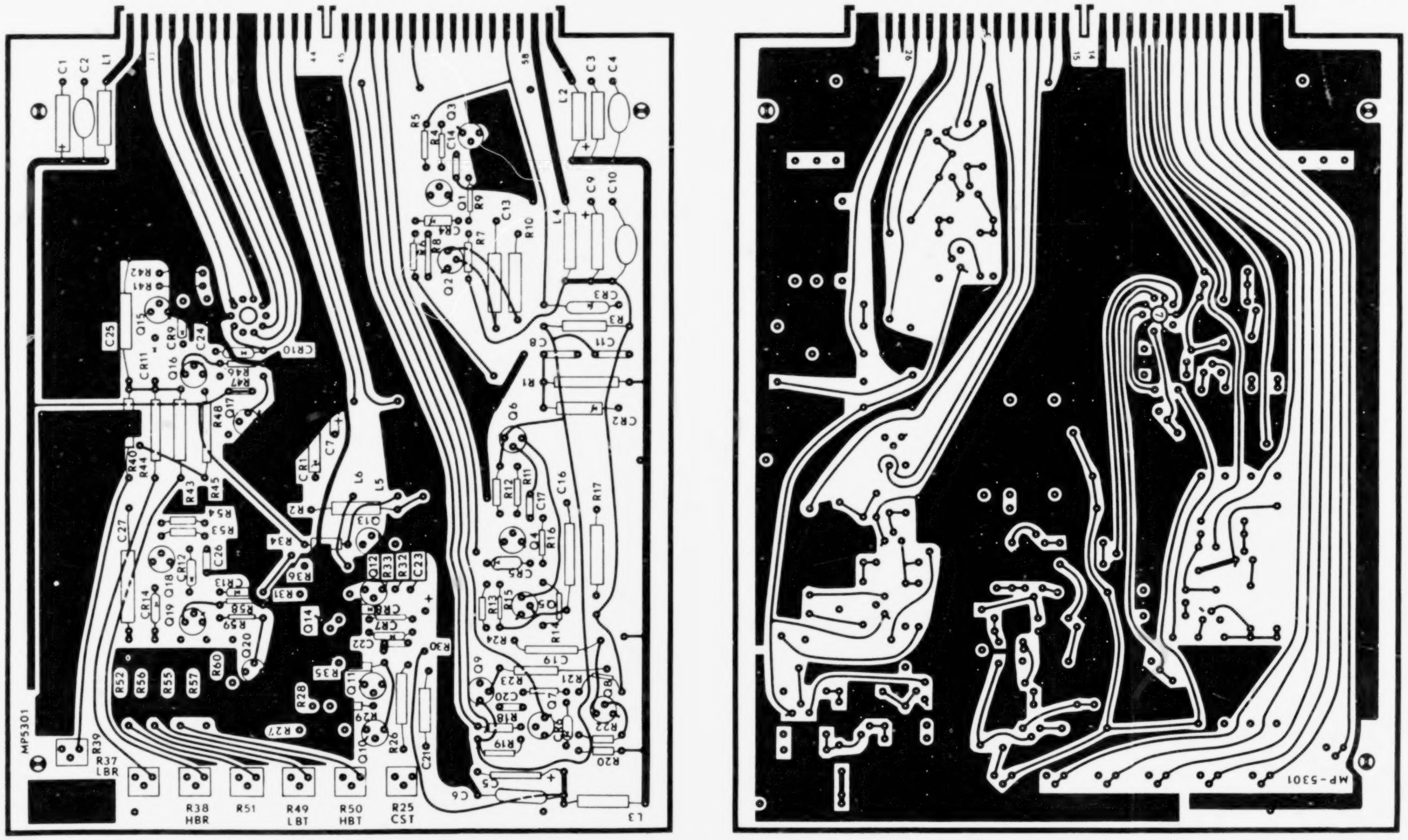
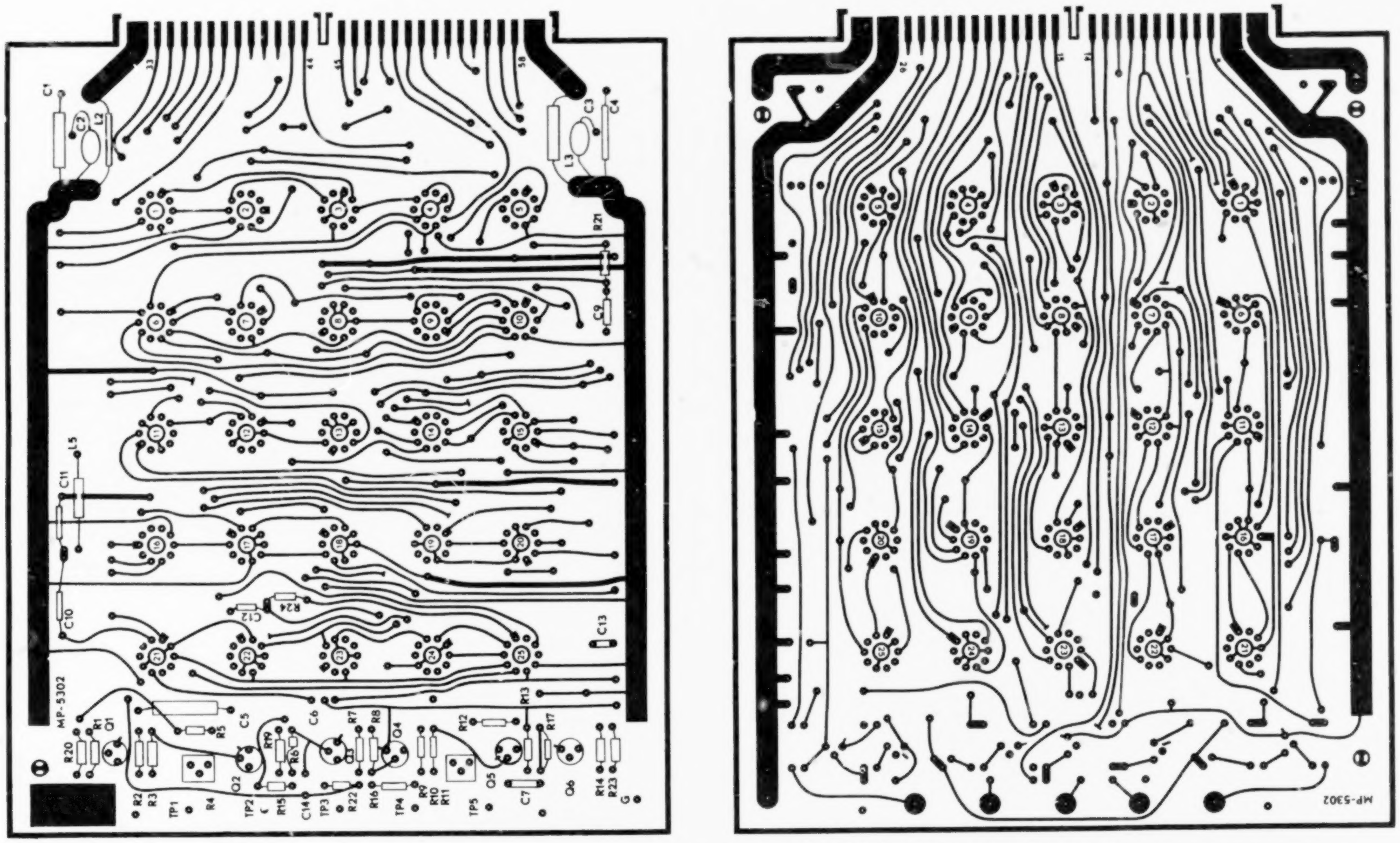

C1
C2
L1
C3
C4
L2
R5
R4
Q3
C14
Q1
R9
C13
R10
L4
C9
C10
R7
R8
R6
CR4
Q2
CR3
R3
C8
C11
R1
CR2
R42
R41
Q15
CR9
C24
C25
CR11
Q16
R46
R47
CR10
R48
Q17
C7
CR1
L6
L5
R2
Q6
R11
R12
C17
C16
R17
R40
R44
R43
R45
R54
R53
C26
C27
R34
Q13
Q4
R16
CR5
R36
Q12
R33
R32
C23
CR14
Q18
R12
CR13
R31
CR6
CR7
R13
R15
Q5
R14
Q19
R58
R59
Q14
C22
R24
R60
Q20
R30
C19
R52
R56
R55
R57
R35
Q11
Q9
R23
C20
R21
Q8
R28
R18
Q7
R22
R27
R29
Q10
R26
R19
C21
R20
C6
C5
L3
MP5301
R39
R37
LBR
R38
HBR
R51
R49
LBT
R50
HBT
R25
CST
MP-5301

Figure 2-9. Logic Card 1A2A7 wiring and parts location diagram.

POSITION NO	
1	N
2	N
3	N
4	N
5	N
6	N
7	
8	N
9	N
10	N
11	N
12	N
13	N
14	N
15	N
16	N
17	N
18	N
19	N
20	N
21	N
22	N
23	N
24	N
25	N

NOTE: R39, R40,
ARE FOR
OTHER THA
SYSTEM BA
ARE NOT


33
44
45
58
C1
C2
L2
C3
C4
L3
R21
C9
L5
C11
C10
C12
R24
C13
MP-5302
R20
R1
Q1
R2
R3
TP1
R4
R5
C5
Q2
TP2
R15
R19
R6
C14
TP3
C6
R7
R8
R22
Q3
Q4
R16
TP4
R9
R10
R11
R12
TP5
Q5
R13
C7
R17
Q6
R14
R23
G
26
15
14
MP-5302

POSITION NO	INTEG CIR MO
1	C79
2	C79
3	C79
4	C79
5	NOT E
6	C79
7	C79
8	C79
9	C79
10	C79
11	C79
12	C79
13	C79
14	C79
15	C79
16	C79
17	C79
18	C79
19	C79
20	C79
21	C79
22	C79
23	C79
24	C79
25	C79

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Figure 2-10. Logic Card 1A2A8 wiring and parts location diagram.

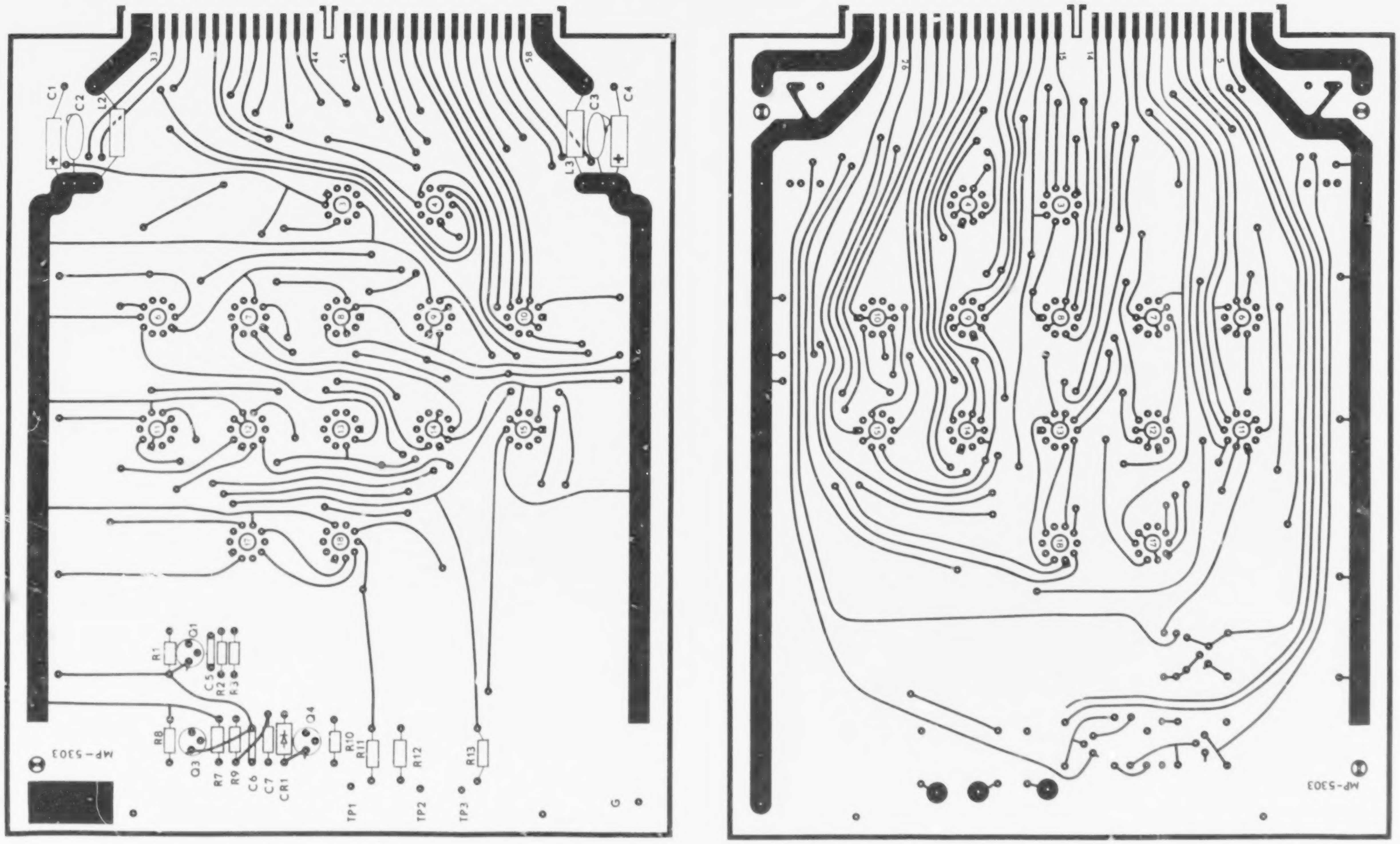
C1
C2
L2
33
44
45
58
C3
C4
L3
R1
Q1
C5
R2
R3
R8
Q3
R7
R9
C6
C7
CR1
Q4
R10
R11
R12
R13
TP1
TP2
TP3
G
MP-5303
26
15
14
5
MP-5303

Figure 2-11. Logic Card 1A2A9 wiring and parts location diagram.

POSITION NO	INTEG CIRC MOD
1	NOT EQ
2	NOT EQ
3	C797
4	C797
5	NOT EQ
6	C797
7	C797
8	C797
9	C797
10	C797
11	C79
12	C797
13	C797
14	C797
15	C797
16	NOT EQ
17	C797
18	C797
19	NOT EQ
20	NOT EQ
21	NOT EQ
22	NOT EQ
23	NOT EQ
24	NOT EQ
25	NOT EQ

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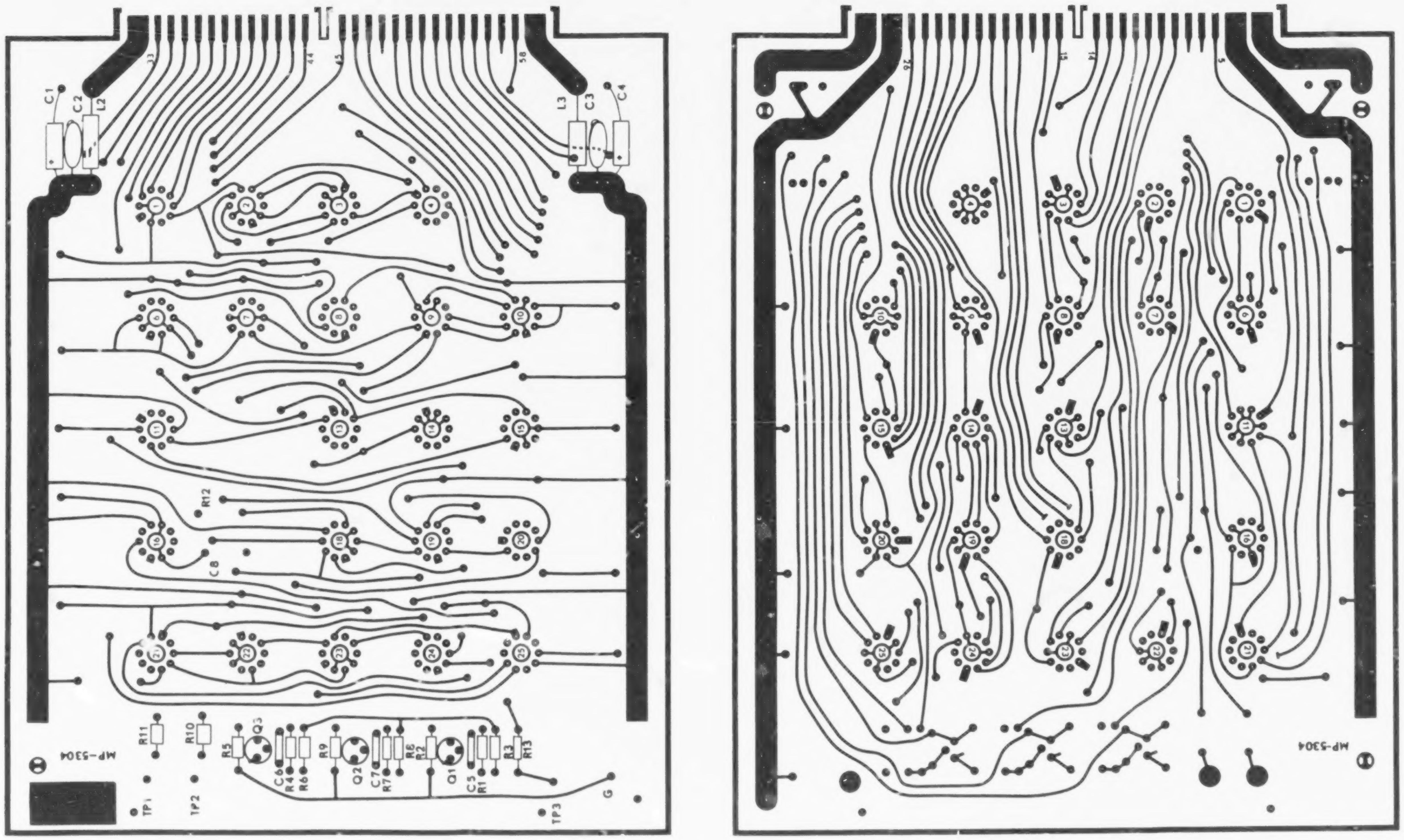
C1
C2
L2
33
44
45
58
L3
C3
C4
R12
C8
R11
R10
R5
Q3
C6
R4
R6
R9
Q2
C7
R7
R8
R2
Q1
C3
R1
R3
R13
TP1
TP2
TP3
G
MP-5304
26
13
14
5
MP-5304

Figure 2-12. Logic Card 1A2A10 wiring and parts location diagram.

POSITION NO	INT C
1	C
2	C
3	C
4	C
5	NOT
6	C
7	C
8	C
9	C
10	C
11	C
12	NOT
13	C
14	C
15	C
16	C
17	NOT
18	C
19	C
20	C
21	C
22	C
23	C
24	C
25	C

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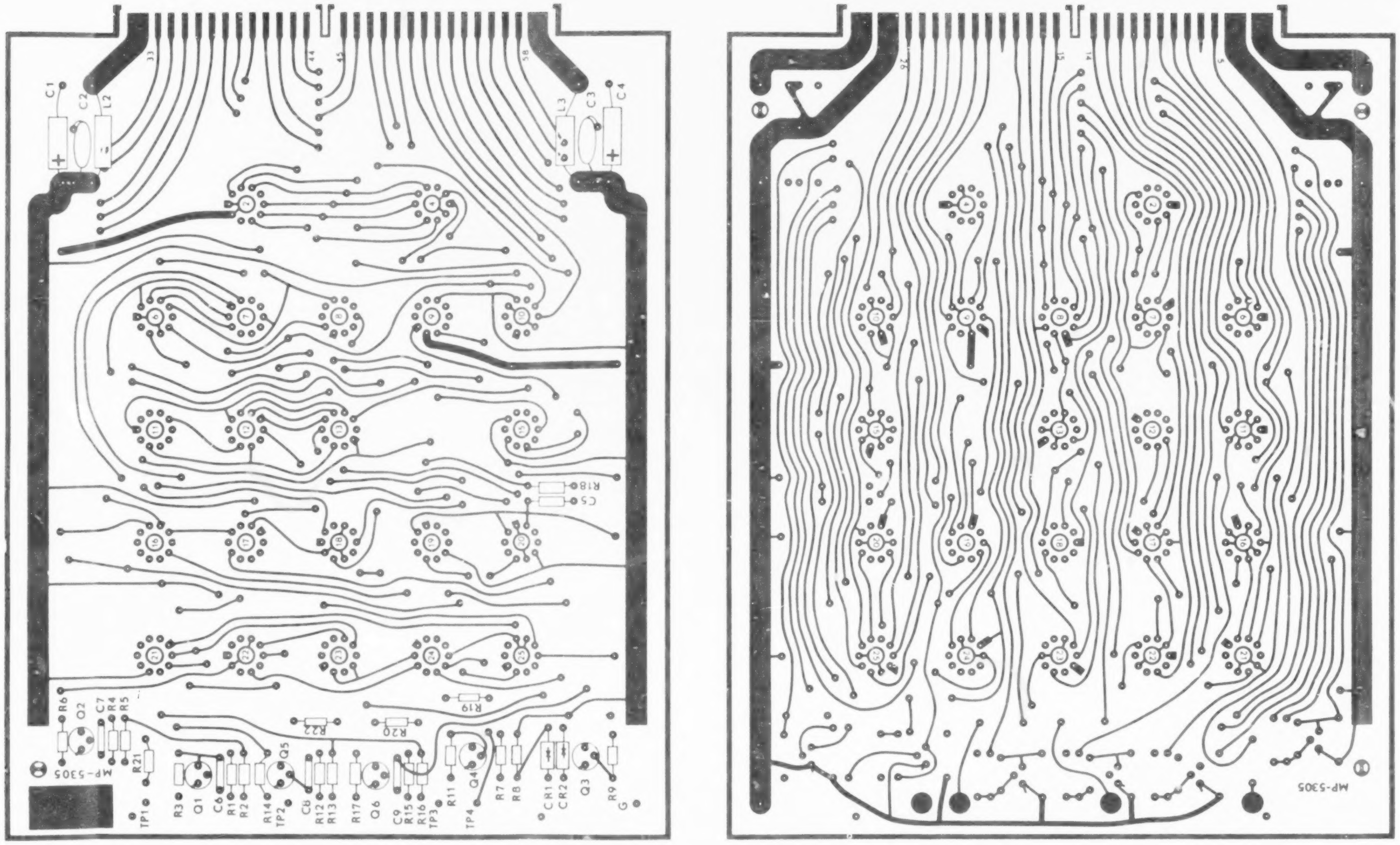
C1
C2
L2
33
44
45
58
L3
C3
C4
R18
C5
R19
R22
R20
R6
Q2
C7
R4
R5
R21
MP-5305
TP1
R3
Q1
C6
R1
R2
R14
TP2
Q5
C8
R12
R13
R17
Q6
C9
R15
R16
TP3
R11
TP4
Q4
R7
R8
CR1
CR2
Q3
R9
G
26
15
14
5
MP-5305

POSITION NO	INTEGRATED CIRCUIT MODULE
1	NOT EQUIPPED
2	C7971K
3	NOT EQUIPPED
4	C7968K
5	NOT EQUIPPED
6	C7976K
7	C7970K
8	C7971K
9	C7976K
10	C7972K
11	C7976K
12	C7970K
13	C7976K
14	NOT EQUIPPED
15	C7972K
16	C7972K
17	C7974K
18	C7976K
19	C7970K
20	C7972K
21	C7970K
22	C7974K
23	C7974K
24	C7975K
25	C7974K

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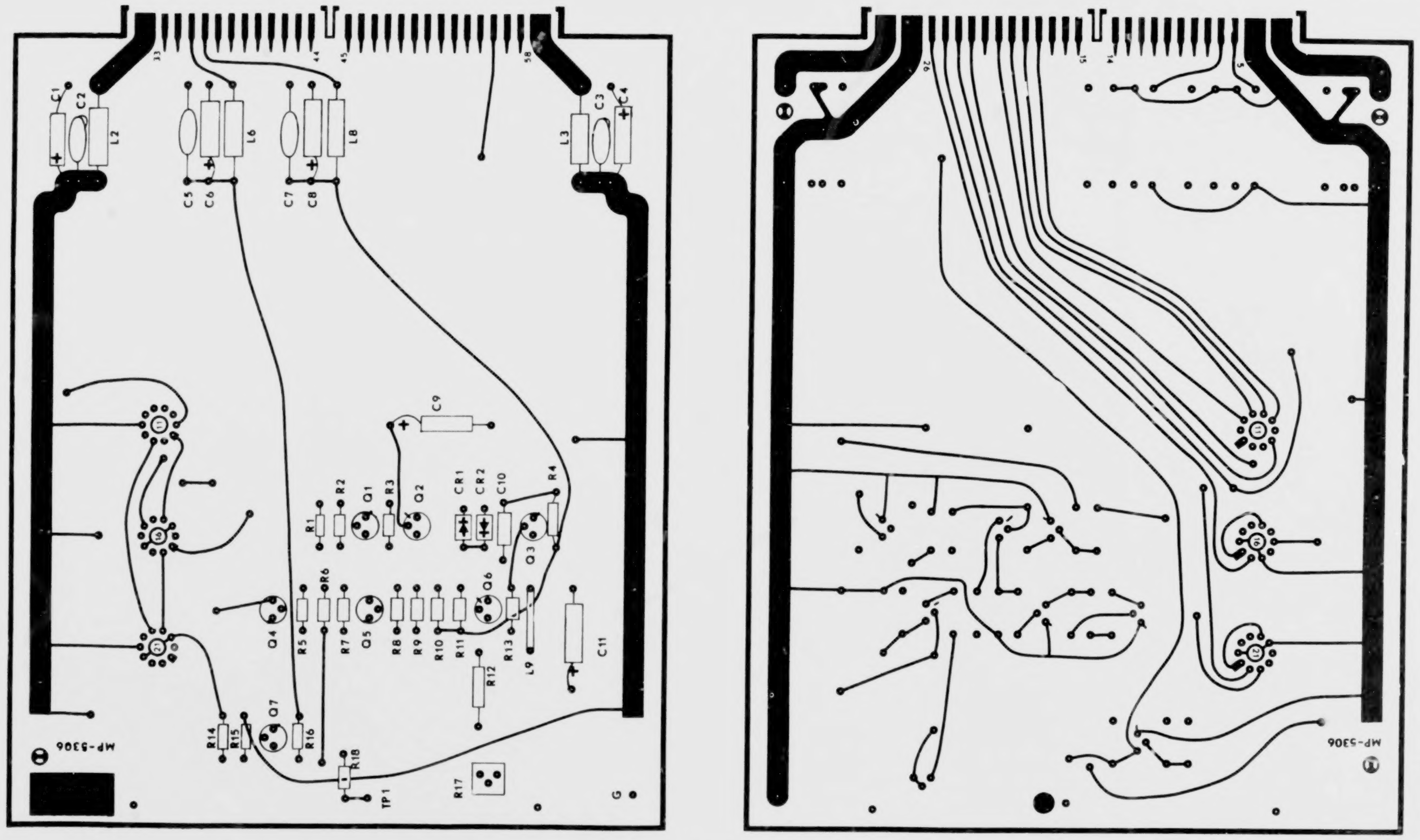
Figure 2-13. Logic Card 1A2A11 wiring and parts location diagram.


33
44
45
58
C1
C2
L2
C5
C6
L6
C7
C8
L8
L3
C3
C4
C9
R1
R2
Q1
R3
Q2
CR1
CR2
C10
R4
Q3
R5
R6
Q4
R7
Q5
R8
R9
R10
R11
Q6
R13
R12
L9
C11
R14
R15
Q7
R16
R18
TP1
R17
G
MP-5306
MP-5306

POSITION NO	INTEGRATED CIRCUIT MODULE
1	NOT EQUIPPED
2	NOT EQUIPPED
3	NOT EQUIPPED
4	NOT EQUIPPED
5	NOT EQUIPPED
6	NOT EQUIPPED
7	NOT EQUIPPED
8	NOT EQUIPPED
9	NOT EQUIPPED
10	NOT EQUIPPED
11	C7970K
12	NOT EQUIPPED
13	NOT EQUIPPED
14	NOT EQUIPPED
15	NOT EQUIPPED
16	C7972K
17	NOT EQUIPPED
18	NOT EQUIPPED
19	NOT EQUIPPED
20	NOT EQUIPPED
21	C7972K
22	NOT EQUIPPED
23	NOT EQUIPPED
24	NOT EQUIPPED
25	NOT EQUIPPED

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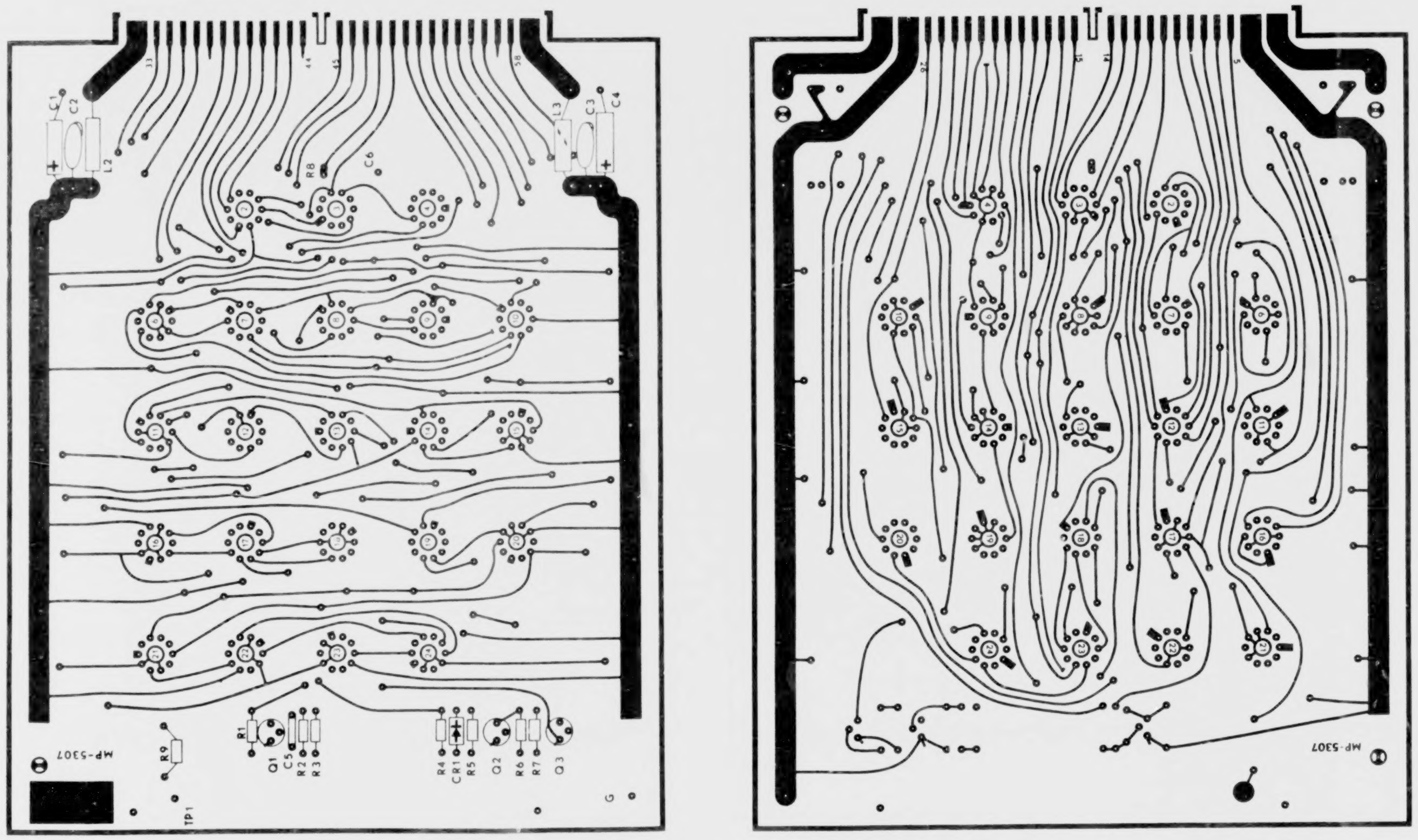
Figure 2-14. Logic Card 2A3 wiring and parts location diagram.


C1
C2
L2
L3
C3
C4
R8
C6
MP-5307
R9
TP1
R1
Q1
C5
R2
R3
R4
CR1
R5
Q2
R6
R7
Q3
G
MP-5307

POSITION NO	INTEGRATED CIRCUIT MODULE
1	NOT EQUIPPED
2	C7973K
3	C7968K
4	C7976K
5	NOT EQUIPPED
6	C7972K
7	C7969K
8	C7972K
9	C7974K
10	C7970K
11	C7976K
12	C7970K
13	C7974K
14	C7974K
15	C7974K
16	C7972K
17	C7974K
18	C7972K
19	C7970K
20	C7974K
21	C7974K
22	C7974K
23	C7974K
24	C7974K
25	NOT EQUIPPED

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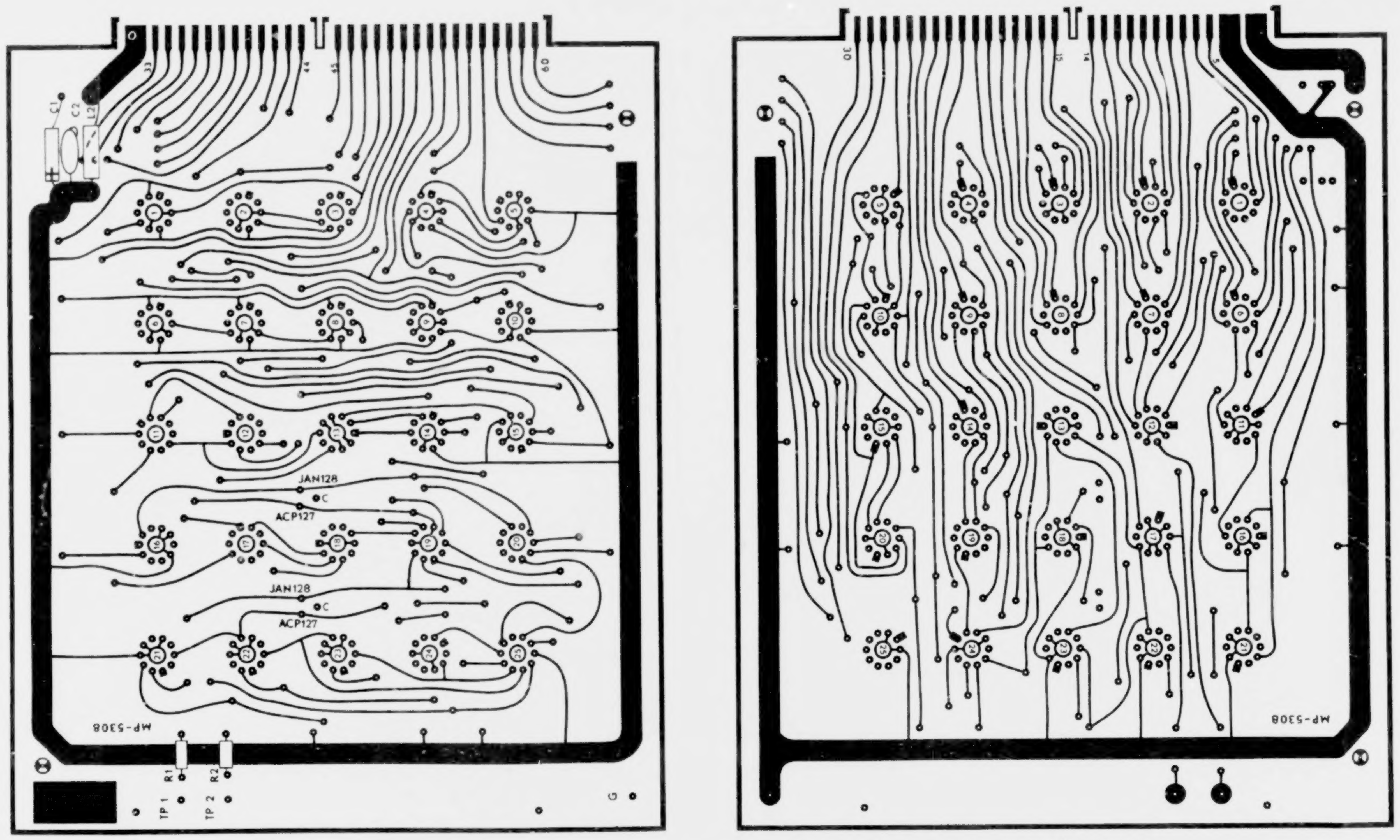
Figure 2-15. Logic Card 1A2A14 wiring and parts location diagram


C1
C2
L1
33
44
45
60
JAN128
C
ACP127
JAN128
C
ACP127
MP-5308
R1
R2
TP 1
TP 2
G
30
MP-5308

POSITION NO	INTEGRATED CIRCUIT MODULE
1	C7970K
2	C7970K
3	C7970K
4	C7972K
5	C7972K
6	C7970K
7	C7970K
8	C7970K
9	C7972K
10	C7972K
11	C7976K
12	C7974K
13	C7976K
14	C7972K
15	C7972K
16	C7974K
17	C7972K
18	C7976K
19	C7972K
20	C7972K
21	C7974K
22	C7974K
23	C7974K
24	C7976K
25	C7976K

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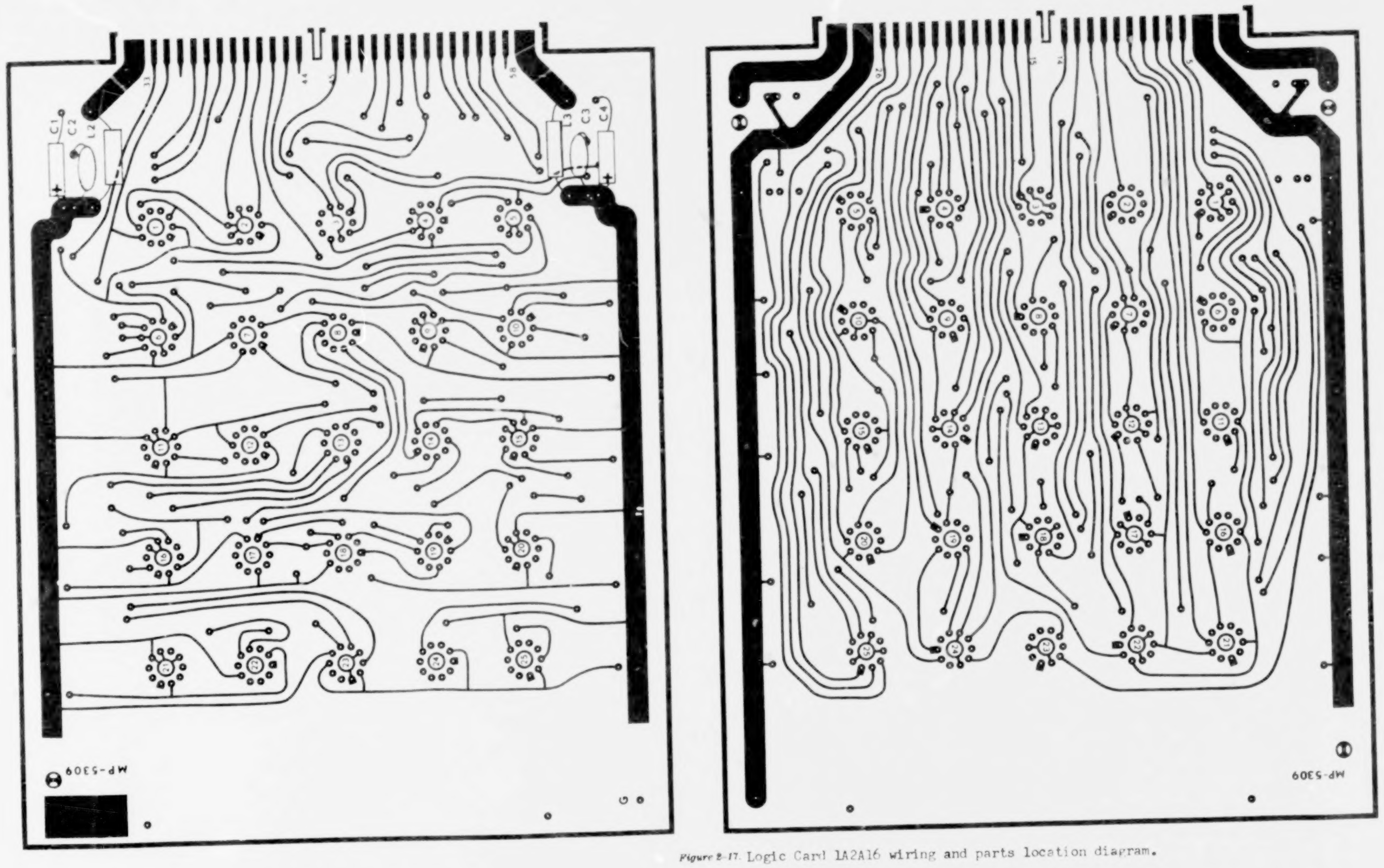
Figure 2-16. Logic Card 1A2A15 wiring and parts location diagram.



POSITION NO	INTEGRATED CIRCUIT MODULE
1	C7970K
2	C7974K
3	C7972K
4	C7974K
5	C7974K
6	C7974K
7	C7970K
8	C7976K
9	C7974K
10	C7974K
11	C7974K
12	C7970K
13	C7972K
14	C7970K
15	C7974K
16	C7974K
17	C7970K
18	C7970K
19	C7976K
20	C7974K
21	C7974K
22	C7974K
23	C7972K
24	C7970K
25	C7972K

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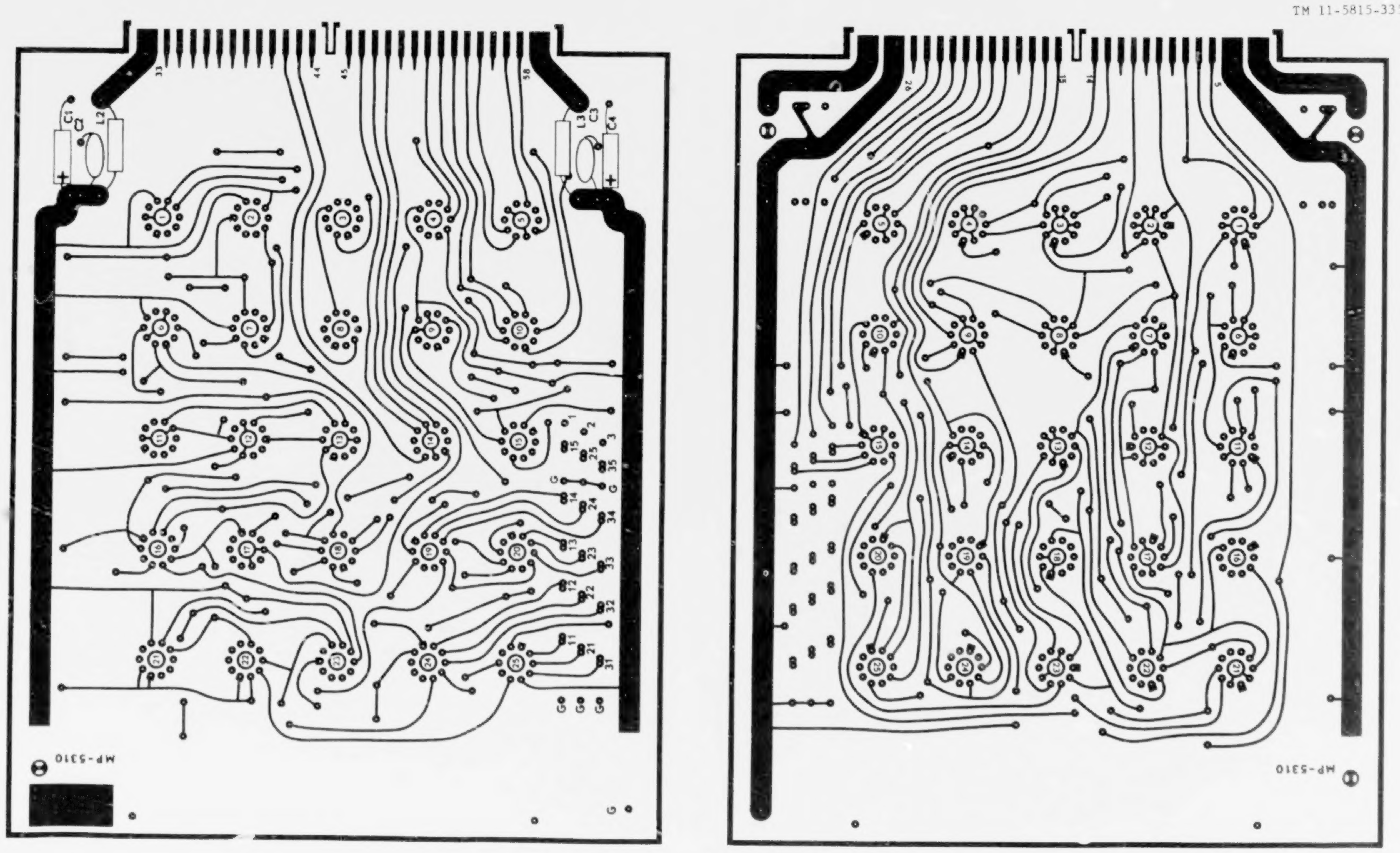
Figure 2-17. Logic Card 1A2A16 wiring and parts location diagram.



POSITION NO.	INTEGRATED CIRCUIT MODULE
1	C7972K
2	C7972K
3	C7972K
4	C7972K
5	C7970K
6	C7970K
7	C7970K
8	C7975K
9	C7975K
10	C7975K
11	C7970K
12	C7970K
13	C7968K
14	C7968K
15	C7968K
16	C7971K
17	C7970K
18	C7968K
19	C7968K
20	C7968K
21	C7971K
22	C7971K
23	C7973K
24	C7968K
25	C7968K

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Figure 2-18. Logic Card 1A2A17 wiring and parts location diagram.

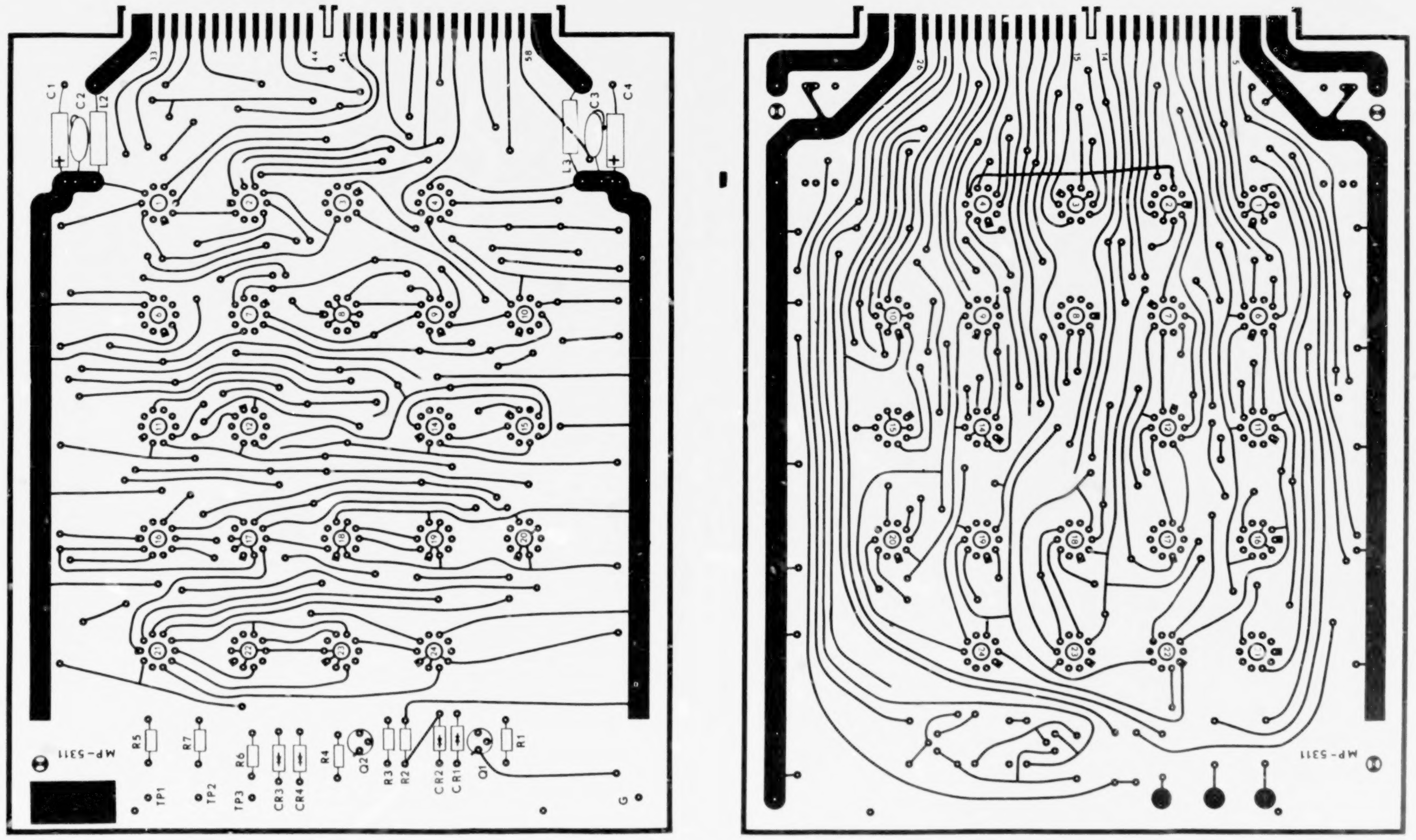
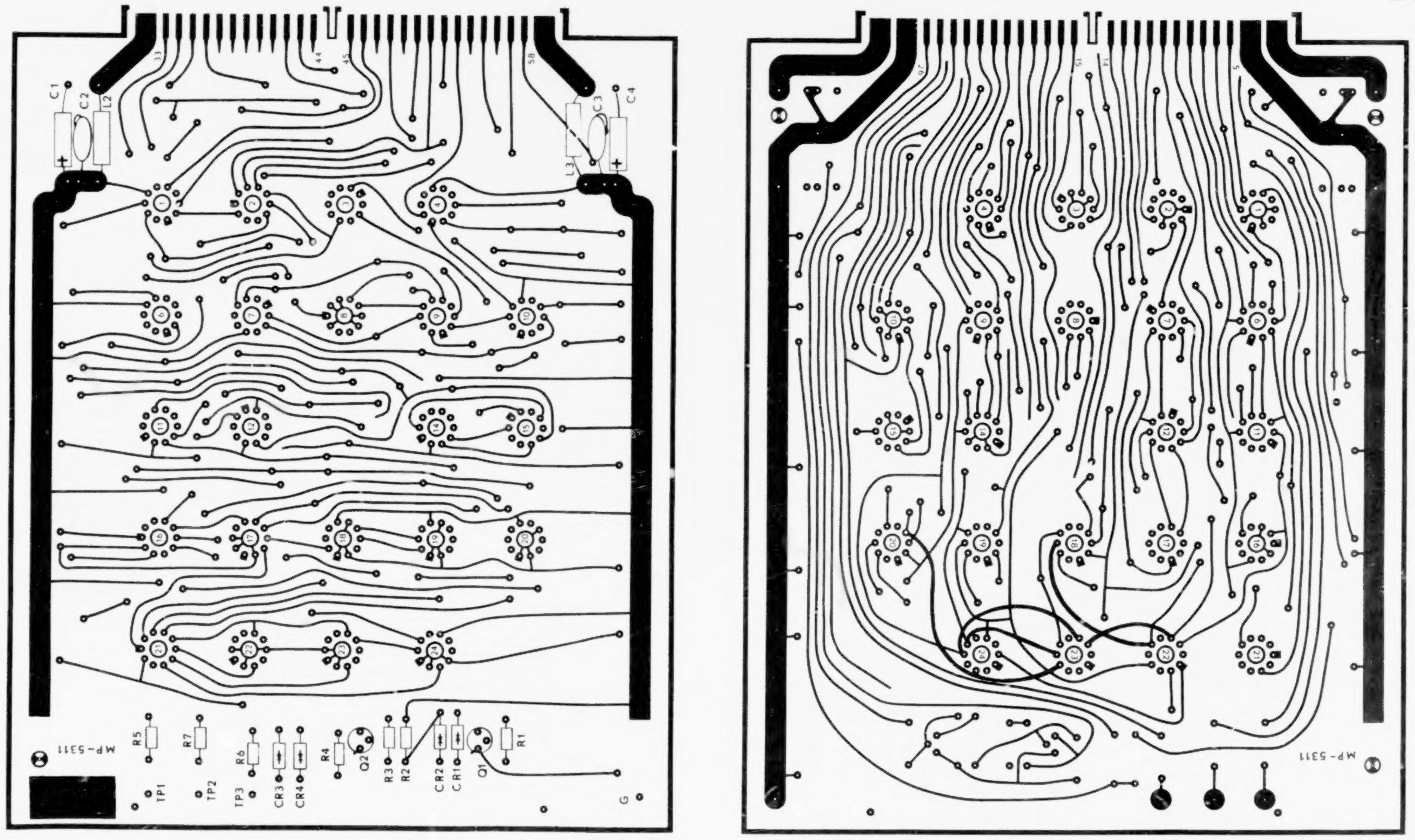

C1
C2
L2
L3
C3
C4
R5
R7
R6
R4
Q2
R3
R2
CR2
CR1
Q1
R1
TP1
TP2
TP3
CR3
CR4
G
MP-5311
MP-5311

Figure 2-19. Logic Card 1A2A18 wiring and parts location diagram.

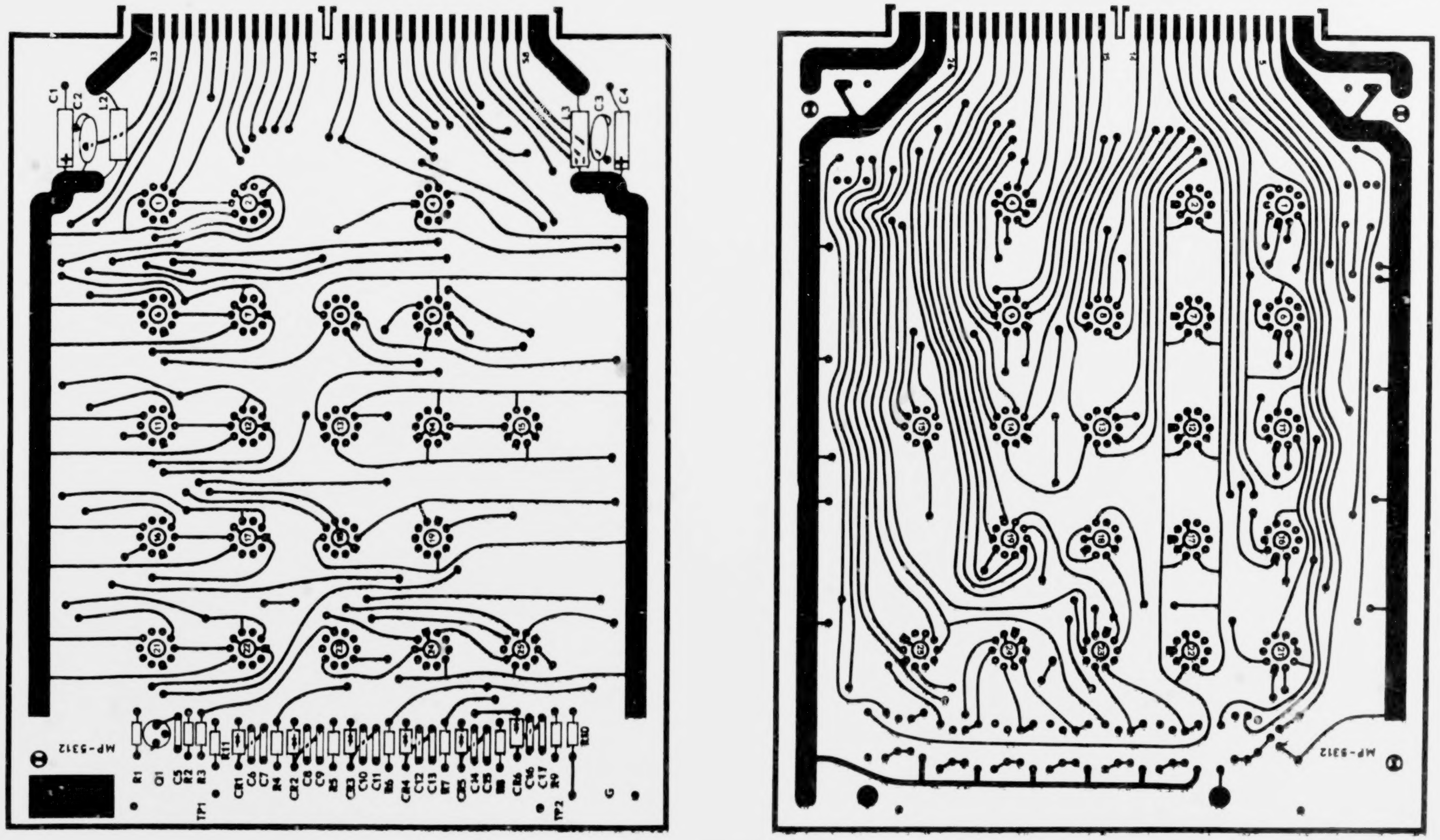
POSITION NO	INTEGRATED CIRCUIT MODULE
1	C7972K
2	C7976K
3	C7974K
4	C7970K
5	NOT EQUIPPED
6	C7974K
7	C7974K
8	C7976K
9	C7974K
10	C7976K
11	C7974K
12	C7974K
13	NOT EQUIPPED
14	C7974K
15	C7974K
16	C7971K
17	C7971K
18	C7971K
19	C7971K
20	C7971K
21	C7971K
22	C7971K
23	C7971K
24	C7971K
25	NOT EQUIPPED


C1
C2
L2
L3
C3
C4
R5
R7
R6
R4
R3
R2
CR2
CR1
Q2
Q1
R1
TP1
TP2
TP3
CR3
CR4
G
MP-5311
21
22
23
24
MP-5311

POSITION NO	INTEGRATED CIRCUIT MODULE
1	C7972K
2	C7976K
3	C7974K
4	C7970K
5	NOT EQUIPPED
6	C7974K
7	C7974K
8	C7976K
9	C7974K
10	C7976K
11	C7974K
12	C7974K
13	NOT EQUIPPED
14	C7974K
15	C7974K
16	C7971K
17	C7971K
18	C7971K
19	C7971K
20	C7971K
21	C7971K
22	C7971K
23	C7971K
24	C7971K
25	NOT EQUIPPED

EL 5895-438-35-C3-2

Figure 2-19.1 Logic Card 1A2A18 wiring and parts location diagram (showing modified wiring for Precedence Character W, AUTODIN MODE V).


C1
C2
L2
33
44
45
56
L3
C3
C4
MP-5312
R1
Q1
C5
R2
R3
R11
TP1
CR1
C6
C7
R4
CR2
C8
C9
R5
CR3
C10
C11
R6
CR4
C12
C13
R7
CR5
C14
C15
R8
CR6
C16
C17
R9
TP2
R10
G
MP-5312

POSITION NO.	INTEGRATED CIRCUIT MODULE
1	C7970K
2	C7972K
3	NOT EQUIPPED
4	C7976K
5	NOT EQUIPPED
6	C7970K
7	C7972K
8	C7976K
9	C7976K
10	NOT EQUIPPED
11	C7970K
12	C7972K
13	C7976K
14	C7976K
15	C7968K
16	C7970K
17	C7972K
18	C7972K
19	C7975K
20	NOT EQUIPPED
21	C7970K
22	C7972K
23	C7975K
24	C7968K
25	C7968K

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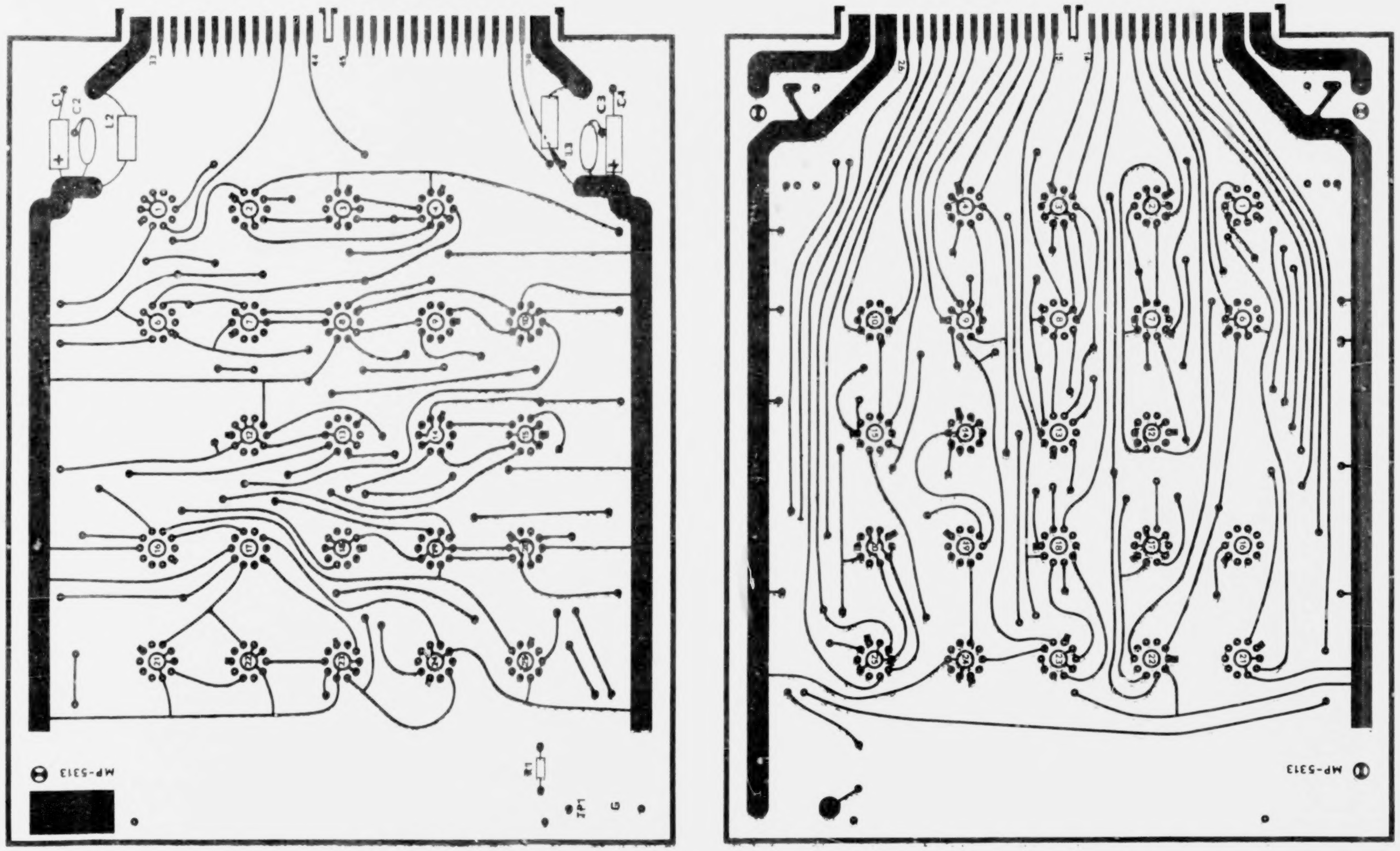
Figure 2-20. Logic Card 1A2A19 wiring and parts location diagram.



POSITION NO	INTEGRATED CIRCUIT MODULE
1	C7972K
2	C7976K
3	C7976K
4	C7976K
5	NOT EQUIPPED
6	C7976K
7	C7972K
8	C7976K
9	C7976K
10	C7972K
11	NOT EQUIPPED
12	C7976K
13	C7976K
14	C7972K
15	C7976K
16	C7970K
17	C7976K
18	C7972K
19	C7972K
20	C7972K
21	C7974K
22	C7974K
23	C7974K
24	C7974K
25	C7974K

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Figure 2-21. Logic Card 2A1 wiring and parts location diagram.

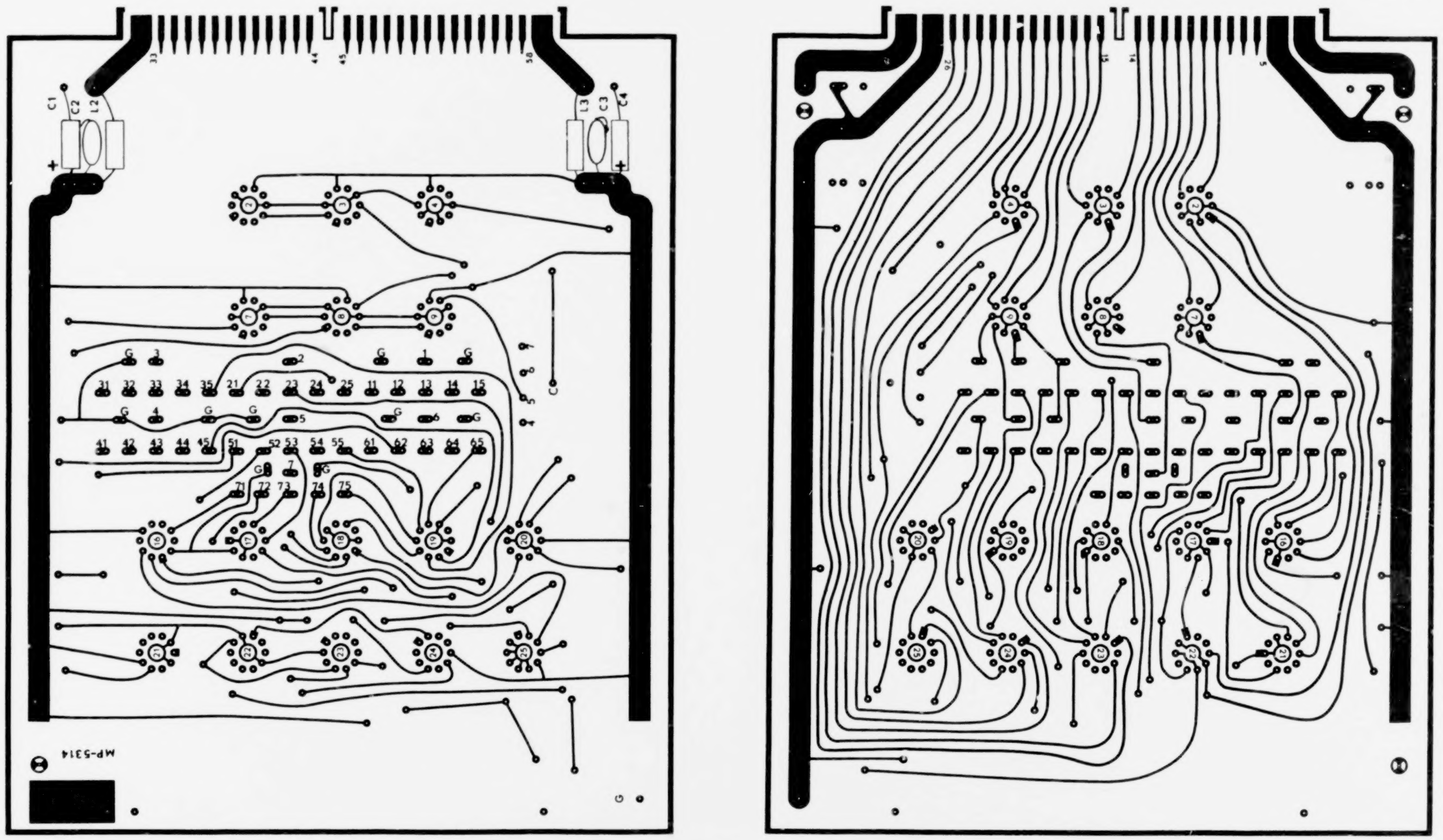

Figure 2-22. Logic Card 2A2 wiring and parts location diagram.

POSITION NO.	INTEGRATED CIRCUIT MODULE
1	NOT EQUIPPED
2	C7972K
3	C7972K
4	C7972K
5	NOT EQUIPPED
6	NOT EQUIPPED
7	C7972K
8	C7972K
9	C7972K
10	NOT EQUIPPED
11	NOT EQUIPPED
12	NOT EQUIPPED
13	NOT EQUIPPED
14	NOT EQUIPPED
15	NOT EQUIPPED
16	C7968K
17	C7968K
18	C7968K
19	C7968K
20	C7968K
21	C7968K
22	C7968K
23	C7975K
24	C7975K
25	C7975K

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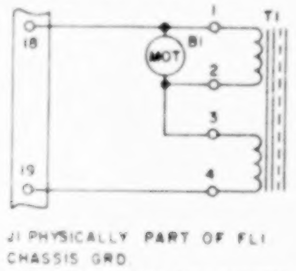
NOTES

1. WIRING SHOWN AS SEEN FROM THE WIRING SIDE
2. T INDICATES THREE WIRES TWISTED
3. RESISTOR A1R5 IS RESISTIVE WIRE
4. LOGIC CARD A1A1 INSERTS INTO A1J1
5. LOGIC CARD A1A2 INSERTS INTO A1J2.
6. PLUGS A3P1 AND A3P2 DO NOT EXIST
7. PLUG A1A3P3 MATES WITH JACK A1J3
8. CONNECTION FOR 230V AC


18
19
MOT
B1
T1
1
2
3
4

9. J1 PHYSICALLY PART OF FL1
10. CHASSIS GRD
11. WIRE DESTINATIONS LIST STATION NUMBER FOLLOWED BY TERMINAL NUMBER IN PARENTHESIS ( ).

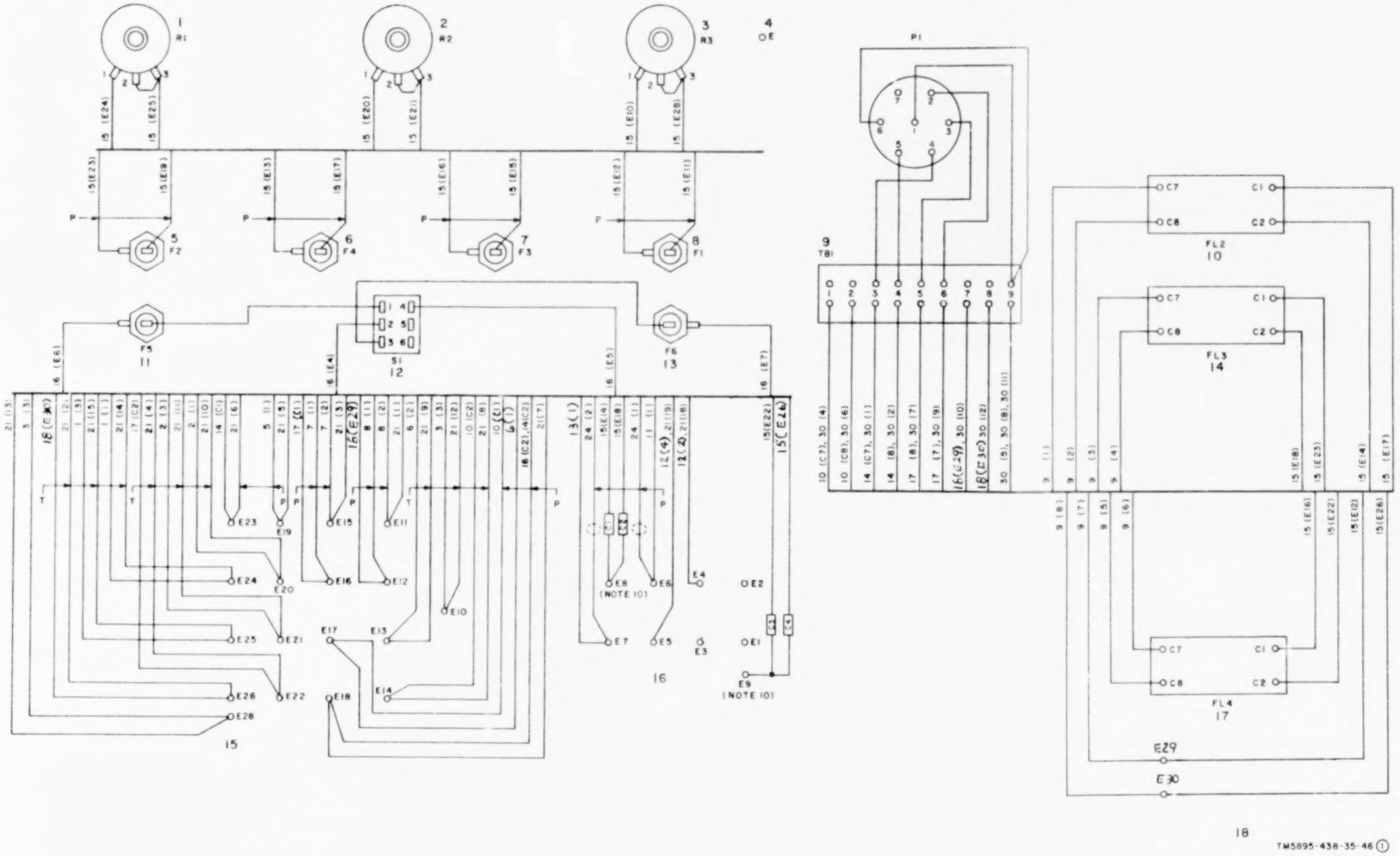

1
R1
2
R2
3
R3
4
E
P1
5
F2
6
F4
7
F3
8
F1
9
TB1
F5
11
S1
12
F6
13
FL2
10
FL3
14
FL4
17
C7
C8
C1
C2
T
P
E23
E19
E15
E11
E24
E20
E16
E12
E10
E8
(NOTE 10)
E6
E4
E2
E25
E21
E17
E13
E7
E5
E3
E1
16
E26
E22
E18
E14
E9
(NOTE 10)
E28
15
E29
E30
18

Figure 2-23①. Power Supply 1A3, wiring diagram (part 1 of 2).

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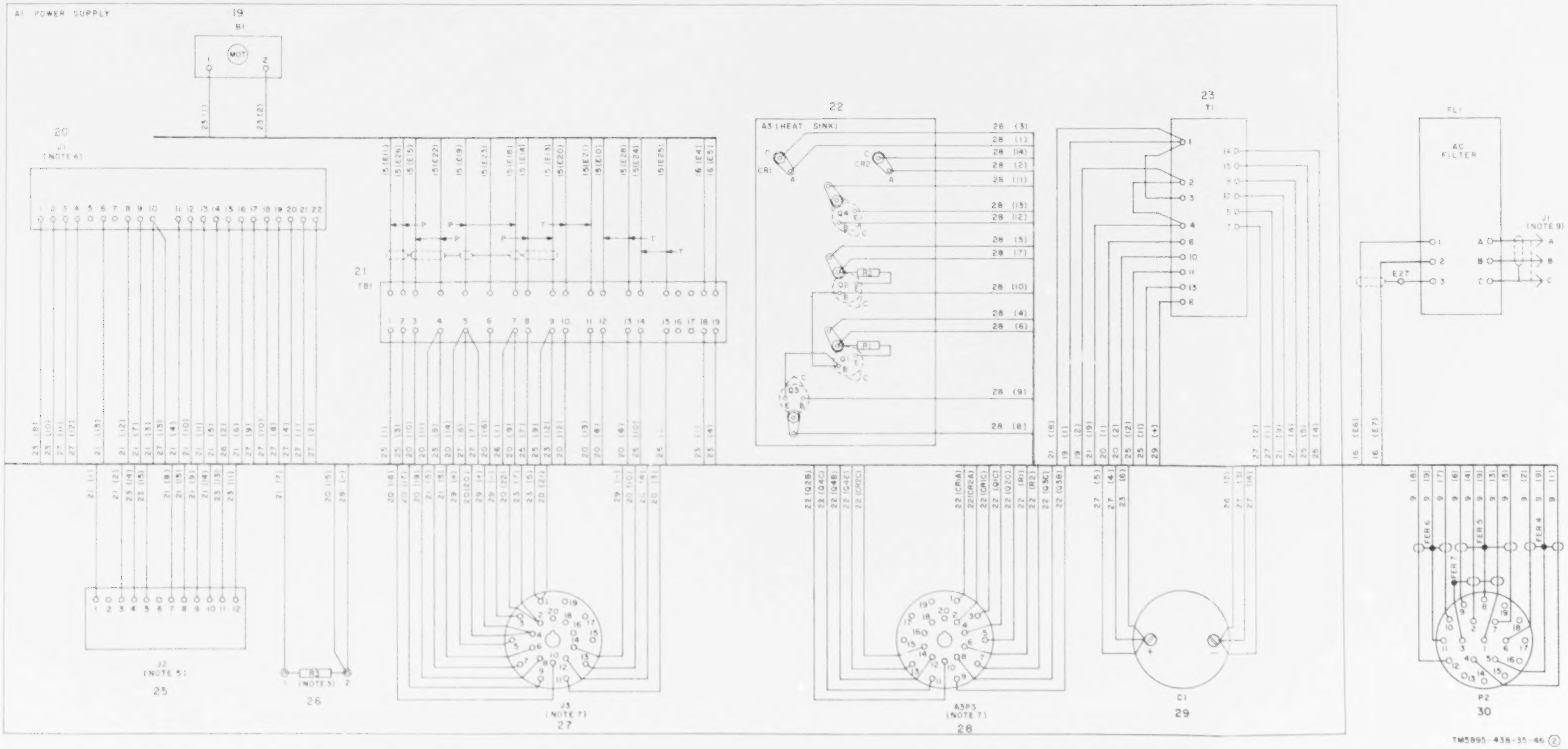
A1 POWER SUPPLY
19
B1
MOT
20
J1
(NOTE 4)
21
TB1
22
A3 (HEAT SINK)
CR1
CR2
Q1
Q2
Q3
Q4
R1
R2
23
T1
FL1
AC FILTER
J1
(NOTE 9)
E27
FER 4
FER 5
FER 6
FER 7
J2
(NOTE 5)
25
R1
(NOTE 3)
26
J3
(NOTE 7)
27
A3P3
(NOTE 7)
28
C1
29
P2
30
TM5895-438-35-46 ②

Figure 2-23②. Power Supply A5, wiring diagram (part 2 of 2).

NOTES

1. UNLESS OTHERWISE INDICATED ALL WIRING IS # 22 AWG BARE COPPER, WITH WHITE INSULATED SLEEVING FOR LONG RUNS
2. ◆◆P INDICATES TWISTED PAIR
3. ⊂⊃ INDICATES SHIELDING
4. SECTION 1, FRONT CONTACTS OF S6, IS NEAREST CONTROL KNOB
5. SWITCH S6 WAFER 5 USED FOR TERMINATING POINT ONLY, NO INTERNAL SWITCHING
6. WIRE DESTINATIONS LIST STATION NUMBER FOLLOWED BY TERMINAL NUMBER IN PARENTHESIS

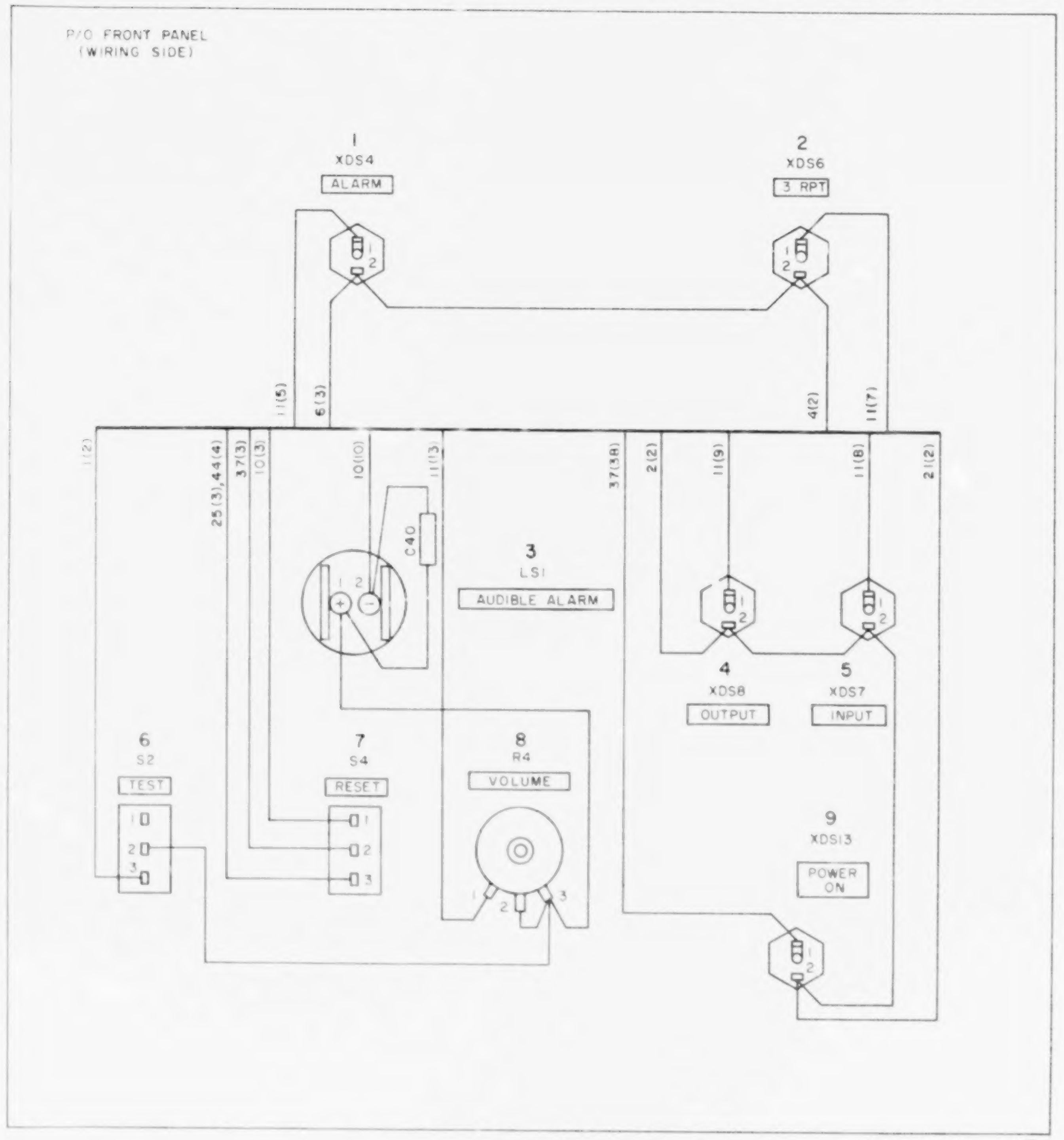
P/O FRONT PANEL
(WIRING SIDE)
1
XDS4
ALARM
2
XDS6
3 RPT
11(5)
6(3)
4(2)
11(7)
1(2)
25(3),44(4)
37(3)
10(3)
10(10)
11(13)
37(38)
2(2)
11(9)
11(8)
21(2)
C40
3
LS1
AUDIBLE ALARM
4
XDS8
OUTPUT
5
XDS7
INPUT
6
S2
TEST
7
S4
RESET
8
R4
VOLUME
9
XDS13
POWER ON

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Figure 2-24①. Control Indicator Panel A1, wiring diagram (part 1 of 4).

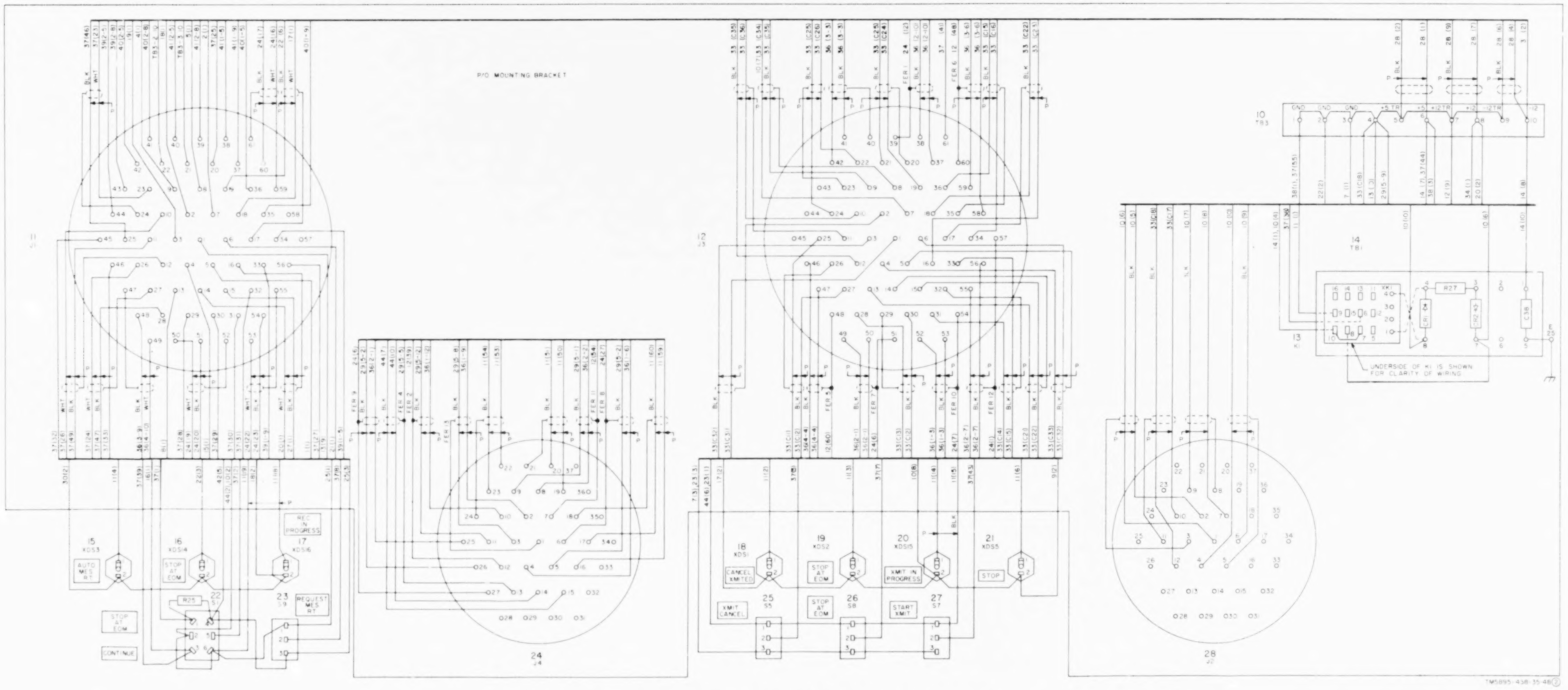

P/O MOUNTING BRACKET
11
J1
12
J3
10
TB3
GND
GND
GND
+5 TR
+5
+12TR
+12
-12TR
-12
14
TB1
13
K1
XK1
R27
CR1
CR2
C38
E
25
UNDERSIDE OF K1 IS SHOWN FOR CLARITY OF WIRING
15
XDS3
AUTO MES RT
16
XDS14
STOP AT EOM
17
XDS16
REC IN PROGRESS
R25
22
S1
23
S9
REQUEST MES RT
STOP AT EOM
CONTINUE
24
J4
18
XDS1
CANCEL XMITED
19
XDS2
STOP AT EOM
20
XDS15
XMIT IN PROGRESS
21
XDS5
STOP
25
S5
XMIT CANCEL
26
S8
STOP AT EOM
27
S7
START XMIT
28
J2
BLK
WHT
P
TM5895-438-35-48②

Figure 2-24②. Control Indicator Panel A1, wiring diagram (part 2 of 4).

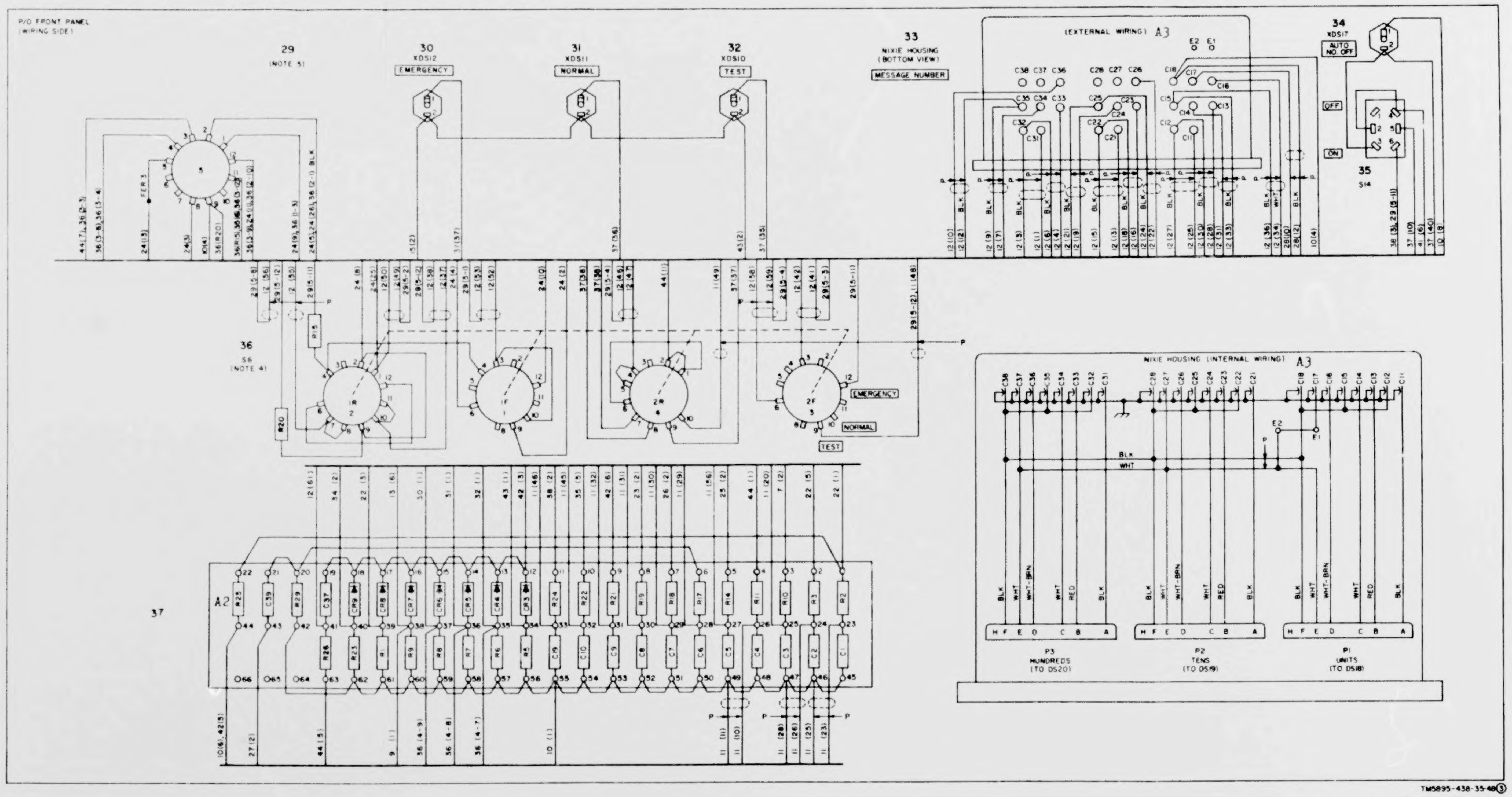
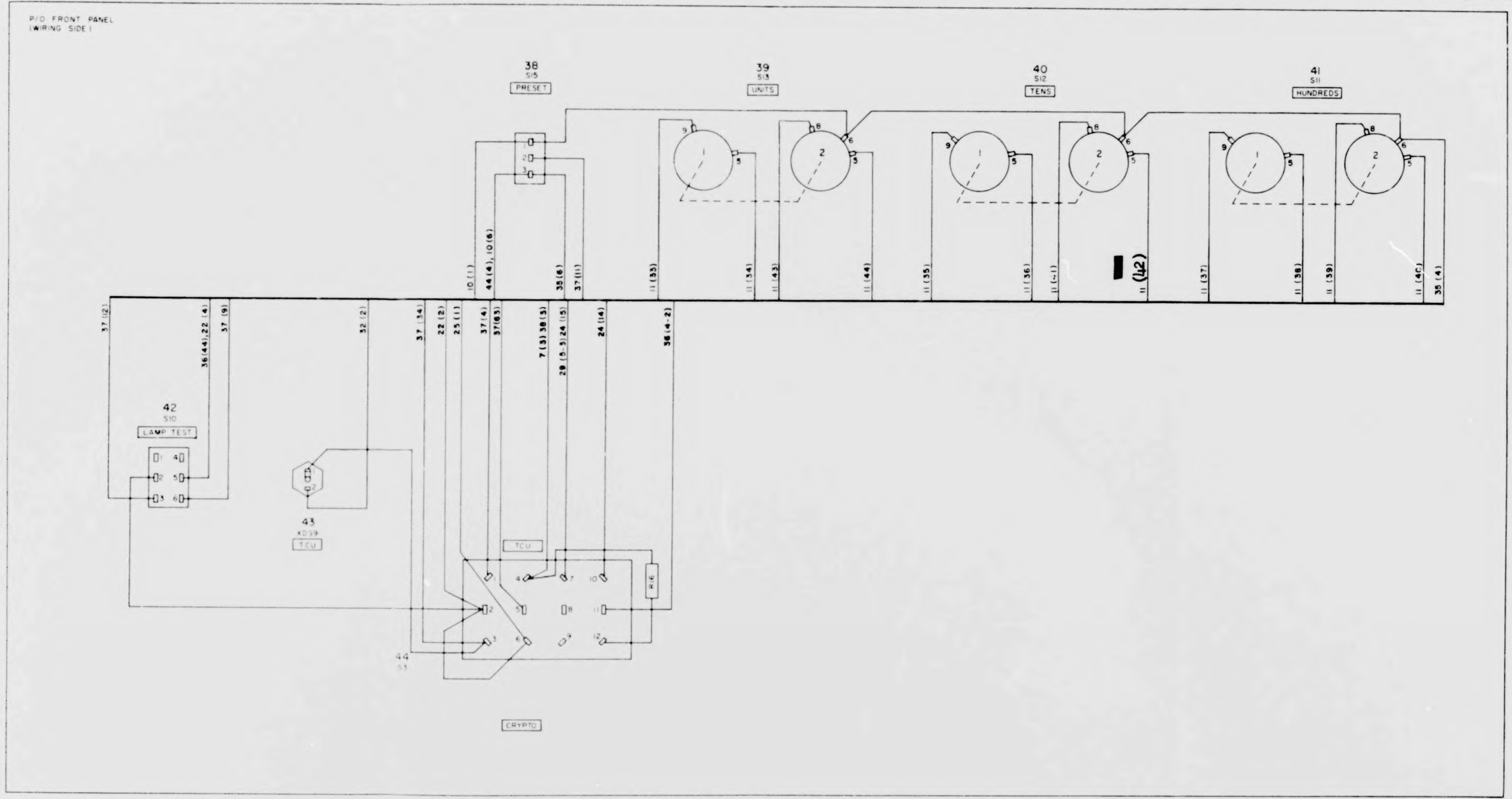
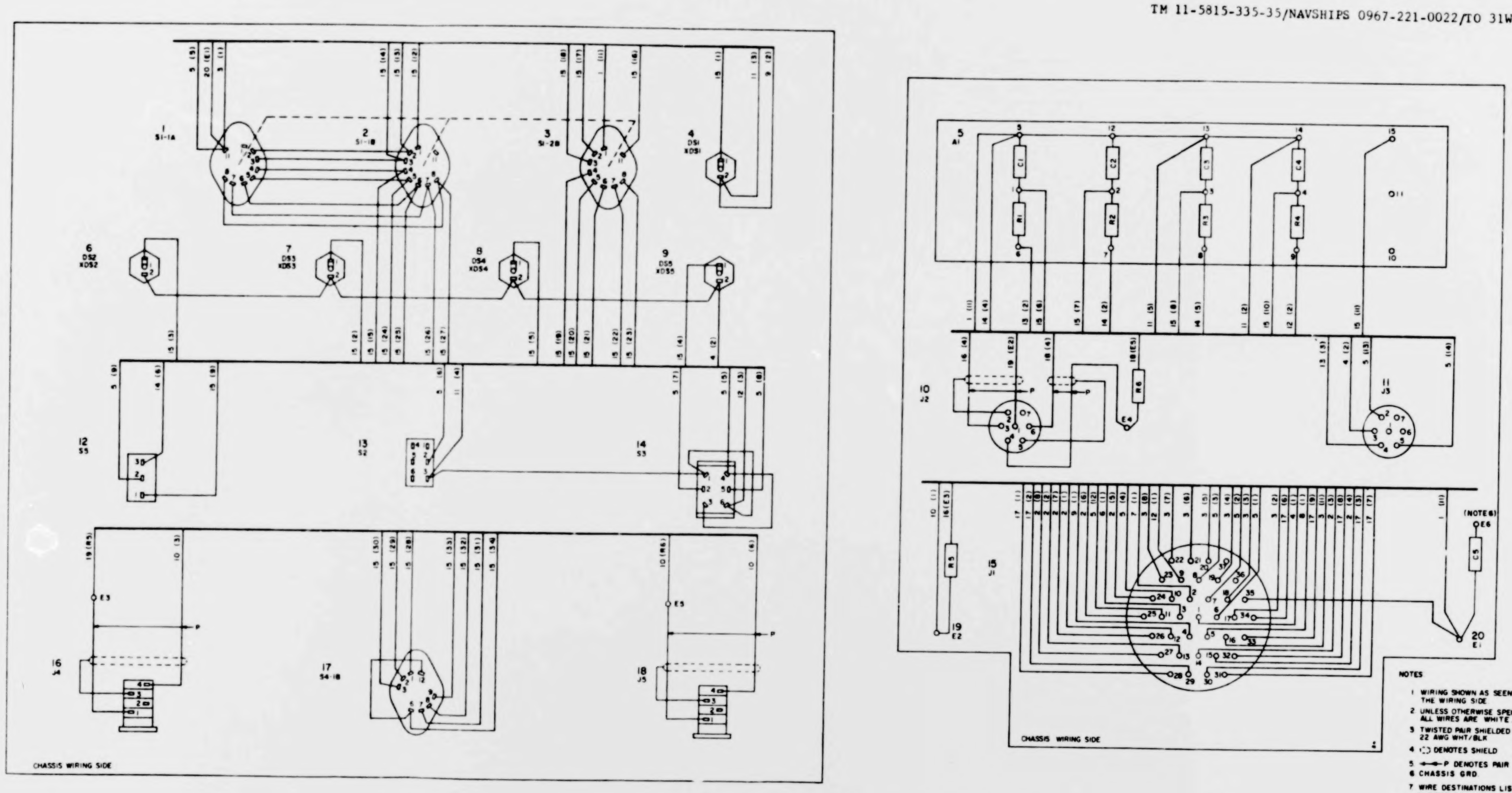

P/O FRONT PANEL
(WIRING SIDE)
29
(NOTE 5)
30
XDS12
EMERGENCY
31
XDS11
NORMAL
32
XDS10
TEST
33
NIXIE HOUSING
(BOTTOM VIEW)
MESSAGE NUMBER
(EXTERNAL WIRING) A3
34
XDS17
AUTO
NO OFF
OFF
ON
35
S14
36
S6
(NOTE 4)
EMERGENCY
NORMAL
TEST
NIXIE HOUSING (INTERNAL WIRING) A3
P3
HUNDREDS
(TO DS20)
P2
TENS
(TO DS19)
P1
UNITS
(TO DS18)
37
A2
TM5895-438-35-48③

Figure 2-24③ Control Indicator Panel 1A1, wiring diagram (part 3 of 4).


P/O FRONT PANEL
(WIRING SIDE)
38
S15
PRESET
39
S13
UNITS
40
S12
TENS
41
S11
HUNDREDS
1
2
9
8
6
5
10 (1)
44 (4), 10 (6)
35 (6)
37 (11)
11 (33)
11 (34)
11 (43)
11 (44)
11 (35)
11 (36)
11 (41)
11 (42)
11 (37)
11 (38)
11 (39)
11 (40)
35 (4)
37 (12)
36 (44), 22 (4)
37 (9)
32 (2)
37 (34)
22 (2)
25 (1)
37 (4)
37 (63)
7 (3) 38 (5)
29 (5-3) 24 (15)
24 (14)
36 (4-2)
42
S10
LAMP TEST
43
XDS9
TCU
TCU
R16
44
S3
CRYPTO

TM5895-438-35-48④

Figure 2-24④. Control Indicator Panel A1, wiring diagram (part 4 of 4).


1
S1-1A
2
S1-1B
3
S1-2B
4
DS1
XDS1
6
DS2
XDS2
7
DS3
XDS3
8
DS4
XDS4
9
DS5
XDS5
12
S5
13
S2
14
S3
16
J4
17
S4-1B
18
J5
E3
E5
P
CHASSIS WIRING SIDE
5
A1
C1
C2
C3
C4
R1
R2
R3
R4
10
J2
11
J3
R6
E4
15
J1
R5
19
E2
C5
E6
(NOTE 6)
20
E1
CHASSIS WIRING SIDE

NOTES

1 WIRING SHOWN AS SEEN FROM THE WIRING SIDE
2 UNLESS OTHERWISE SPECIFIED, ALL WIRES ARE WHITE
3 TWISTED PAIR SHIELDED WIRES ARE 22 AWG WHT/BLK
4 (⁚⁚) DENOTES SHIELD
5 ←→P DENOTES PAIR
6 CHASSIS GRD
7 WIRE DESTINATIONS LIST STATION NUMBER FOLLOWED BY TERMINAL NUMBER IN PARENTHESIS ( ).

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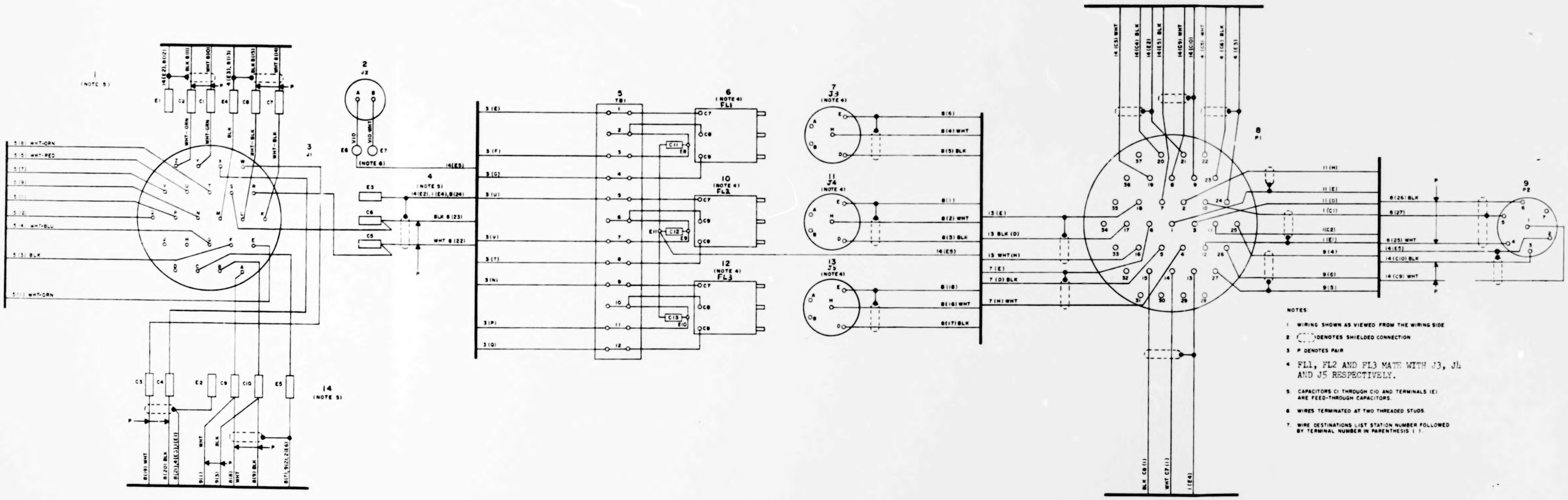
Figure 2-25. Simulation Test Unit 1A4, wiring diagram.


1
(NOTE 5)
2
J2
A
B
VIO
VIO WHT
E6
E7
(NOTE 6)
3
J1
4
(NOTE 5)
E3
C6
C5
BLK 8 (23)
WHT 8 (22)
5
TB1
6
(NOTE 4)
FL1
10
(NOTE 4)
FL2
12
(NOTE 4)
FL3
C11
C12
C13
E8
E9
E10
E11
7
J3
(NOTE 4)
11
J4
(NOTE 4)
13
J5
(NOTE 4)
8
P1
9
P2
14
(NOTE 5)
E1
C2
C1
E4
C8
C7
C3
C4
E2
C9
C10
E5
P
5 (8) WHT-ORN
5 (5) WHT-RED
5 (7)
5 (9)
5 (1)
5 (2)
5 (4) WHT-BLU
5 (3) BLK
5 (1) WHT-ORN
3 (E)
3 (F)
3 (G)
3 (U)
3 (V)
3 (T)
3 (N)
3 (P)
3 (Q)
14 (E5)
8 (6)
8 (4) WHT
8 (5) BLK
8 (1)
8 (2) WHT
8 (3) BLK
8 (18)
8 (16) WHT
8 (17) BLK
13 (E)
13 BLK (D)
13 WHT (H)
7 (E)
7 (D) BLK
7 (H) WHT
11 (H)
11 (E)
11 (D)
1 (C1)
1 (C2)
1 (E1)
9 (4)
9 (6)
9 (5)
8 (26) BLK
8 (27)
8 (25) WHT
14 (E5)
14 (C10) BLK
14 (C9) WHT
BLK C8 (1)
WHT C7 (1)
1 (E4)

NOTES:

1 WIRING SHOWN AS VIEWED FROM THE WIRING SIDE

2 ( ) DENOTES SHIELDED CONNECTION

3 P DENOTES PAIR

4 FL1, FL2 AND FL3 MATE WITH J3, J4 AND J5 RESPECTIVELY.

5 CAPACITORS C1 THROUGH C10 AND TERMINALS (E) ARE FEED-THROUGH CAPACITORS.

6 WIRES TERMINATED AT TWO THREADED STUDS.

7 WIRE DESTINATIONS LIST STATION NUMBER FOLLOWED BY TERMINAL NUMBER IN PARENTHESIS ( ).

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Figure 2-26. T-R Filter 1A5, wiring diagram.

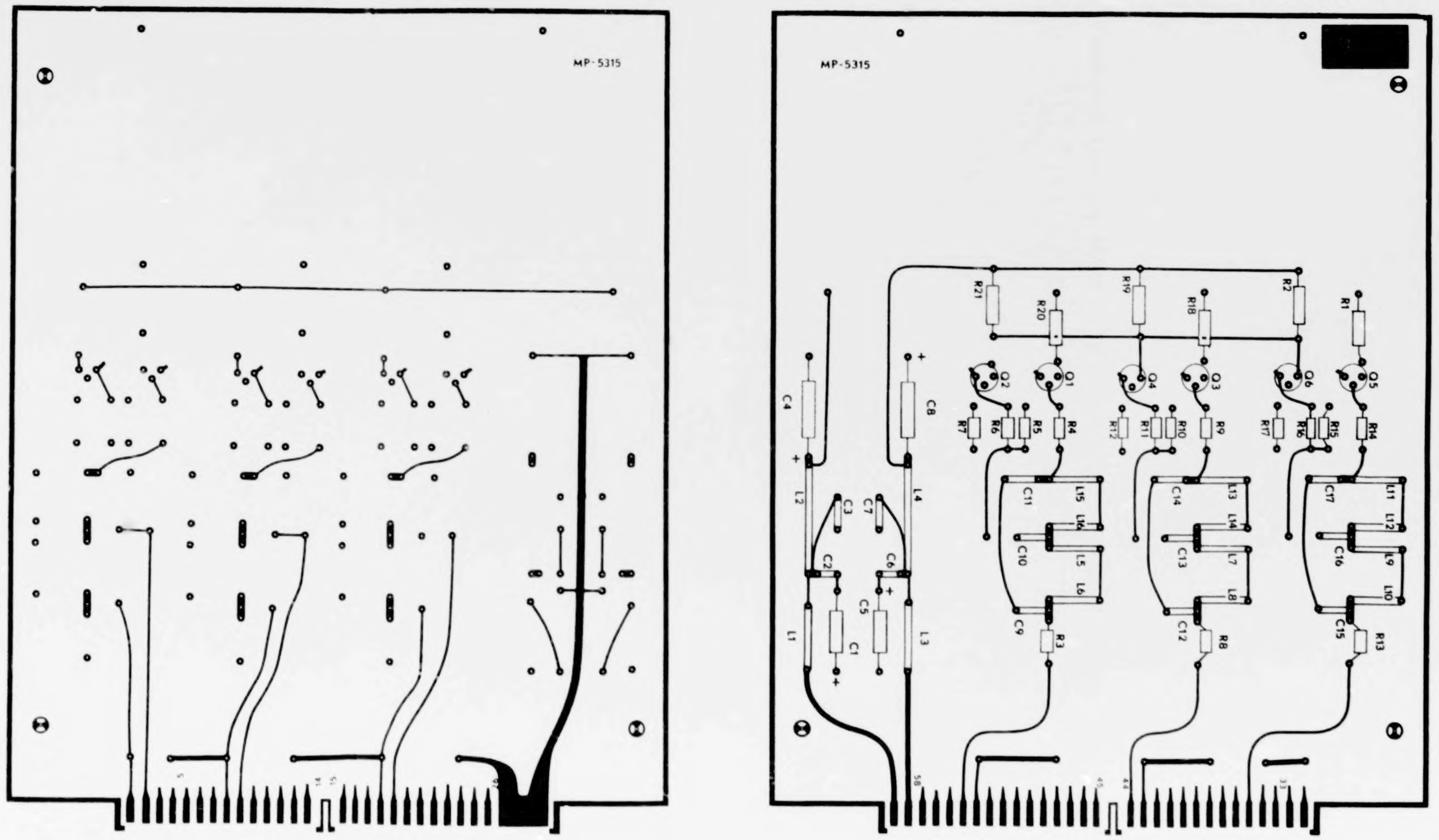
MP-5315
MP-5315
R21
R20
R19
R18
R2
R1
Q2
Q1
Q4
Q3
Q6
Q5
R7
R6
R5
R4
R12
R11
R10
R9
R17
R16
R15
R14
C4
C8
+
+
+
+
L2
L4
C3
C7
C2
C6
C5
C1
L1
L3
C11
L15
L16
C10
L5
L6
C9
R3
C14
L13
L14
C13
L7
L8
C12
R8
C17
L11
L12
C16
L9
L10
C15
R13
58
45
44
33

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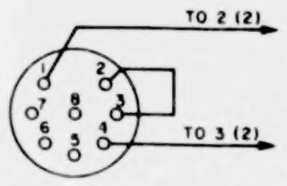
Figure 2-27. Logic Card A2A1, wiring and parts location diagram.

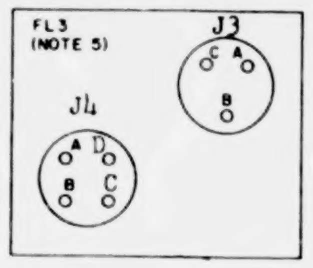
NOTES:

1. WIRING SHOWN AS SEEN FROM THE WIRING SIDE
2. PS1 SHOWN WIRED FOR 120 V OPERATION. FOR 230V OPERATION WIRE AS SHOWN BELOW FOR TERMINALS 1, 2, 3 AND 4 ONLY. REMAINING TERMINALS ARE NOT EFFECTED.



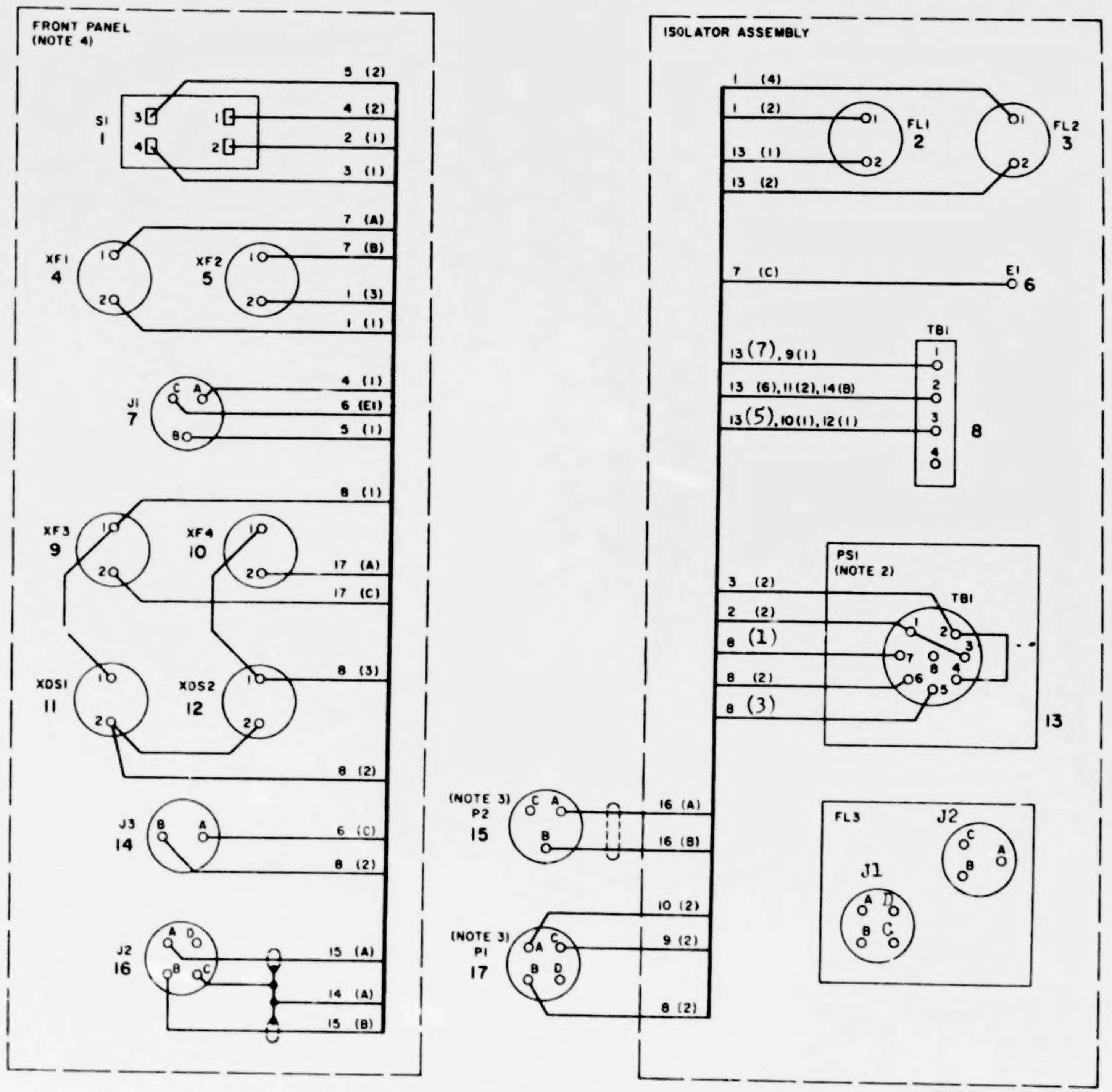
TO 2 (2)
1
2
7
8
3
6
4
5
TO 3 (2)

3. P1 MATES WITH J1 OF FL3, P2 MATES WITH J2 OF FL3.
4. FRONT PANEL TURNED 180 DEGREES.
5. REAR OF FILTER FL3 EXTENDS FROM REAR OF ASSEMBLY AS SHOWN BELOW.



FL3
(NOTE 5)
J3
C
A
B
J4
A
D
B
C

6. WIRE DESTINATIONS LIST STATION NUMBER FOLLOWED BY TERMINAL NUMBER IN PARENTHESIS



FRONT PANEL
(NOTE 4)
S1
1
5 (2)
4 (2)
2 (1)
3 (1)
XF1
4
XF2
5
7 (A)
7 (B)
1 (3)
1 (1)
J1
7
4 (1)
6 (E1)
5 (1)
XF3
9
XF4
10
8 (1)
17 (A)
17 (C)
XDS1
11
XDS2
12
8 (3)
8 (2)
J3
14
6 (C)
8 (2)
J2
16
15 (A)
14 (A)
15 (B)
(NOTE 3)
P2
15
16 (A)
16 (B)
(NOTE 3)
P1
17
10 (2)
9 (2)
8 (2)
ISOLATOR ASSEMBLY
1 (4)
1 (2)
13 (1)
13 (2)
FL1
2
FL2
3
7 (C)
E1
6
TB1
13(7), 9(1)
13 (6), 11(2), 14(B)
13(5), 10(1), 12(1)
8
PS1
(NOTE 2)
TB1
3 (2)
2 (2)
8 (1)
8 (2)
8 (3)
13
FL3
J2
J1

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Figure 2-28. Isolator Assembly 2A6, wiring diagram.